

# 128K x 16 Static RAM

## Features

- Pin equivalent to CY7C1011BV33
- High speed
  - $t_{AA} = 10 \text{ ns}$
- Low active power
  - 360 mW (max.)
- Data Retention at 2.0
- Automatic power-down when deselected
- Independent control of upper and lower bits
- Easy memory expansion with  $\overline{CE}$  and  $\overline{OE}$  features
- Available in 44-pin TSOP II, 44-pin TQFP, and 48-ball VFBGA
- Also available in Lead-Free 44-pin TSOP II and 44-pin TQFP packages

## Functional Description

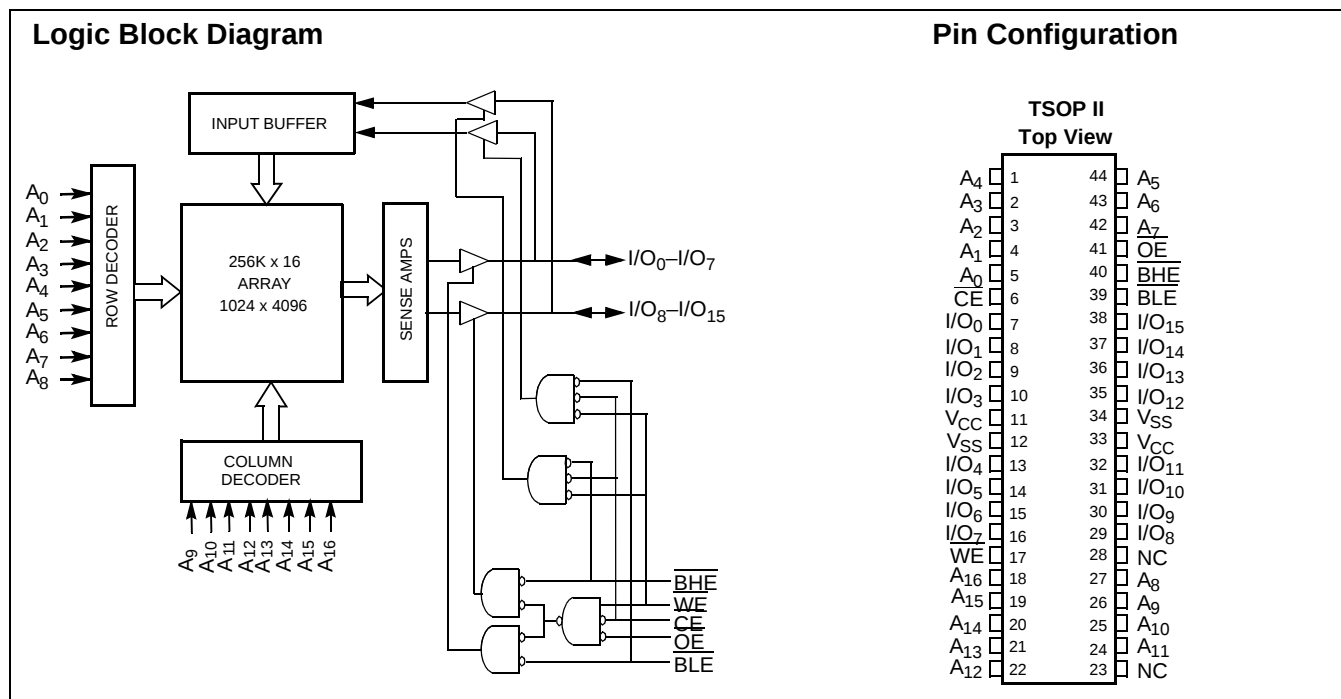
The CY7C1011CV33 is a high-performance CMOS Static RAM organized as 131,072 words by 16 bits.

Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from I/O pins ( $I/O_0$  through  $I/O_7$ ), is written into the location specified on the address pins ( $A_0$  through  $A_{16}$ ). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from I/O pins ( $I/O_8$  through  $I/O_{15}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{16}$ ).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins will appear on  $I/O_0$  to  $I/O_7$ . If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory will appear on  $I/O_8$  to  $I/O_{15}$ . See the truth table at the back of this data sheet for a complete description of read and write modes.

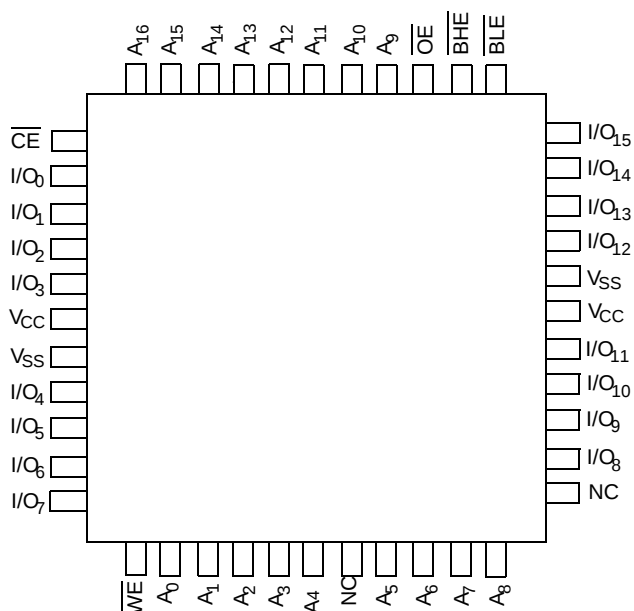
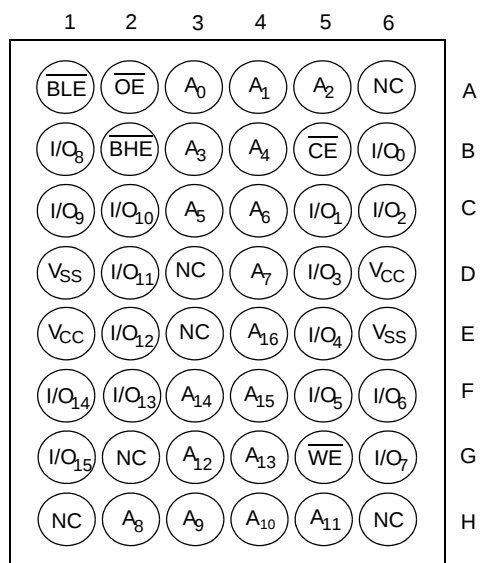
The input/output pins ( $I/O_0$  through  $I/O_{15}$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), the  $\overline{BHE}$  and  $\overline{BLE}$  are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW, and  $\overline{WE}$  LOW).

The CY7C1011CV33 is available in a standard 44-pin TSOP II package with center power and ground pinout, a 44-pin Thin Plastic Quad Flatpack (TQFP), as well as a 48-ball fine-pitch ball grid array (VFBGA) package.



**Selection Guide**

|                              |             | -10 | -12 | -15 | Unit |
|------------------------------|-------------|-----|-----|-----|------|
| Maximum Access Time          |             | 10  | 12  | 15  | ns   |
| Maximum Operating Current    | Com'l       | 90  | 85  | 80  | mA   |
|                              | Ind'l       | 100 | 95  | 90  |      |
| Maximum CMOS Standby Current | Com'l/Ind'l | 10  | 10  | 10  | mA   |

**Pin Configurations**
**44-pin TQFP  
(Top View)**

**48-ball VFBGA  
(Top View)**


**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with  
Power Applied ..... -55°C to +125°C

Supply Voltage on  $V_{CC}$  to Relative GND<sup>[2]</sup> .... -0.5V to +4.6V

DC Voltage Applied to Outputs  
in High-Z State<sup>[2]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

DC Input Voltage<sup>[2]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

Current into Outputs (LOW) ..... 20 mA

**Operating Range**

| Range      | Ambient Temperature | $V_{CC}$    |
|------------|---------------------|-------------|
| Commercial | 0°C to +70°C        | 3.3V ± 0.3V |
| Industrial | -40°C to +85°C      |             |

**DC Electrical Characteristics** Over the Operating Range

| Parameter | Description                                   | Test Conditions                                                                                                       | -10             |                | -12  |                | -15  |                | Unit |
|-----------|-----------------------------------------------|-----------------------------------------------------------------------------------------------------------------------|-----------------|----------------|------|----------------|------|----------------|------|
|           |                                               |                                                                                                                       | Min.            | Max.           | Min. | Max.           | Min. | Max.           |      |
| $V_{OH}$  | Output HIGH Voltage                           | $V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$                                                                      | 2.4             |                | 2.4  |                | 2.4  |                | V    |
| $V_{OL}$  | Output LOW Voltage                            | $V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$                                                                       |                 | 0.4            |      | 0.4            |      | 0.4            | V    |
| $V_{IH}$  | Input HIGH Voltage                            |                                                                                                                       | 2.0             | $V_{CC} + 0.3$ | 2.0  | $V_{CC} + 0.3$ | 2.0  | $V_{CC} + 0.3$ | V    |
| $V_{IL}$  | Input LOW Voltage <sup>[1]</sup>              |                                                                                                                       | -0.3            | 0.8            | -0.3 | 0.8            | -0.3 | 0.8            | V    |
| $I_{IX}$  | Input Load Current                            | $GND \leq V_I \leq V_{CC}$                                                                                            | -1              | +1             | -1   | +1             | -1   | +1             | μA   |
| $I_{OZ}$  | Output Leakage Current                        | $GND \leq V_{OUT} \leq V_{CC},$<br>Output Disabled                                                                    | -1              | +1             | -1   | +1             | -1   | +1             | μA   |
| $I_{CC}$  | $V_{CC}$ Operating Supply Current             | $V_{CC} = \text{Max.}, f = f_{MAX} = 1/t_{RC}$                                                                        | Com'l           | 90             |      | 85             |      | 80             | mA   |
|           |                                               |                                                                                                                       | Ind'l           | 100            |      | 95             |      | 90             |      |
| $I_{SB1}$ | Automatic CE Power-down Current — TTL Inputs  | Max. $V_{CC}, \overline{CE} \geq V_{IH}$<br>$V_{IN} \geq V_{IH}$ or<br>$V_{IN} \leq V_{IL}, f = f_{MAX}$              |                 | 40             |      | 40             |      | 40             | mA   |
| $I_{SB2}$ | Automatic CE Power-down Current — CMOS Inputs | Max. $V_{CC},$<br>$\overline{CE} \geq V_{CC} - 0.3V,$<br>$V_{IN} \geq V_{CC} - 0.3V,$<br>or $V_{IN} \leq 0.3V, f = 0$ | Com'l/<br>Ind'l | 10             |      | 10             |      | 10             | mA   |

**Capacitance<sup>[2]</sup>**

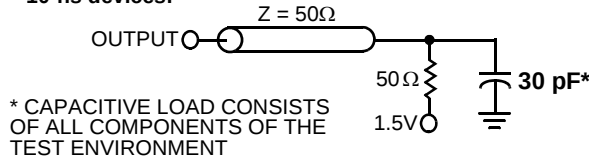
| Parameter | Description       | Test Conditions                                            | Max. | Unit |
|-----------|-------------------|------------------------------------------------------------|------|------|
| $C_{IN}$  | Input Capacitance | $T_A = 25^\circ\text{C}, f = 1 \text{ MHz}, V_{CC} = 3.3V$ | 8    | pF   |
| $C_{OUT}$ | I/O Capacitance   |                                                            | 8    | pF   |

**Notes:**

- $V_{IL}$  (min.) = -2.0V for pulse durations of less than 20 ns.
- Tested initially and after any design or process changes that may affect these parameters.

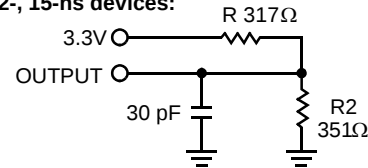
## AC Test Loads and Waveforms<sup>[3]</sup>

10-ns devices:



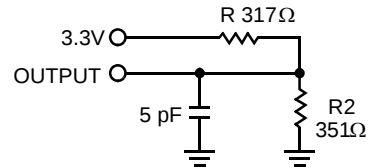
(a)

12-, 15-ns devices:

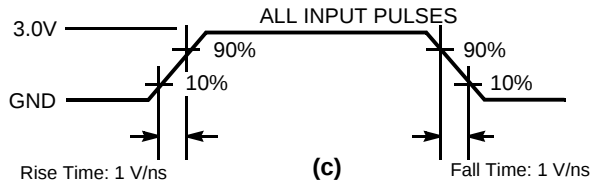


(b)

High-Z characteristics:



(d)



(c)

## AC Switching Characteristics Over the Operating Range<sup>[4]</sup>

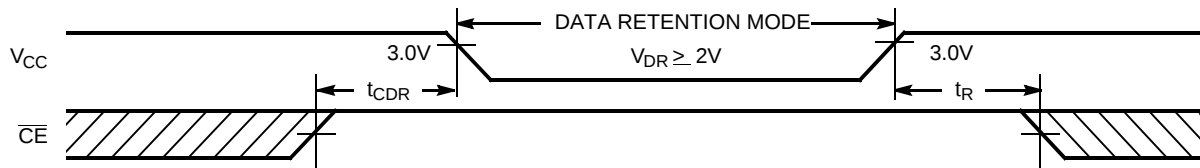
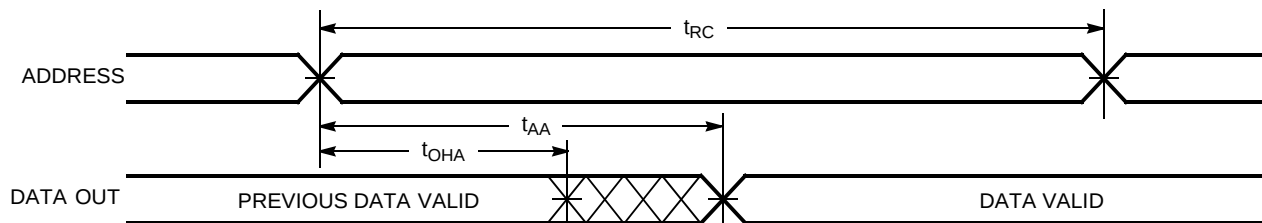
| Parameter                         | Description                                             | -10  |      | -12  |      | -15  |      | Unit |
|-----------------------------------|---------------------------------------------------------|------|------|------|------|------|------|------|
|                                   |                                                         | Min. | Max. | Min. | Max. | Min. | Max. |      |
| Read Cycle                        |                                                         |      |      |      |      |      |      |      |
| t <sub>power</sub> <sup>[5]</sup> | V <sub>CC</sub> (typical) to the first access           | 1    |      | 1    |      | 1    |      | μs   |
| t <sub>RC</sub>                   | Read Cycle Time                                         | 10   |      | 12   |      | 15   |      | ns   |
| t <sub>AA</sub>                   | Address to Data Valid                                   |      | 10   |      | 12   |      | 15   | ns   |
| t <sub>OHA</sub>                  | Data Hold from Address Change                           | 3    |      | 3    |      | 3    |      | ns   |
| t <sub>ACE</sub>                  | $\overline{\text{CE}}$ LOW to Data Valid                |      | 10   |      | 12   |      | 15   | ns   |
| t <sub>DOE</sub>                  | $\overline{\text{OE}}$ LOW to Data Valid                |      | 5    |      | 6    |      | 7    | ns   |
| t <sub>LZOE</sub>                 | $\overline{\text{OE}}$ LOW to Low-Z                     | 0    |      | 0    |      | 0    |      | ns   |
| t <sub>HZOE</sub>                 | $\overline{\text{OE}}$ HIGH to High-Z <sup>[6, 7]</sup> |      | 5    |      | 6    |      | 7    | ns   |
| t <sub>LZCE</sub>                 | $\overline{\text{CE}}$ LOW to Low-Z <sup>[7]</sup>      | 3    |      | 3    |      | 3    |      | ns   |
| t <sub>HZCE</sub>                 | $\overline{\text{CE}}$ HIGH to High-Z <sup>[6, 7]</sup> |      | 5    |      | 6    |      | 7    | ns   |
| t <sub>PU</sub>                   | $\overline{\text{CE}}$ LOW to Power-up                  | 0    |      | 0    |      | 0    |      | ns   |
| t <sub>PD</sub>                   | $\overline{\text{CE}}$ HIGH to Power-down               |      | 10   |      | 12   |      | 15   | ns   |
| t <sub>DBE</sub>                  | Byte Enable to Data Valid                               |      | 5    |      | 6    |      | 7    | ns   |
| t <sub>LZBE</sub>                 | Byte Enable to Low-Z                                    | 0    |      | 0    |      | 0    |      | ns   |
| t <sub>HZBE</sub>                 | Byte Disable to High-Z                                  |      | 6    |      | 6    |      | 7    | ns   |
| Write Cycle <sup>[8, 9]</sup>     |                                                         |      |      |      |      |      |      |      |
| t <sub>WC</sub>                   | Write Cycle Time                                        | 10   |      | 12   |      | 15   |      | ns   |

### Notes:

- AC characteristics (except High-Z) for all 10-ns parts are tested using the load conditions shown in (a). All other speeds are tested using the Thevenin load shown in (b). High-Z characteristics are tested for all speeds using the test load shown in (d).
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V.
- $t_{\text{POWER}}$  gives the minimum amount of time that the power supply should be at typical  $V_{\text{CC}}$  values until the first memory access is performed.
- $t_{\text{HZOE}}$ ,  $t_{\text{HZCE}}$ , and  $t_{\text{HZWE}}$  are specified with a load capacitance of 5 pF as in part (d) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
- At any given temperature and voltage condition,  $t_{\text{HZCE}}$  is less than  $t_{\text{LZCE}}$ ,  $t_{\text{HZOE}}$  is less than  $t_{\text{LZOE}}$ , and  $t_{\text{HZWE}}$  is less than  $t_{\text{LZWE}}$  for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{\text{CE}}$  LOW, and  $\overline{\text{WE}}$  LOW.  $\overline{\text{CE}}$  and  $\overline{\text{WE}}$  must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle No. 3 ( $\overline{\text{WE}}$  controlled,  $\overline{\text{OE}}$  LOW) is the sum of  $t_{\text{HZWE}}$  and  $t_{\text{SD}}$ .

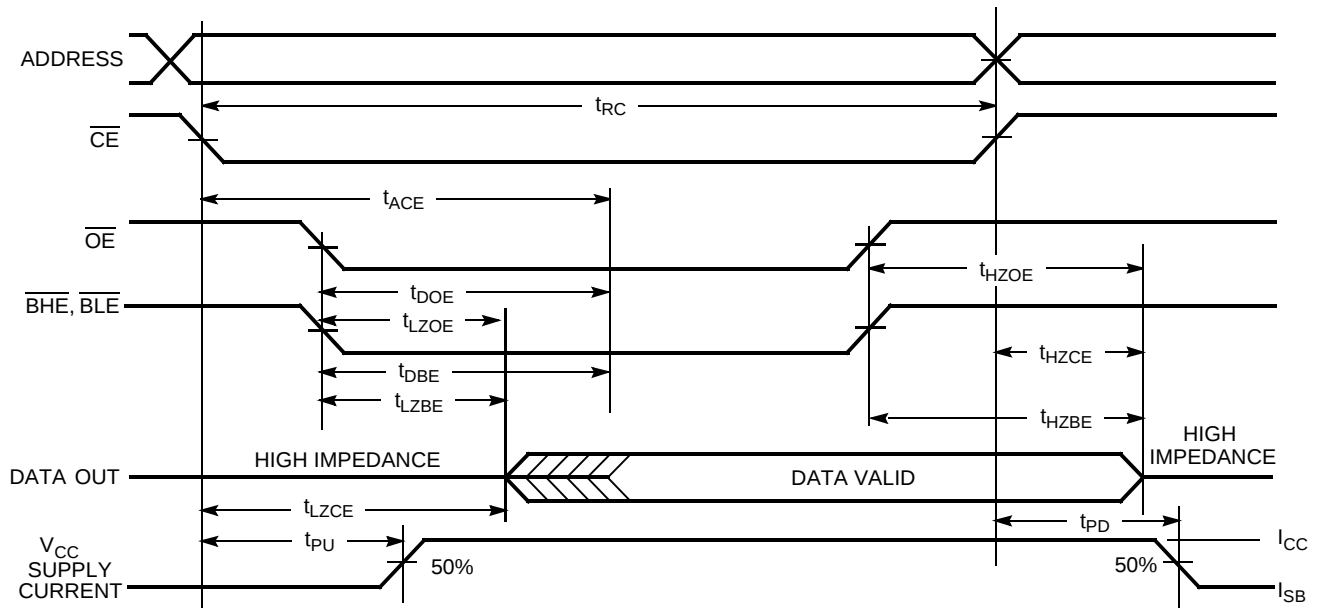
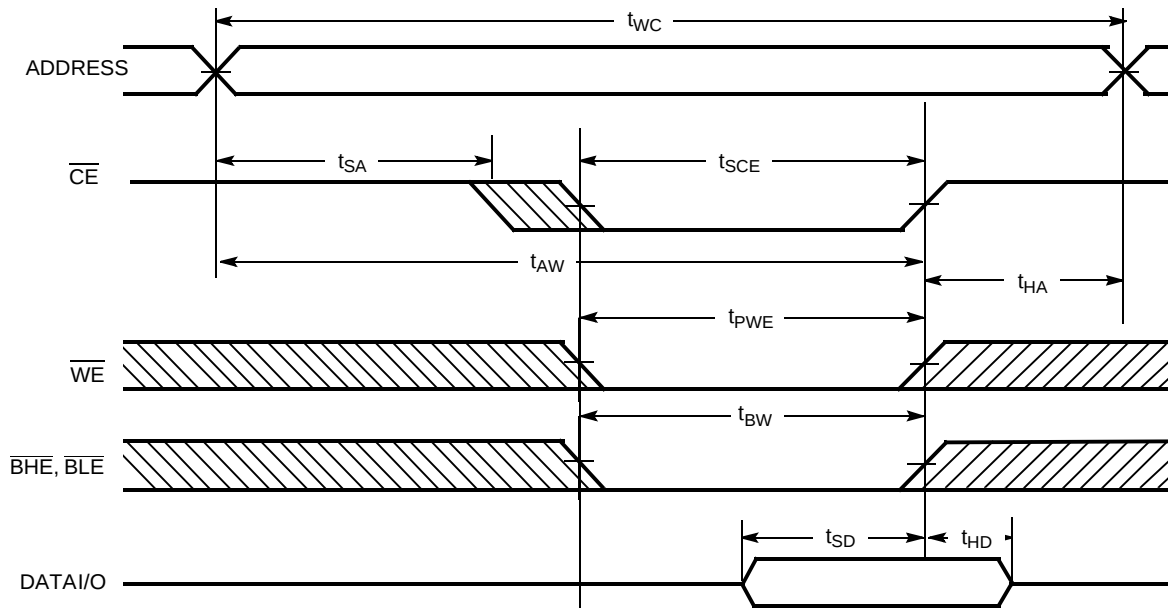
**AC Switching Characteristics** Over the Operating Range (continued)<sup>[4]</sup>

| Parameter  | Description                                     | -10  |      | -12  |      | -15  |      | Unit |
|------------|-------------------------------------------------|------|------|------|------|------|------|------|
|            |                                                 | Min. | Max. | Min. | Max. | Min. | Max. |      |
| $t_{SCE}$  | $\overline{CE}$ LOW to Write End                | 7    |      | 8    |      | 10   |      | ns   |
| $t_{AW}$   | Address Set-up to Write End                     | 7    |      | 8    |      | 10   |      | ns   |
| $t_{HA}$   | Address Hold from Write End                     | 0    |      | 0    |      | 0    |      | ns   |
| $t_{SA}$   | Address Set-up to Write Start                   | 0    |      | 0    |      | 0    |      | ns   |
| $t_{PWE}$  | $\overline{WE}$ Pulse Width                     | 7    |      | 8    |      | 10   |      | ns   |
| $t_{SD}$   | Data Set-up to Write End                        | 5    |      | 6    |      | 7    |      | ns   |
| $t_{HD}$   | Data Hold from Write End                        | 0    |      | 0    |      | 0    |      | ns   |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to Low-Z <sup>[7]</sup>    | 3    |      | 3    |      | 3    |      | ns   |
| $t_{HZWE}$ | $\overline{WE}$ LOW to High-Z <sup>[6, 7]</sup> |      | 5    |      | 6    |      | 7    | ns   |
| $t_{BW}$   | Byte Enable to End of Write                     | 7    |      | 8    |      | 10   |      | ns   |

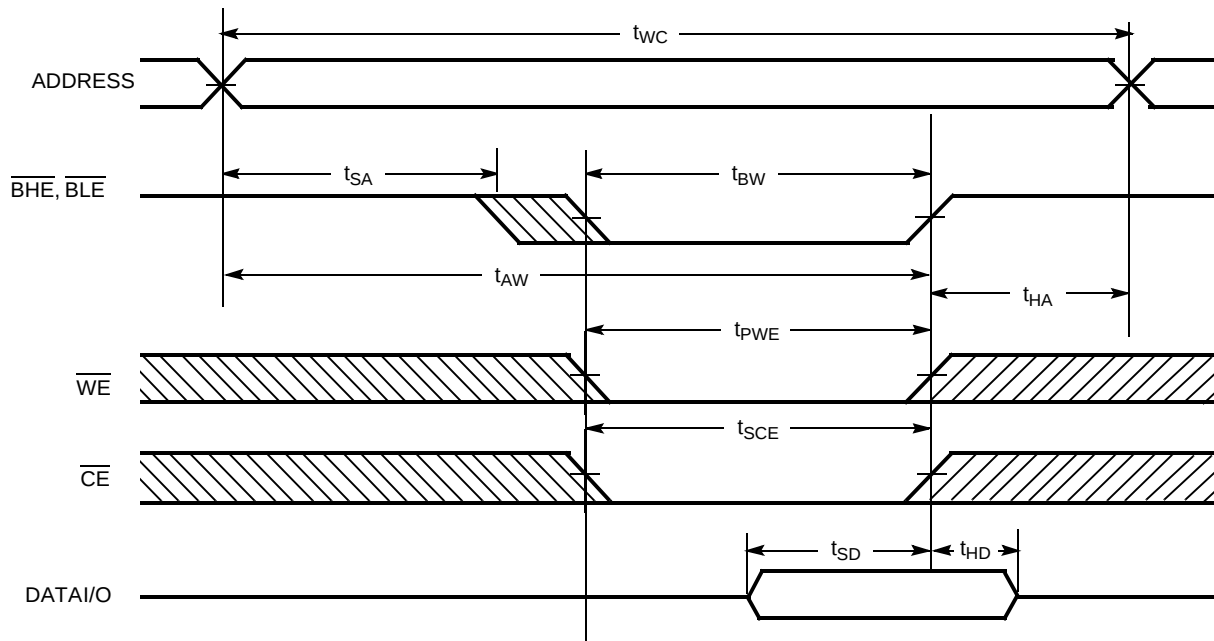
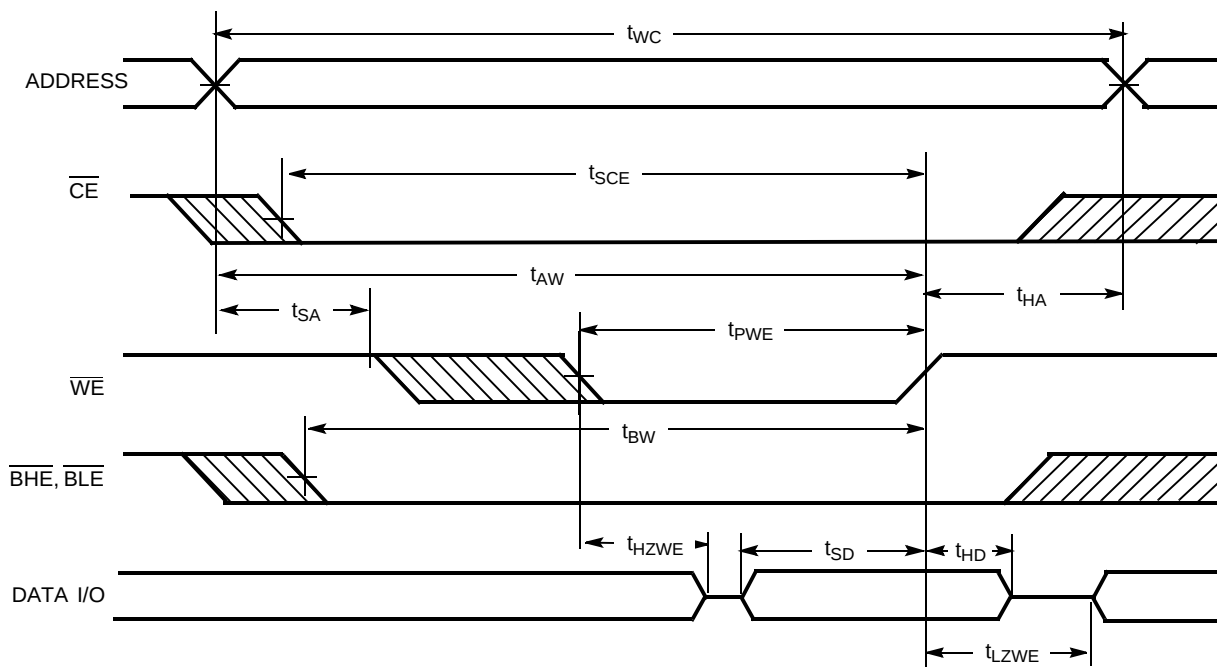
**Data Retention Waveform**

**Switching Waveforms**
**Read Cycle No. 1**<sup>[10, 11]</sup>

**Notes:**

10. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{BHE}$  and/or  $\overline{BHE}$  =  $V_{IL}$ .

11.  $\overline{WE}$  is HIGH for read cycle.

**Switching Waveforms (continued)**
**Read Cycle No. 2 ( $\overline{OE}$  Controlled)<sup>[11, 12]</sup>**

**Write Cycle No. 1 ( $\overline{CE}$  Controlled)<sup>[13, 14]</sup>**

**Notes:**

12. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
13. Data I/O is high-impedance if  $\overline{OE}$  or  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IH}$ .
14. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.

**Switching Waveforms (continued)**
**Write Cycle No. 2 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled)**

**Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW)**


**Truth Table**

| $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | $\overline{BLE}$ | $\overline{BHE}$ | I/O <sub>0</sub> –I/O <sub>7</sub> | I/O <sub>8</sub> –I/O <sub>15</sub> | Mode                       | Power                      |
|-----------------|-----------------|-----------------|------------------|------------------|------------------------------------|-------------------------------------|----------------------------|----------------------------|
| H               | X               | X               | X                | X                | High-Z                             | High-Z                              | Power-down                 | Standby (I <sub>SB</sub> ) |
| L               | L               | H               | L                | L                | Data Out                           | Data Out                            | Read All Bits              | Active (I <sub>CC</sub> )  |
| L               | L               | H               | L                | H                | Data Out                           | High-Z                              | Read Lower Bits Only       | Active (I <sub>CC</sub> )  |
| L               | L               | H               | H                | L                | High-Z                             | Data Out                            | Read Upper Bits Only       | Active (I <sub>CC</sub> )  |
| L               | X               | L               | L                | L                | Data In                            | Data In                             | Write All Bits             | Active (I <sub>CC</sub> )  |
| L               | X               | L               | L                | H                | Data In                            | High-Z                              | Write Lower Bits Only      | Active (I <sub>CC</sub> )  |
| L               | X               | L               | H                | L                | High-Z                             | Data In                             | Write Upper Bits Only      | Active (I <sub>CC</sub> )  |
| L               | H               | H               | X                | X                | High-Z                             | High-Z                              | Selected, Outputs Disabled | Active (I <sub>CC</sub> )  |

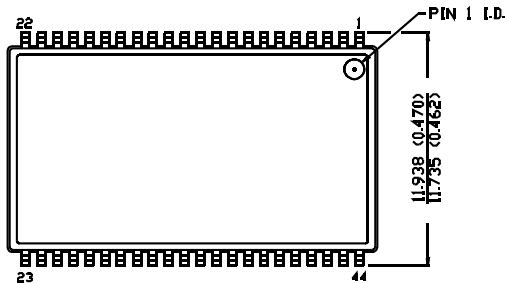
**Ordering Information**

| Speed (ns) | Ordering Code      | Package Name | Package Type             | Operating Range |
|------------|--------------------|--------------|--------------------------|-----------------|
| 10         | CY7C1011CV33-10ZC  | Z44          | 44-pin TSOP II           | Commercial      |
|            | CY7C1011CV33-10ZXC | Z44          | 44-pin TSOP II (Pb-Free) | Commercial      |
|            | CY7C1011CV33-10ZXI | Z44          | 44-pin TSOP II (Pb-Free) | Industrial      |
|            | CY7C1011CV33-10ZI  | Z44          | 44-pin TSOP II           | Industrial      |
|            | CY7C1011CV33-10BVC | BV48A        | 48-ball VFBGA            | Commercial      |
|            | CY7C1011CV33-10BVI | BV48A        | 48-ball VFBGA            | Industrial      |
| 12         | CY7C1011CV33-12ZC  | Z44          | 44-pin TSOP II           | Commercial      |
|            | CY7C1011CV33-12ZXC | Z44          | 44-pin TSOP II (Pb-Free) | Commercial      |
|            | CY7C1011CV33-12ZI  | Z44          | 44-pin TSOP II           | Industrial      |
|            | CY7C1011CV33-12ZXI | Z44          | 44-pin TSOP II (Pb-Free) | Industrial      |
|            | CY7C1011CV33-12AC  | A44          | 44-pin TQFP              | Commercial      |
|            | CY7C1011CV33-12AI  | A44          | 44-pin TQFP              | Industrial      |
|            | CY7C1011CV33-12AXI | A44          | 44-pin TQFP (Pb-Free)    | Industrial      |
|            | CY7C1011CV33-12BVC | BV48A        | 48-ball VFBGA            | Commercial      |
|            | CY7C1011CV33-12BVI | BV48A        | 48-ball VFBGA            | Industrial      |
| 15         | CY7C1011CV33-15ZC  | Z44          | 44-pin TSOP II           | Commercial      |
|            | CY7C1011CV33-15ZI  | Z44          | 44-pin TSOP II           | Industrial      |
|            | CY7C1011CV33-15ZXC | Z44          | 44-pin TSOP II (Pb-Free) | Commercial      |
|            | CY7C1011CV33-15AC  | A44          | 44-pin TQFP              | Commercial      |
|            | CY7C1011CV33-15AI  | A44          | 44-pin TQFP              | Industrial      |
|            | CY7C1011CV33-15AXI | A44          | 44-pin TQFP (Pb-Free)    | Industrial      |
|            | CY7C1011CV33-15BVC | BV48A        | 48-ball VFBGA            | Commercial      |
|            | CY7C1011CV33-15BVI | BV48A        | 48-ball VFBGA            | Industrial      |

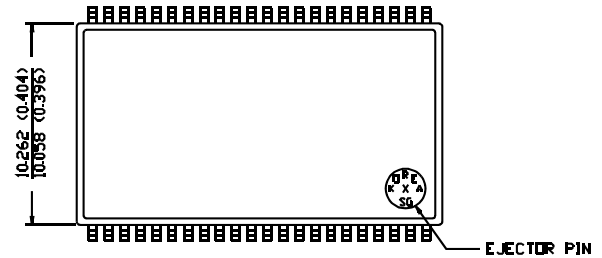
Package Diagrams

44-Pin TSOP II Z44

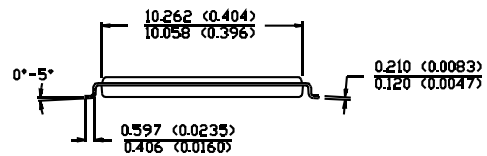
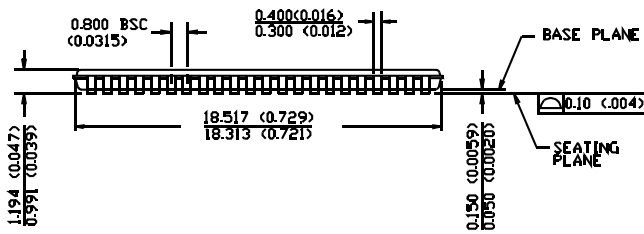
DIMENSION IN MM (INCH)  
MAX  
MIN



TOP VIEW



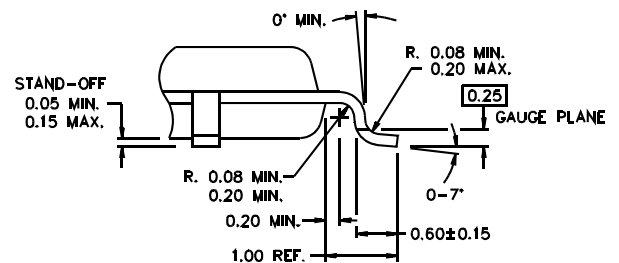
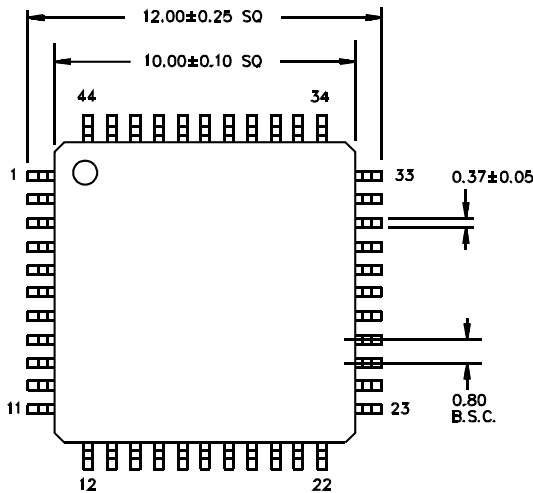
BOTTOM VIEW



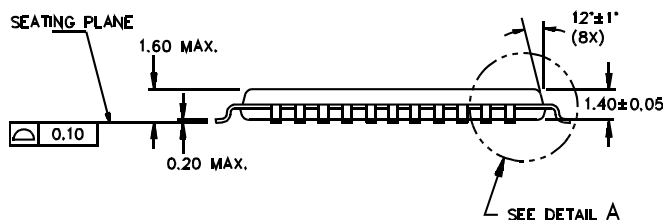
51-85087-A

44-Lead Thin Plastic Quad Flat Pack A44

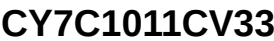
DIMENSIONS ARE IN MILLIMETERS



DETAIL A



51-85064-B



### 48-Lead VFBGA (6 x 8 x 1 mm) BV48A

BOTTOM VIEW



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## Document History Page

| Document Title: CY7C1011CV33 128K x 16 Static RAM<br>Document Number: 38-05232 |         |            |                 |                                                                                                                                                                         |
|--------------------------------------------------------------------------------|---------|------------|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| REV.                                                                           | ECN NO. | Issue Date | Orig. of Change | Description of Change                                                                                                                                                   |
| **                                                                             | 117132  | 07/31/02   | HGK             | New Data Sheet                                                                                                                                                          |
| *A                                                                             | 118057  | 08/19/02   | HGK             | Pin configuration for 48-ball FBGA correction                                                                                                                           |
| *B                                                                             | 119702  | 10/11/02   | DFP             | Updated FBGA to VFBGA; updated package code on page 8 to BV48A. Updated address pinouts on page 1 to A0 to A16. Updated CMOS standby current on page 1 from 8 to 10 mA. |
| *C                                                                             | 386106  | See ECN    | PCI             | Added lead-free parts in Ordering Information Table                                                                                                                     |