



CYPRESS

CY7C199

32K x 8 Static RAM

Features

- High speed
— 12 ns
- Fast t_{DOE}
- CMOS for optimum speed/power
- Low active power
— 880 mW
- Low standby power
— 165 mW
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- TTL-compatible inputs and outputs
- Automatic power-down when deselected

Functional Description

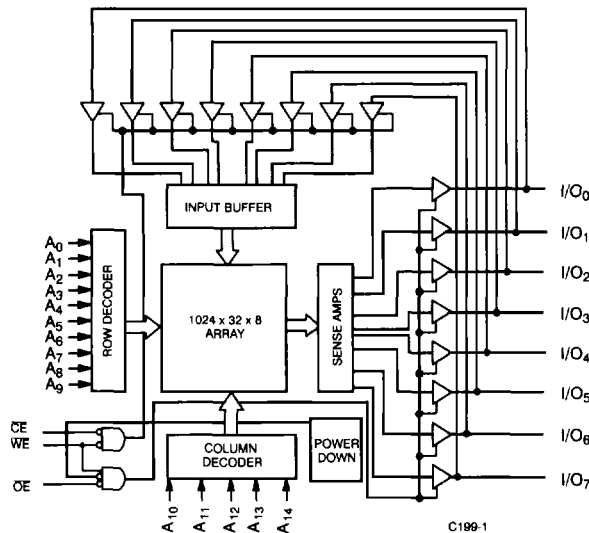
The CY7C199 is a high-performance CMOS static RAM organized as 32,768 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and active LOW output enable ($\overline{OE}$) and three-state drivers. This device has an automatic power-down feature, reducing the power consumption by 81% when deselected. The CY7C199 is in the standard 300-mil-wide DIP, SOJ, and LCC packages.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE}$ and $\overline{WE}$ inputs are both LOW, data on the eight data input/

output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{14}). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE}$ and $\overline{OE}$ active LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

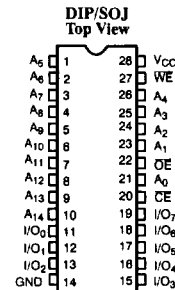
The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH. A die coat is used to ensure alpha immunity.

Logic Block Diagram

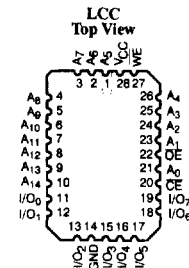


C199-1

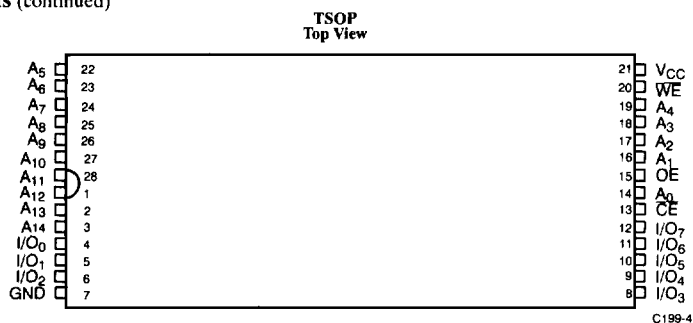
Pin Configurations



C199-2



C199-3

Pin Configurations (continued)

Selection Guide

		7C199-10	7C199-12	7C199-15	7C199-20	7C199-25	7C199-35	7C199-45
Maximum Access Time (ns)		10	12	15	20	25	35	45
Maximum Operating Current (mA)	Com'l	160	160	155	150	150	140	
	L		130	110	100	100	100	100
	Mil			180	170	150	150	150
	L			150	130	130	130	130
Maximum Standby Current (mA)		30	30	30	30	30	25	25
	L		20	20	15	15	15	15

Shaded area contains preliminary information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with

Power Applied -55°C to +125°C

Supply Voltage to Ground Potential

(Pin 28 to Pin 14) -0.5V to +7.0V

DC Voltage Applied to Outputs

in High Z State^[1] -0.5V to V_{CC} + 0.5V

DC Input Voltage^[1] -0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Military ^[2]	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range^[3]

Parameter	Description	Test Conditions	7C199-10		7C199-12		7C199-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC} + 0.3V	2.2	V _{CC} + 0.3V	2.2	V _{CC} + 0.3V	V
V _{IL}	Input LOW Voltage		-0.5	0.8	-0.5	0.8	-0.5	0.8	V
I _{Ix}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-5	+5	-5	+5	-5	+5	μA

Shaded area contains preliminary information.

Notes:

1. V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.

2. T_A is the "instant on" case temperature.

3. See the last page of this specification for Group A subgroup testing information.

Electrical Characteristics Over the Operating Range^[3] (continued)

Parameter	Description	Test Conditions	7C199-10		7C199-12		7C199-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-5	+5	-5	+5	-5	+5	μA
I _{OS}	Output Short Circuit Current ^[4]	V _{CC} = Max., V _{OUT} = GND		-300		-300		-300	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}	Com'l	160		160		155	mA
			L			130		110	
			Mil					180	
			L					150	
I _{SB1}	Automatic CE Power-Down Current—TTL Inputs	Max. V _{CC} , CE ≥ V _{IH} , V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}		30		30		30	mA
			L			20		20	mA
I _{SB2}	Automatic CE Power-Down Current—CMOS Inputs	Max. V _{CC} , CE ≥ V _{CC} - 0.3V V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V, f = 0	Com'l	10		10		10	mA
			L			500		500	μA
			Mil					15	mA
			L					5	

Shaded area contains preliminary information.

Electrical Characteristics Over the Operating Range^[3] (continued)

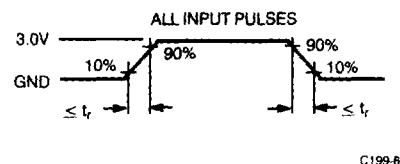
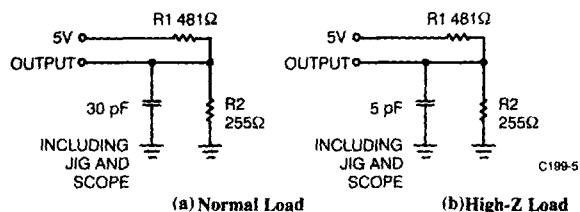
Parameter	Description	Test Conditions	7C199-20		7C199-25		7C199-35, 45		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC} + 0.3V	2.2	V _{CC} + 0.3V	2.2	V _{CC} + 0.3V	V
V _{IL}	Input LOW Voltage		-0.5	0.8	-3.0	0.8	-3.0	0.8	V
I _{Ix}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-5	+5	-5	+5	-5	+5	μA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	-5	+5	-5	+5	-5	+5	μA
I _{OS}	Output Short Circuit Current ^[4]	V _{CC} = Max., V _{OUT} = GND		-300		-300		-300	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}	Com'l	150		150		140	mA
			L	100		100		100	
			Mil	170		150		150	
			L	130		130		130	
I _{SB1}	Automatic CE Power-Down Current—TTL Inputs	Max. V _{CC} , CE ≥ V _{IH} , V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}		30		30		25	mA
			L	15		15		15	
I _{SB2}	Automatic CE Power-Down Current—CMOS Inputs	Max. V _{CC} , CE ≥ V _{CC} - 0.3V V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V, f = 0	Com'l	15		15		15	mA
			L	500		500		500	μA
			Mil	15		15		15	mA
			L	5		5		5	

Note:

4. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.

Capacitance^[5]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = 5.0\text{V}$	8	pF
C_{OUT}	Output Capacitance		8	pF

AC Test Loads and Waveforms^[6]


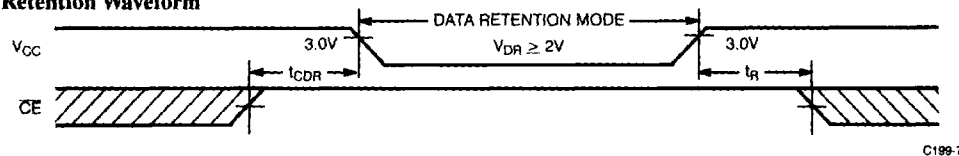
Equivalent to: THÉVENIN EQUIVALENT

167Ω

OUTPUT ——— 1.73V

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions ^[7]	Min.	Max.	Unit
V_{DR}	V_{CC} for Data Retention		2.0		V
I_{CCDR}	Data Retention Current	Com'l		10	μA
		Mil		100	
$t_{CDR}^{[5]}$	Chip Deselect to Data Retention Time	$V_{CC} = V_{DR} = 2.0\text{V}$, $\overline{CE} \geq V_{CC} - 0.3\text{V}$, $V_{IN} \geq V_{CC} - 0.3\text{V}$ or $V_{IN} \leq 0.3\text{V}$	0		ns
$t_R^{[5]}$	Operation Recovery Time		t_{RC}		ns

Data Retention Waveform

Notes:

- Tested initially and after any design or process changes that may affect these parameters.
- $t_r \leq 3\text{ ns}$ for the -12 and -15 speeds. $t_r \leq 5\text{ ns}$ for the -20 and slower speeds.
- No input may exceed $V_{CC} + 0.5\text{V}$.



Switching Characteristics Over the Operating Range^[3, 8]

Parameter	Description	7C199-10		7C199-12		7C199-15		7C199-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t _{RC}	Read Cycle Time	10		12		15		20		ns
t _{AA}	Address to Data Valid		10		12		15		20	ns
t _{OHA}	Data Hold from Address Change	3		3		3		3		ns
t _{ACE}	CE LOW to Data Valid		10		12		15		20	ns
t _{DOE}	OE LOW to Data Valid		5		5		7		9	ns
t _{LZOE}	OE LOW to Low Z ^[9]	0		0		0		0		ns
t _{HZOE}	OE HIGH to High Z ^[9, 10]		5		5		7		9	ns
t _{LZCE}	CE LOW to Low Z ^[9]	3		3		3		3		ns
t _{HZCE}	CE HIGH to High Z ^[9, 10]		5		5		7		9	ns
t _{PU}	CE LOW to Power-Up	0		0		0		0		ns
t _{PD}	CE HIGH to Power-Down		10		12		15		20	ns
WRITE CYCLE ^[11, 12]										
t _{WC}	Write Cycle Time	10		12		15		20		ns
t _{SCE}	CE LOW to Write End	7		9		10		15		ns
t _{AW}	Address Set-Up to Write End	7		9		10		15		ns
t _{HA}	Address Hold from Write End	0		0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		0		ns
t _{PWE}	WE Pulse Width	7		8		9		15		ns
t _{SD}	Data Set-Up to Write End	5		8		9		10		ns
t _{HD}	Data Hold from Write End	0		0		0		0		ns
t _{HZWE}	WE LOW to High Z ^[10]		5		7		7		10	ns
t _{LZWE}	WE HIGH to Low Z ^[9]	3		3		3		3		ns

Shaded area contains preliminary information.

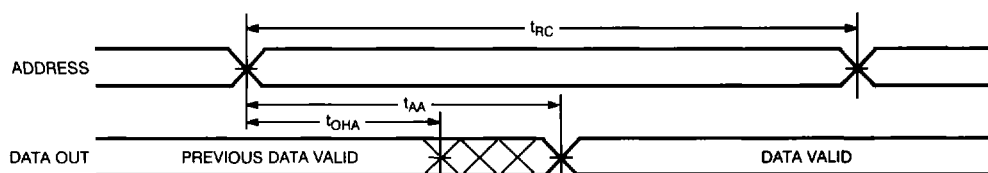
Notes:

8. Test conditions assume signal transition time of 3 ns or less for -12 and -15 speeds and 5 ns or less for -20 and slower speeds, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
9. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
10. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
11. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
12. The minimum write cycle time for write cycle #3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Characteristics Over the Operating Range^[3, 8] (continued)

Parameter	Description	7C199-25		7C199-35		7C199-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t _{RC}	Read Cycle Time	25		35		45		ns
t _{AA}	Address to Data Valid		25		35		45	ns
t _{OHA}	Data Hold from Address Change	3		3		3		ns
t _{ACE}	$\overline{CE}$ LOW to Data Valid		25		35		45	ns
t _{DOE}	$\overline{OE}$ LOW to Data Valid		10		16		16	ns
t _{LZOE}	$\overline{OE}$ LOW to Low Z ^[9]	3		3		3		ns
t _{HZOE}	$\overline{OE}$ HIGH to High Z ^[9, 10]		11		15		15	ns
t _{LZCE}	$\overline{CE}$ LOW to Low Z ^[9]	3		3		3		ns
t _{HZCE}	$\overline{CE}$ HIGH to High Z ^[9, 10]		11		15		15	ns
t _{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t _{PD}	$\overline{CE}$ HIGH to Power-Down		20		20		25	ns
WRITE CYCLE ^[11, 12]								
t _{WC}	Write Cycle Time	25		35		45		ns
t _{SCE}	$\overline{CE}$ LOW to Write End	18		22		22		ns
t _{AW}	Address Set-Up to Write End	20		30		40		ns
t _{HA}	Address Hold from Write End	0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		ns
t _{PWE}	$\overline{WE}$ Pulse Width	18		22		22		ns
t _{SD}	Data Set-Up to Write End	10		15		15		ns
t _{HD}	Data Hold from Write End	0		0		0		ns
t _{HZWE}	$\overline{WE}$ LOW to High Z ^[10]		11		15		15	ns
t _{LZWE}	$\overline{WE}$ HIGH to Low Z ^[9]	3		3		3		ns

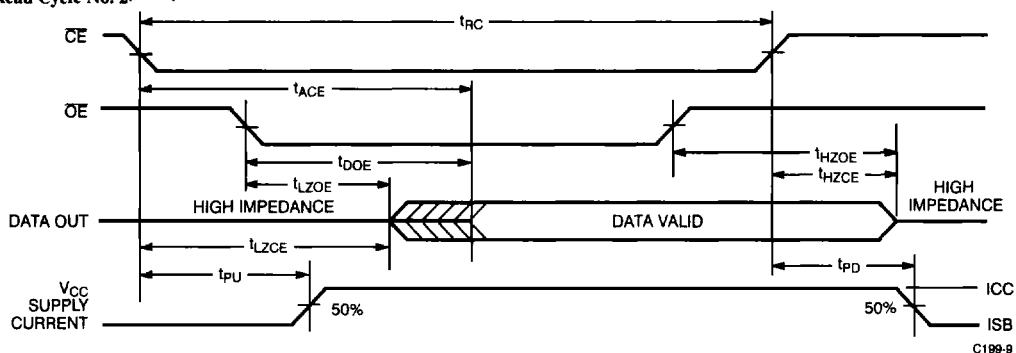
Switching Waveforms

Read Cycle No. 1^[13, 14]

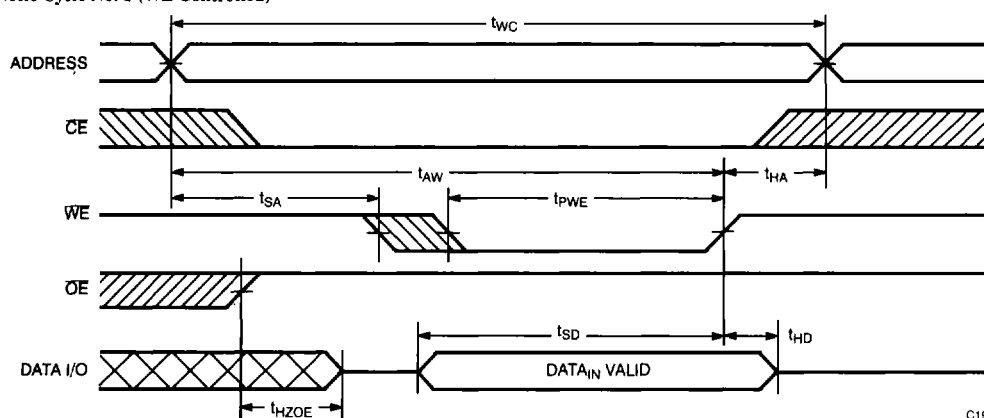
C199-8

Notes:

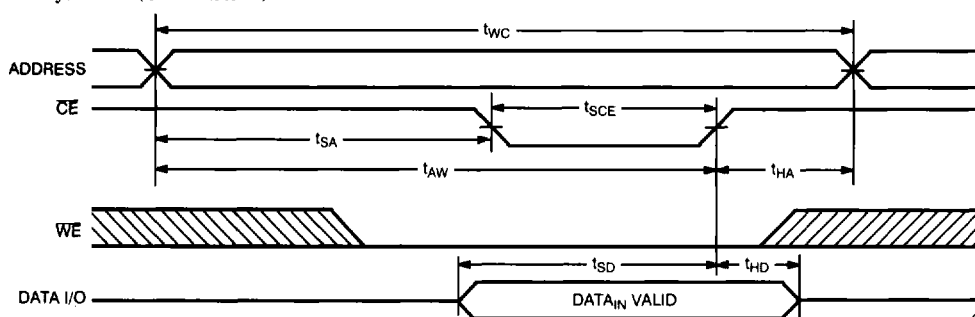
13. Device is continuously selected. $\overline{OE}$, $\overline{CE} = V_{IL}$.14. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)
Read Cycle No. 2^[14, 15]


C199-9

Write Cycle No. 1 (WE Controlled)^[11, 16, 17]


C199-10

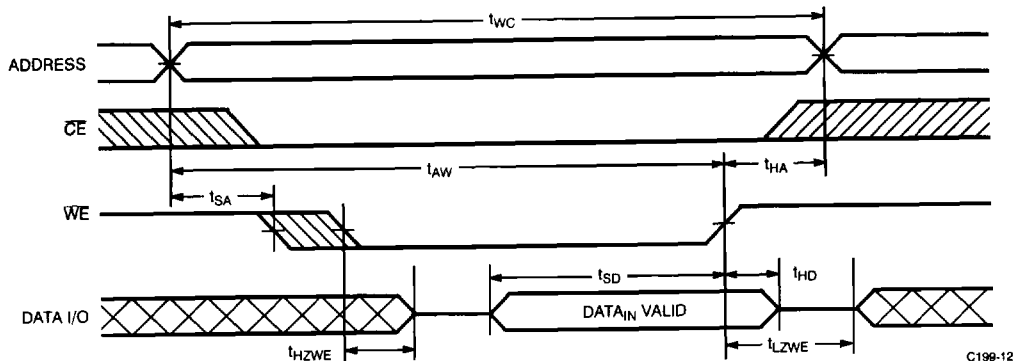
Write Cycle No. 2 (CE Controlled)^[11, 16, 17]


C199-11

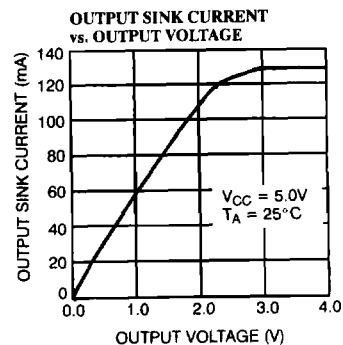
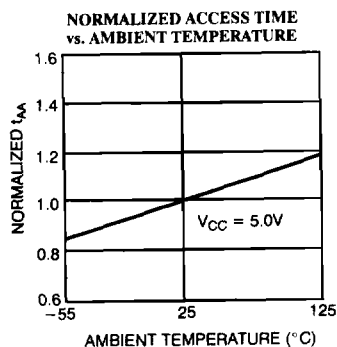
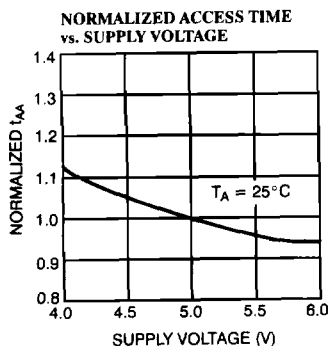
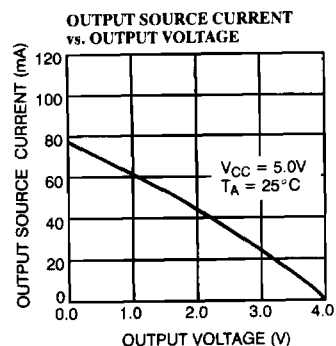
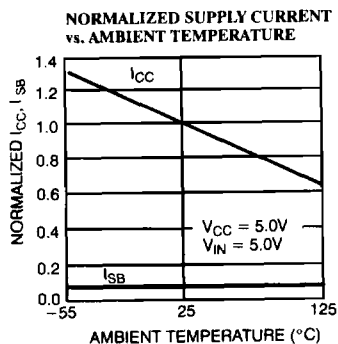
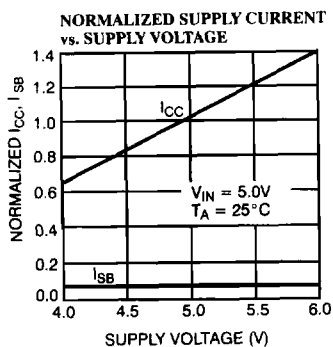
Notes:

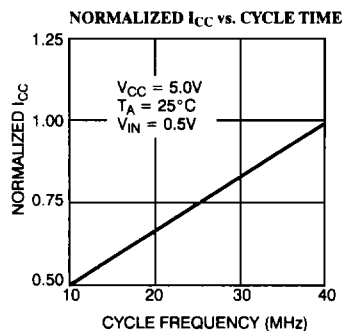
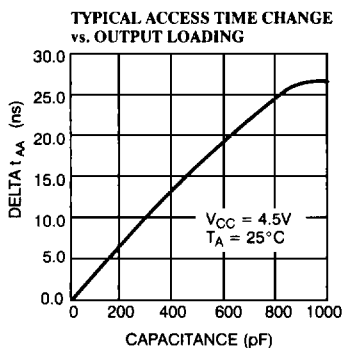
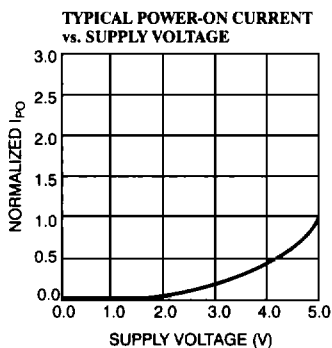
15. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
 16. Data I/O is high impedance if $\overline{OE} = V_{IH}$.

17. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)
Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)^[12, 17]


C199-12

Typical DC and AC Characteristics


Typical DC and AC Characteristics (continued)

Truth Table

CE	WE	OE	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Deselect, Output Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C199-10VC	V21	28-Lead Molded SOJ	Commercial
12	CY7C199-12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199L-12PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C199-12VC	V21	28-Lead Molded SOJ	
	CY7C199L-12VC	V21	28-Lead Molded SOJ	
	CY7C199-12ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199L-12ZC	Z28	28-Lead Thin Small Outline Package	
15	CY7C199-15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199L-15PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C199-15VC	V21	28-Lead Molded SOJ	
	CY7C199L-15VC	V21	28-Lead Molded SOJ	
	CY7C199-15ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199L-15ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199-15DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C199L-15DMB	D22	28-Lead (300-Mil) CerDIP	
	CY7C199-15LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
	CY7C199L-15LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
20	CY7C199-20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199L-20PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C199-20VC	V21	28-Lead Molded SOJ	
	CY7C199L-20VC	V21	28-Lead Molded SOJ	
	CY7C199-20ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199L-20ZC	Z28	28-Lead Thin Small Outline Package	



Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7C199-20DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C199L-20DMB	D22	28-Lead (300-Mil) CerDIP	
	CY7C199-20LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
	CY7C199L-20LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
25	CY7C199-25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199L-25PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C199-25VC	V21	28-Lead Molded SOJ	
	CY7C199L-25VC	V21	28-Lead Molded SOJ	
	CY7C199-25ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199L-25ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199-25DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C199L-25DMB	D22	28-Lead (300-Mil) CerDIP	
	CY7C199-25LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
	CY7C199L-25LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
35	CY7C199-35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C199L-35PC	P21	28-Lead (300-Mil) Molded DIP	
	CY7C199-35VC	V21	28-Lead Molded SOJ	
	CY7C199L-35VC	V21	28-Lead Molded SOJ	
	CY7C199-35ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199L-35ZC	Z28	28-Lead Thin Small Outline Package	
	CY7C199-35DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C199L-35DMB	D22	28-Lead (300-Mil) CerDIP	
	CY7C199-35LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
	CY7C199L-35LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
45	CY7C199-45DMB	D22	28-Lead (300-Mil) CerDIP	Military
	CY7C199L-45DMB	D22	28-Lead (300-Mil) CerDIP	
	CY7C199-45LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
	CY7C199L-45LMB	L54	28-Pin Rectangular Leadless Chip Carrier	

Shaded area contains preliminary information.

MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL} Max.	1, 2, 3
I _{Ix}	1, 2, 3
I _{OZ}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB1}	1, 2, 3
I _{SB2}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t _{RC}	7, 8, 9, 10, 11
t _{AA}	7, 8, 9, 10, 11
t _{OHA}	7, 8, 9, 10, 11
t _{ACE}	7, 8, 9, 10, 11
t _{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t _{WC}	7, 8, 9, 10, 11
t _{SCE}	7, 8, 9, 10, 11
t _{AW}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{SA}	7, 8, 9, 10, 11
t _{PWE}	7, 8, 9, 10, 11
t _{SD}	7, 8, 9, 10, 11
t _{HD}	7, 8, 9, 10, 11

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