COMPLEMENTARY PAIR ENHANCEMENT MODE MOSFET
PowerDI5060-8

Product Summary

Device	$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D T_A = +25°C
Q1	12V	17mΩ @ V_{GS} = 4.5V	9.5A
		25mΩ @ V_{GS} = 2.5V	7.8A
Q2	-20V	32mΩ @ V_{GS} = -4.5V	-6.9A
		53mΩ @ V_{GS} = -2.5V	-5.4A

Description and Applications

This new generation Complementary Pair Enhancement Mode MOSFET has been designed to minimize $R_{DS(ON)}$ and yet maintain superior switching performance. This device is ideal for use in Notebook battery power management and Loadswitch.

- Notebook Battery Power Management
- DC-DC Converters
- Loadswitch

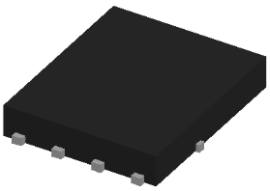
Features and Benefits

- Thermally Efficient Package-Cooler Running Applications
- High Conversion Efficiency
- Low $R_{DS(ON)}$ – Minimizes On State Losses
- Low Input Capacitance
- Fast Switching Speed
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e.: parts qualified to AEC-Q101, PPAP capable, and manufactured in IATF 16949 certified facilities), please refer to the related automotive grade (Q-suffix) part. A listing can be found at https://www.diodes.com/products/automotive/automotive-products/.**
- **This part is qualified to JEDEC standards (as references in AEC-Q101) for High Reliability. https://www.diodes.com/quality/product-definitions/**

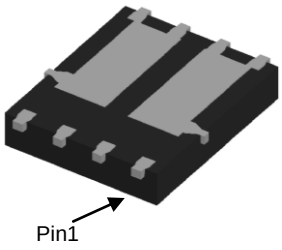
Mechanical Data

- Case: PowerDI®5060-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – 100% Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 e3
- Terminal Connections: See Diagram Below
- Weight: 0.097 grams (Approximate)

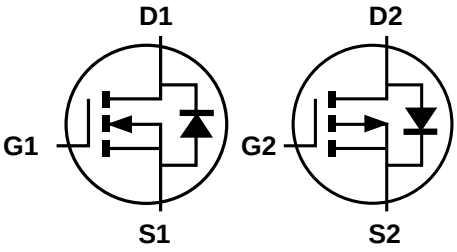
PowerDI5060-8 (Type C)



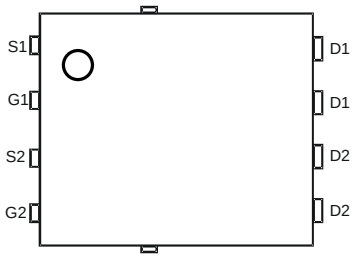
Top View



Bottom View



Q1 N-Channel MOSFET Q2 P-Channel MOSFET



Top View
Pin Configuration

Ordering Information (Note 4)

Part Number	Case	Packaging
DMC1018UPD-13	PowerDI5060-8 (Type C)	2500 / Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

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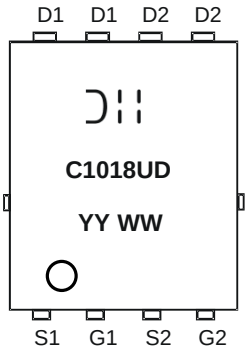
Marking Information



= Manufacturer's Marking
C1018UD = Product Type Marking Code
YYWW = Date Code Marking
YY = Year (ex: 15 = 2015)
WW = Week (01 - 53)

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Q1 Value	Q2 Value	Units
Drain-Source Voltage			V_{DSS}	12	-20	V
Gate-Source Voltage			V_{GSS}	±8	±12	V
Continuous Drain Current (Note 5) V_{GS} = 4.5V	Steady State	T_A = +25°C T_A = +70°C	I_D	9.5 7.6	-6.9 -5.5	A
	t<10s	T_A = +25°C T_A = +70°C	I_D	13.0 10.4	-9.4 -7.5	A
Maximum Body Diode Forward Current (Note 5)			I_S	2.5	-2.5	A
Pulsed Drain Current (10µs pulse, duty cycle = 1%)			I_{DM}	60	-40	A
Avalanche Current (Note 6) L = 0.1mH			I_{AS}	20	-17	A
Avalanche Energy (Note 6) L = 0.1mH			E_{AS}	25	14	mJ

Thermal Characteristics

Characteristic		Symbol	Value	Units
Total Power Dissipation (Note 5)	T_A = +25°C	P_D	2.3	W
	T_A = +70°C		1.5	
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	54	°C/W
	t<10s		29	
Thermal Resistance, Junction to Case		$R_{\theta JC}$	6.5	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Notes: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
6. I_{AS} and E_{AS} rating are based on low frequency and duty cycles to keep T_J = +25°C.

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Electrical Characteristics Q1 N-Channel (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	12	—	—	V	V_{GS} = 0V, I_D = 250µA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	µA	V_{DS} = 12V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±8V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	0.6	0.8	1.5	V	V_{DS} = V_{GS}, I_D = 250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	8	17	mΩ	V_{GS} = 4.5V, I_D = 11.8A
		—	11	25		V_{GS} = 2.5V, I_D = 9.8A
Diode Forward Voltage	V_{SD}	—	0.7	1.2	V	V_{GS} = 0V, I_S = 2.9A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	1525	—	pF	V_{DS} = 6V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	—	329	—		
Reverse Transfer Capacitance	C_{rss}	—	303	—		
Gate Resistance	R_G	—	1.6	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz
Total Gate Charge (V_{GS} = 4.5V)	Q_g	—	17.1	—	nC	V_{DS} = 6V, I_D = 11.8A
Total Gate Charge (V_{GS} = 8V)	Q_g	—	30.4	—		
Gate-Source Charge	Q_{gs}	—	2.6	—		
Gate-Drain Charge	Q_{gd}	—	4.3	—		
Turn-On Delay Time	$t_{D(ON)}$	—	6.6	—	ns	V_{DD} = 6V, R_L = 6Ω, V_{GS} = 4.5V, R_G = 6Ω, I_D = 1A
Turn-On Rise Time	t_R	—	10.8	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	41.5	—		
Turn-Off Fall Time	t_F	—	21.9	—		
Body Diode Reverse Recovery Time	t_{RR}	—	14.3	—	ns	I_F = 11.8A, di/dt = 100A/µs
Body Diode Reverse Recovery Charge	Q_{RR}	—	2.3	—	nC	I_F = 11.8A, di/dt = 100A/µs

Notes: 7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.

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Electrical Characteristics Q2 P-Channel (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	-20	—	—	V	V_{GS} = 0V, I_D = -250µA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-1	µA	V_{DS} = -16V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±12V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	-0.6	-0.8	-1.5	V	V_{DS} = V_{GS}, I_D = -250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	22	32	mΩ	V_{GS} = -4.5V, I_D = -8.9A
		—	31	53		V_{GS} = -2.5V, I_D = -6.9A
Diode Forward Voltage	V_{SD}	—	-0.7	-1.2	V	V_{GS} = 0V, I_S = -2.9A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	866	—	pF	V_{DS} = -6V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	—	167	—		
Reverse Transfer Capacitance	C_{rss}	—	131	—		
Gate Resistance	R_G	—	4.9	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz
Total Gate Charge (V_{GS} = -4.5V)	Q_g	—	8.6	—	nC	V_{DS} = -6V, I_D = -8.9A
Total Gate Charge (V_{GS} = -8V)	Q_g	—	19	—		
Gate-Source Charge	Q_{gs}	—	1.5	—		
Gate-Drain Charge	Q_{gd}	—	2.5	—		
Turn-On Delay Time	$t_{D(ON)}$	—	5.8	—	ns	V_{DD} = -6V, R_L = 6Ω, V_{GS} = -4.5V, R_G = 6Ω, I_D = -1A
Turn-On Rise Time	t_R	—	7.7	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	28.1	—		
Turn-Off Fall Time	t_F	—	14.6	—		
Body Diode Reverse Recovery Time	t_{RR}	—	9.8	—	ns	I_F = -8.9A, di/dt = -100A/µs
Body Diode Reverse Recovery Charge	Q_{RR}	—	2.7	—	nC	I_F = -8.9A, di/dt = -100A/µs

Notes: 7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.

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Typical Characteristics - N-CHANNEL

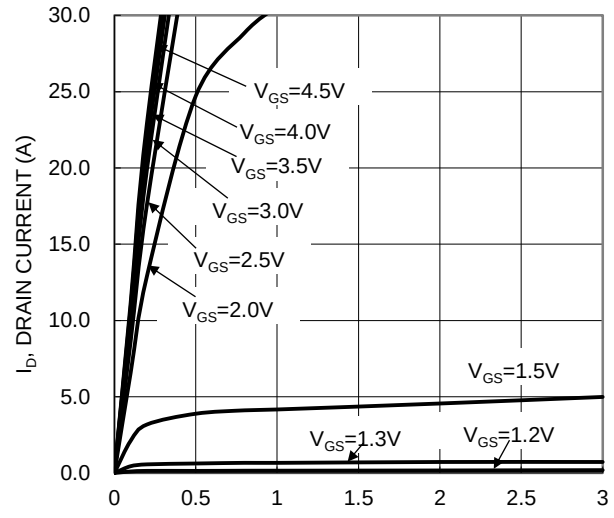

Figure 1. Typical Output Characteristic

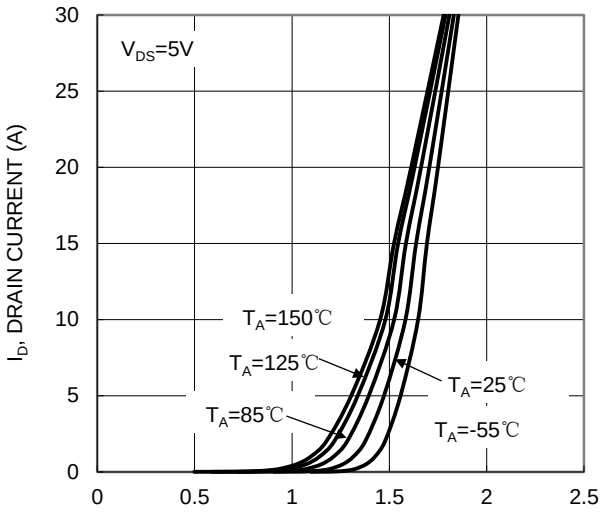

Figure 2. Typical Transfer Characteristic

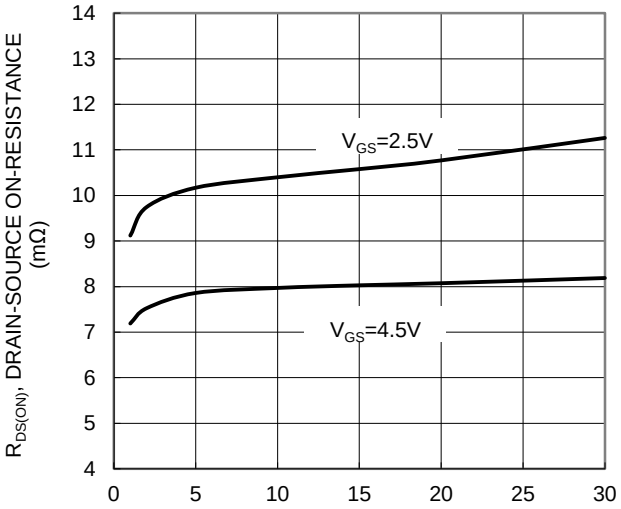

Figure 3. Typical On-Resistance vs Drain Current and Gate Voltage

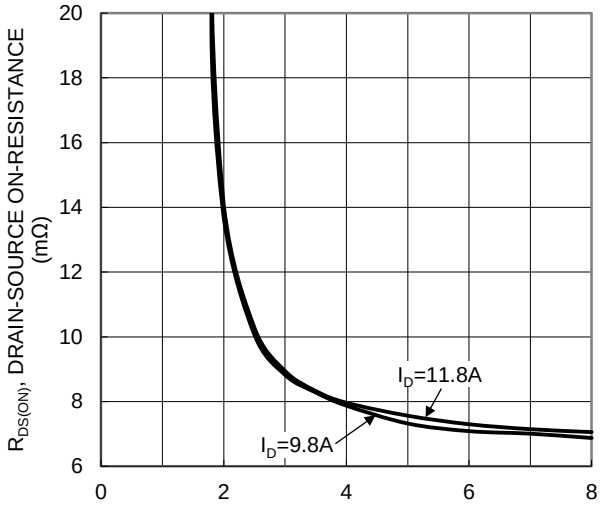

Figure 4. Typical Transfer Characteristic

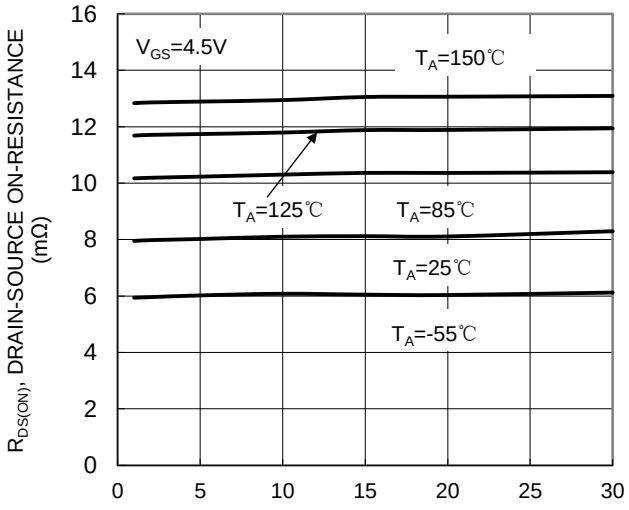

Figure 5. Typical On-Resistance vs Drain Current and Junction Temperature

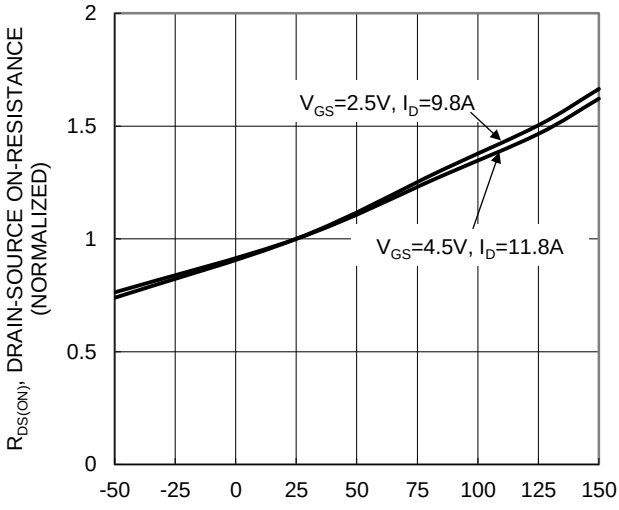

Figure 6. On-Resistance Variation with Junction Temperature

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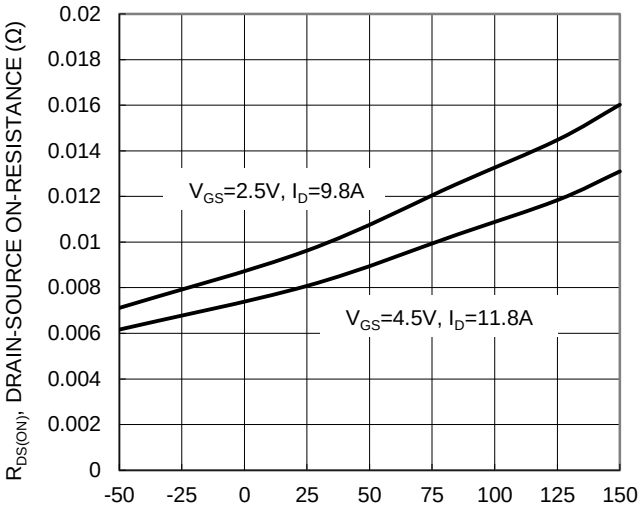

Figure 7. On-Resistance Variation with Junction Temperature

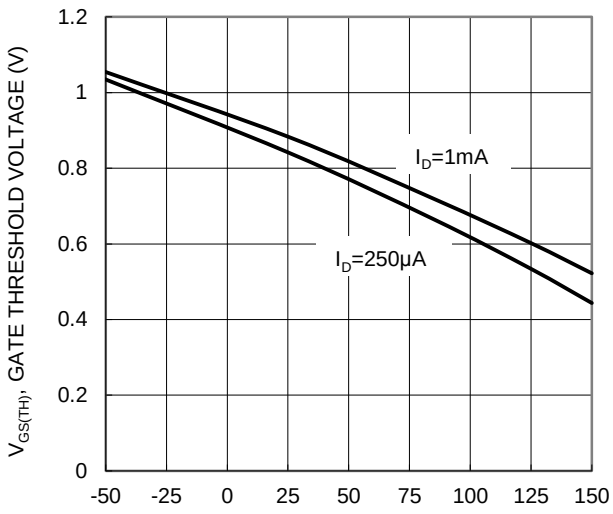

Figure 8. Gate Threshold Variation vs Junction Temperature

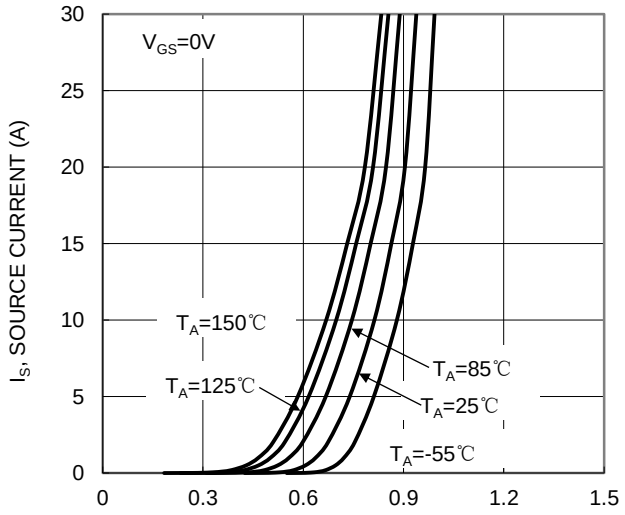

Figure 9. Diode Forward Voltage vs Current

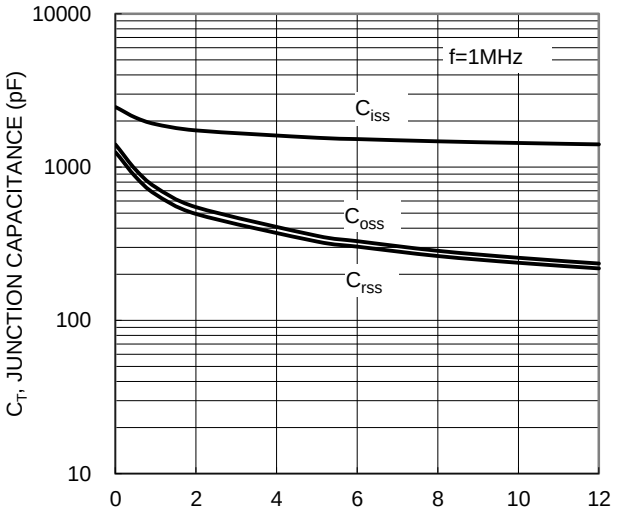

Figure 10. Typical Junction Capacitance

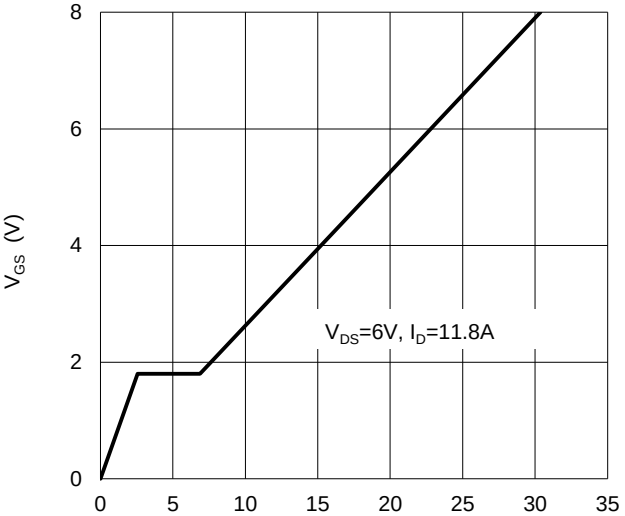

Figure 11. Gate Charge

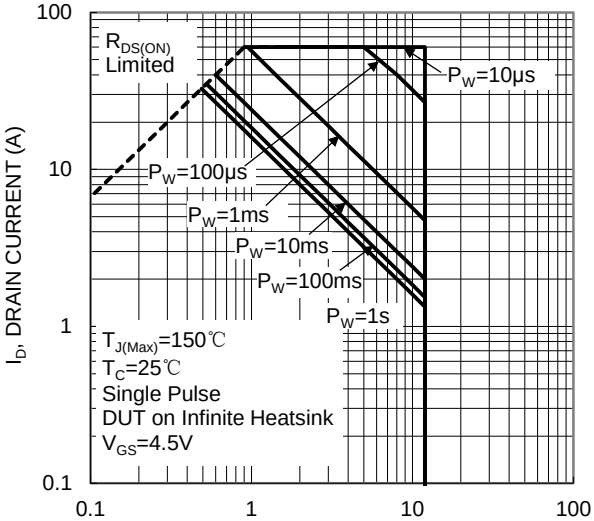

Figure 12. SOA, Safe Operation Area

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Typical Characteristics - P-CHANNEL

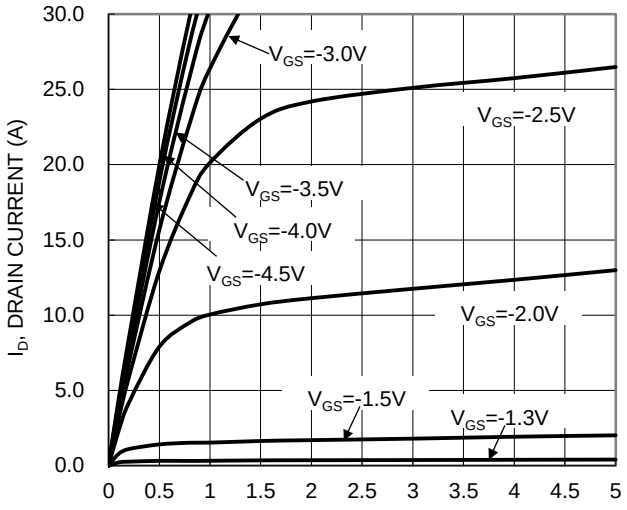

Figure 13. Typical Output Characteristic

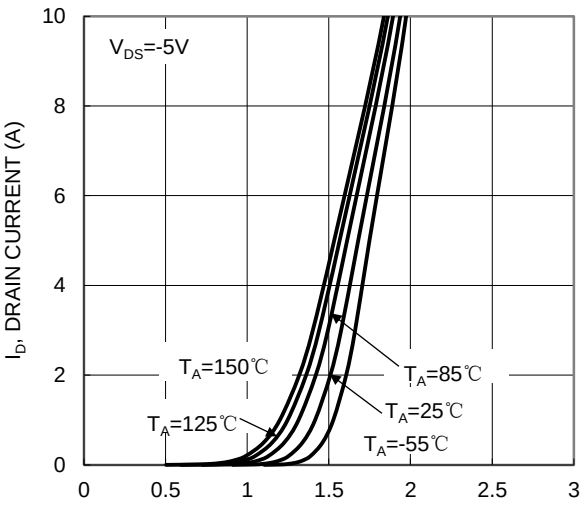

Figure 14. Typical Transfer Characteristic

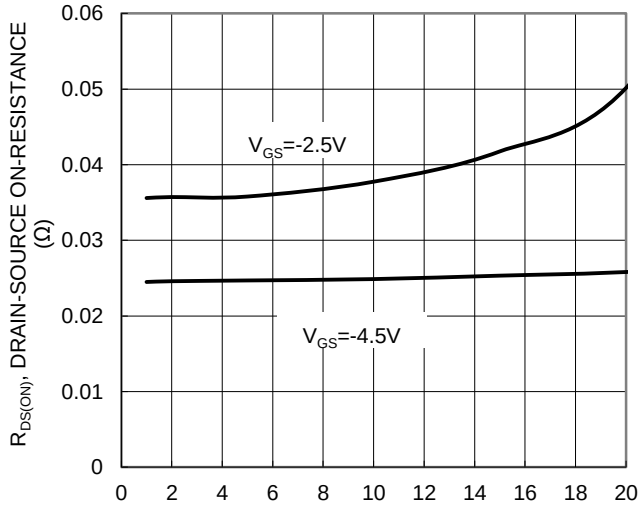

Figure 15. Typical On-Resistance vs Drain Current and Gate Voltage

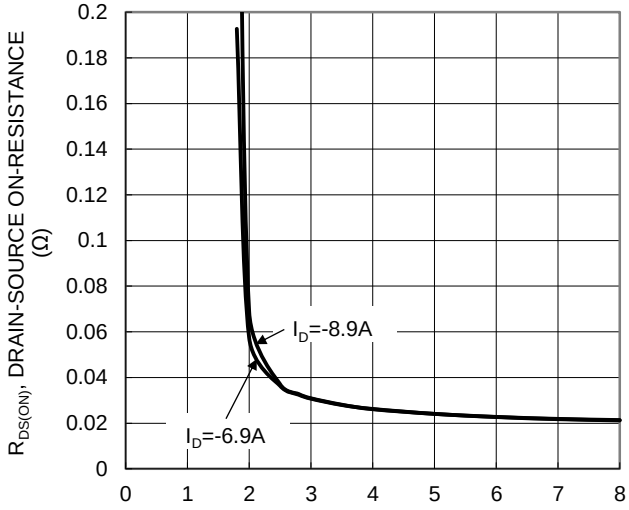

Figure 16. Typical Transfer Characteristic

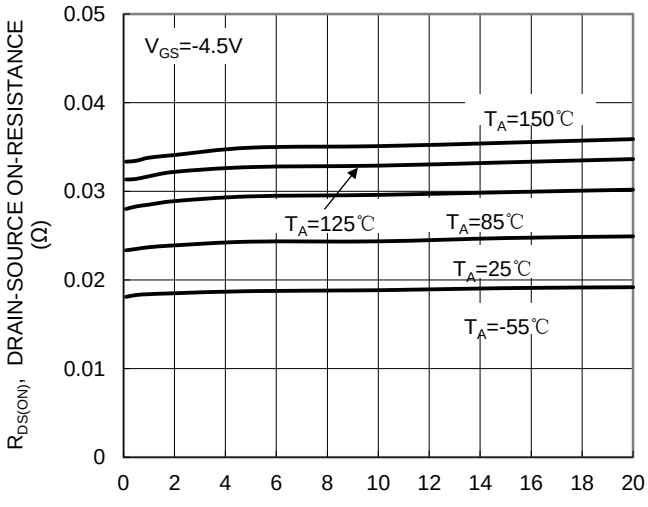

Figure 17. Typical On-Resistance vs Drain Current and Temperature

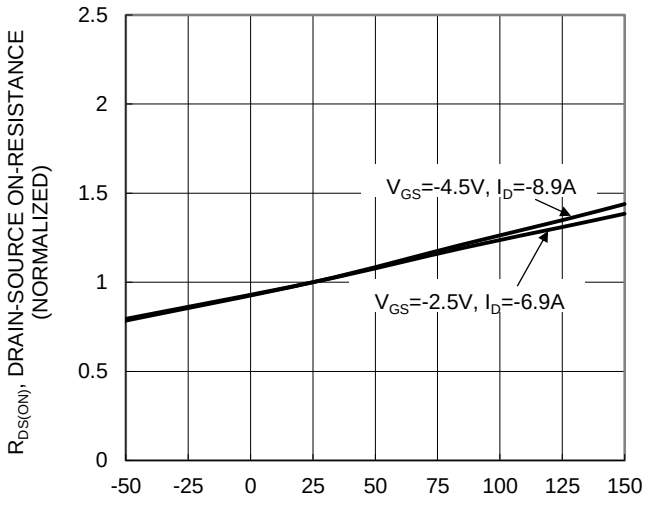

Figure 18. On-Resistance Variation with Temperature

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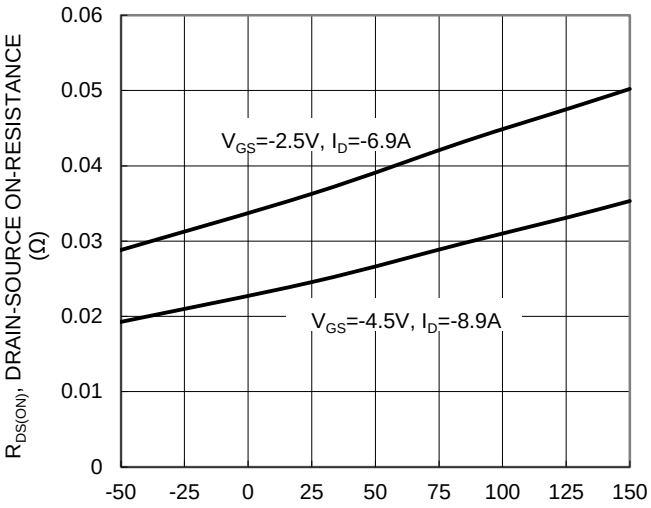

Figure 19. On-Resistance Variation with Temperature

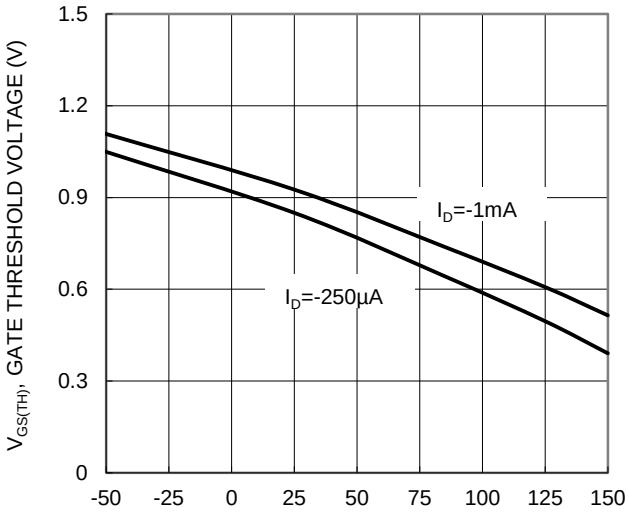

Figure 20. Gate Threshold Variation vs Junction Temperature

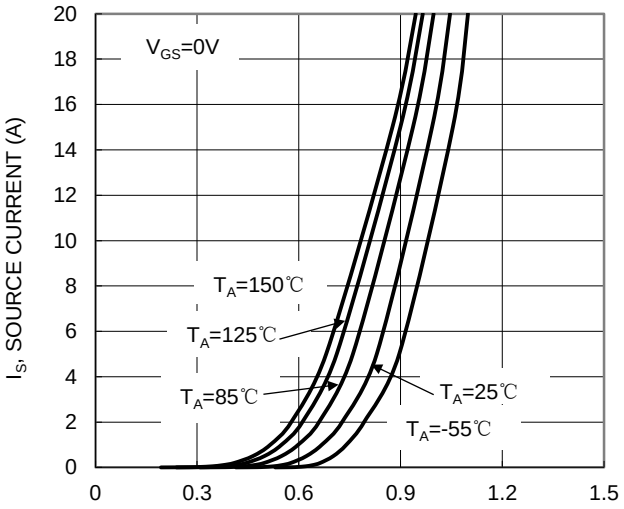

Figure 21. Diode Forward Voltage vs Current

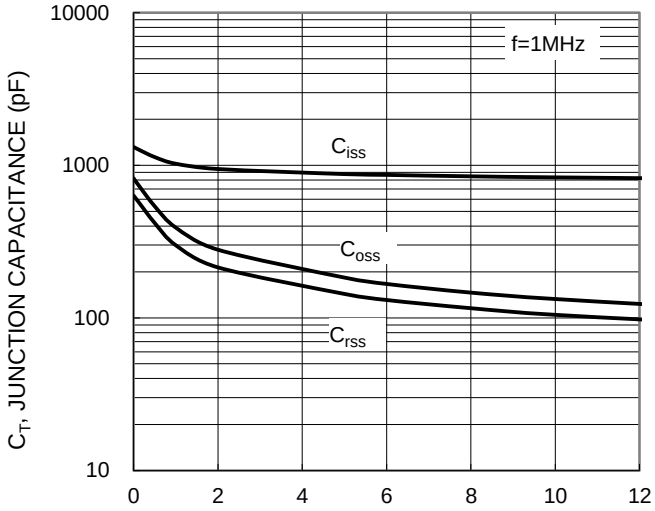

Figure 22. Typical Junction Capacitance

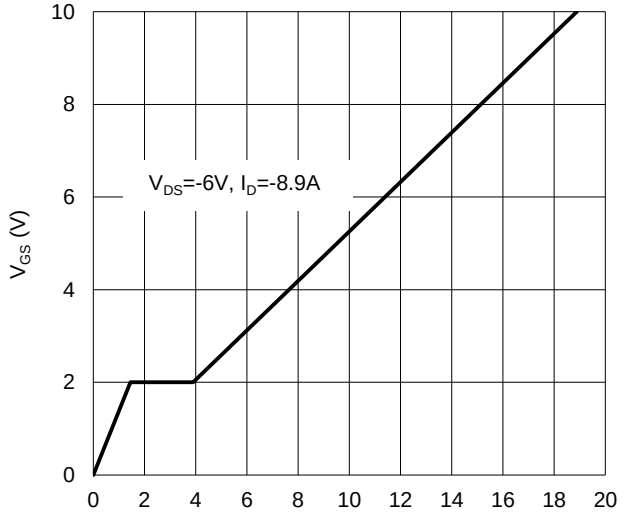

Figure 23. Gate Charge

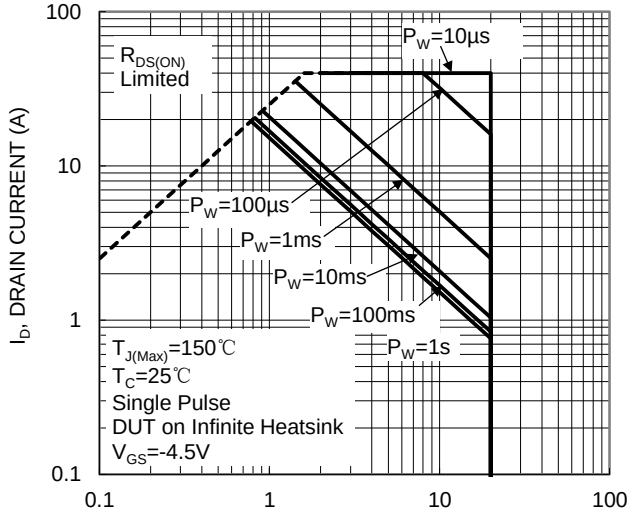

Figure 24. SOA, Safe Operation Area

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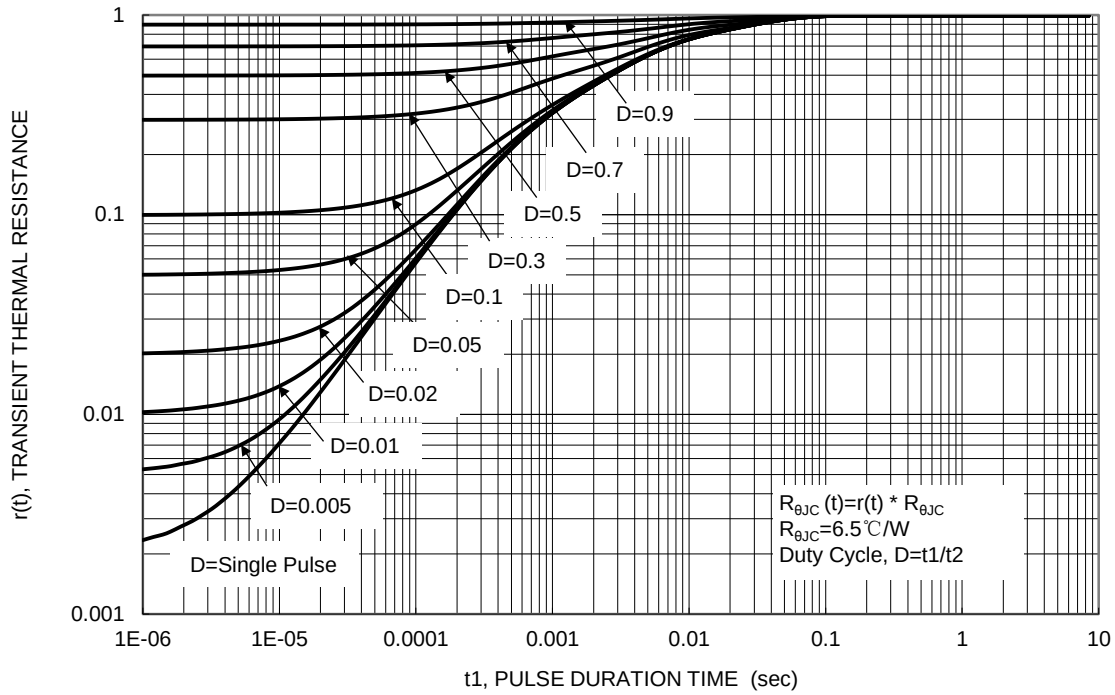

Figure 25. Transient Thermal Resistance

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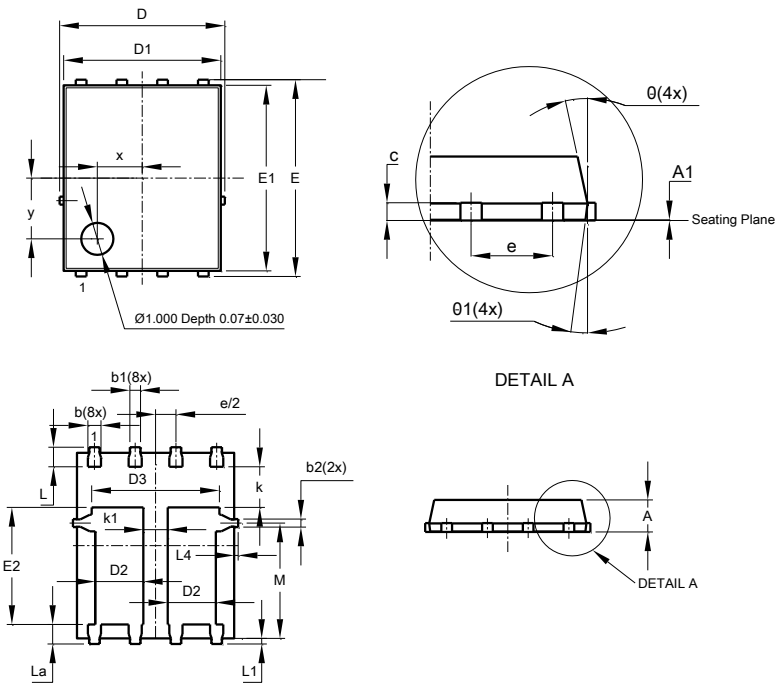
Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI5060-8 (Type C)

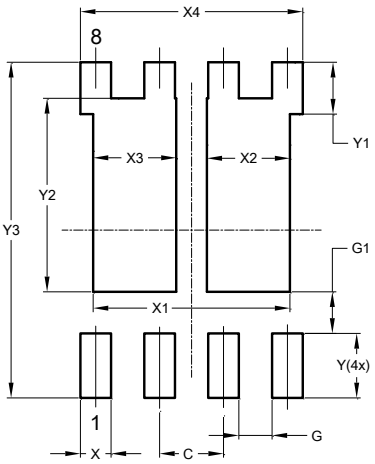


PowerDI5060-8 (Type C)			
Dim	**Min**	**Max**	**Typ**
A	0.90	1.10	1.00
A1	0	0.05	0.02
b	0.33	0.51	0.41
b1	0.300	0.366	0.333
b2	0.20	0.35	0.25
c	0.23	0.33	0.277
D	5.15 BSC		
D1	4.85	4.95	4.90
D2	1.40	1.60	1.50
D3	-	-	3.98
E	6.15 BSC		
E1	5.75	5.85	5.80
E2	3.56	3.76	3.66
e	1.27BSC		
k	-	-	1.27
k1	0.56	-	-
L	0.51	0.71	0.61
La	0.51	0.71	0.61
L1	0.05	0.20	0.175
L4	-	-	0.125
M	3.50	3.71	3.605
x	-	-	1.400
y	-	-	1.900
θ	10°	12°	11°
θ1	6°	8°	7°
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI5060-8 (Type C)



Dimensions	Value (in mm)
C	1.270
G	0.660
G1	0.820
X	0.610
X1	3.910
X2	1.650
X3	1.650
X4	4.420
Y	1.270
Y1	1.020
Y2	3.810
Y3	6.610

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