



STD2NK70Z - STD2NK70Z-1

N-CHANNEL 700 V - 6 Ω - 1.6 A DPAK/IPAK

Zener-Protected SuperMESH™ MOSFET

Table 1: General Features

TYPE	V _{DSS}	R _{DS(on)}	I _D	P _w
STD2NK70Z	700 V	7 Ω	1.6 A	45 W
STD2NK70Z-1	700 V	7 Ω	1.6 A	45 W

- TYPICAL R_{DS(on)} = 6 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- ESD IMPROVED CAPABILITY
- 100% AVALANCHE TESTED
- NEW HIGH VOLTAGE BENCHMARK
- GATE CHARGE MINIMIZED

DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding application. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

APPLICATIONS

- SINGLE-ENDED SMPS IN MONITORS, COMPUTER AND INDUSTRIAL APPLICATION
- WELDING EQUIPMENT
- FLYBACK CONFIGURATION FOR BATTERY CHARGER

Figure 1: Package

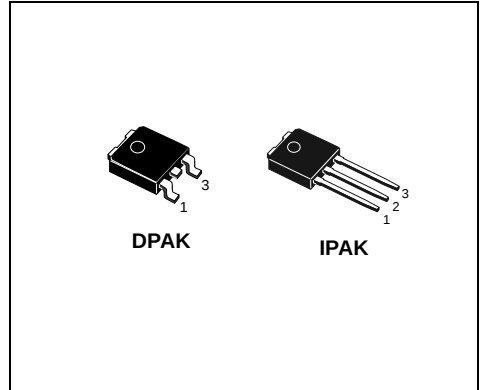


Figure 2: Internal Schematic Diagram

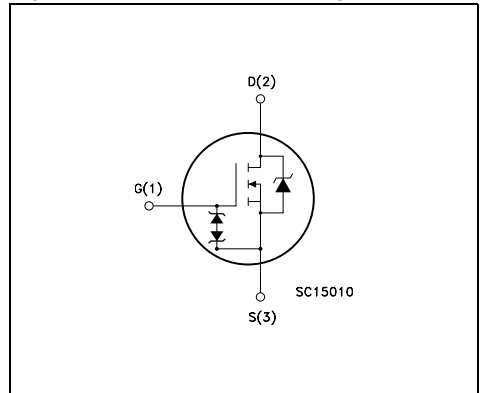


Table 2: Order Codes

Sales Type	Marking	Package	Packaging
STD2NK70ZT4	D2NK70Z	DPAK	TAPE & REEL
STD2NK70Z-1	D2NK70Z	IPAK	TUBE

Table 3: Absolute Maximum ratings

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	700	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 KΩ)	700	V
V _{GS}	Gate- source Voltage	± 30	V
I _D	Drain Current (continuous) at T _C = 25°C	1.6	A
I _D	Drain Current (continuous) at T _C = 100°C	1	A
I _{DM} (*)	Drain Current (pulsed)	6.4	A
P _{TOT}	Total Dissipation at T _C = 25°C	45	W
	Derating Factor	0.36	W/°C
V _{ESD} (G-S)	Gate source ESD (HBM-C = 100pF, R = 1.5 KΩ)	2000	V
dv/dt (1)	Peak Diode Recovery voltage slope	4.5	V/ns
T _{stg}	Storage Temperature	-55 to 150	°C
T _j	Max. Operating Junction Temperature		

(*) Pulse width limited by safe operating area

(1) I_{SD} ≤ 1.6 A, di/dt ≤ 200 A/μs, V_{DD} ≤ V_(BR)DSS

Table 4: Thermal Data

R _{thj-case}	Thermal Resistance Junction-case Max	2.78	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient Max	100	°C/W
T _l	Maximum Lead Temperature For Soldering Purpose	300	°C

Table 5: Avalanche Characteristics

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max)	1.6	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	110	mJ

Table 6: Gate-Source Zener Diode

Symbol	Parameter	Test Condition	Min.	Typ.	Max	Unit
BV _{GSO}	Gate-Source Breakdown Voltage	I _{GS} = ± 1mA (Open Drain)	30			A

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

TABLE 7: ELECTRICAL CHARACTERISTICS ($T_{CASE} = 25^{\circ}\text{C}$ UNLESS OTHERWISE SPECIFIED)**On /Off**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	700			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$, $T_C = 125^{\circ}\text{C}$			1 50	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 50\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\text{ V}$, $I_D = 0.8\text{ A}$		6	7	Ω

Table 8: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	$V_{DS} = 15\text{ V}$, $I_D = 0.8\text{ A}$		1.4		S
C_{OSS} eq.(3)	Equivalent Output Capacitance	$V_{GS} = 0\text{ V}$, $V_{DS} = 0$ to 560 V		17		
C_{ISS} C_{OSS} C_{RSS}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$		280 35 6.5		pF pF pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on Delay Time Rise Time Turn-off-Delay Time Fall Time	$V_{DD} = 350\text{ V}$, $I_D = 0.8\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 17)		7 17 20 35		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 560\text{ V}$, $I_D = 0.8\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 20)		11.4 2 6.8	15	nC nC nC

Table 9: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (2)	Source-drain Current Source-drain Current (pulsed)				1.6 6.4	A A
V_{SD} (1)	Forward On Voltage	$I_{SD} = 1.6\text{ A}$, $V_{GS} = 0$			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 1.6$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 50\text{ V}$, $T_J = 25^{\circ}\text{C}$ (see Figure 18)		334 918 5.5		ns μC A
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 1.6$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 50\text{ V}$, $T_J = 150^{\circ}\text{C}$ (see Figure 18)		350 1050 6		ns μC A

(1) Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

(2) Pulse width limited by safe operating area

(3) C_{OSS} eq- is defined as a constant equivalent capacitance giving the same charging time as C_{OSS} when V_{DS} increases from 0 to 80% V_{DSS}

Figure 3: Safe Operating Area

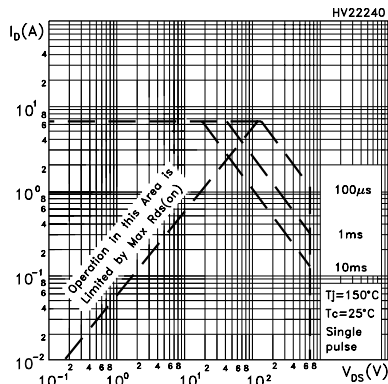


Figure 4: Output Characteristics

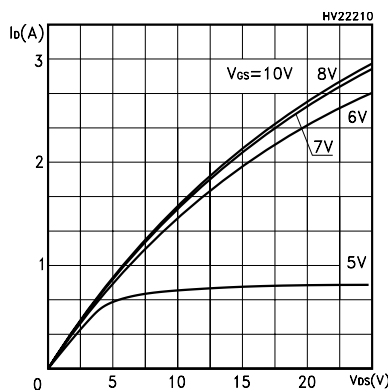


Figure 5: Transconductance

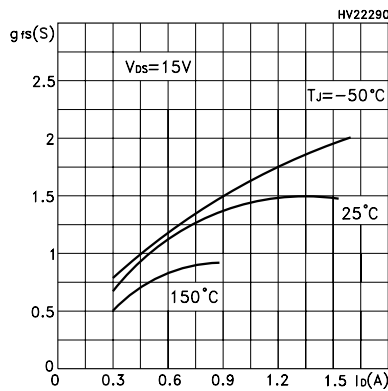


Figure 6: Thermal Impedance

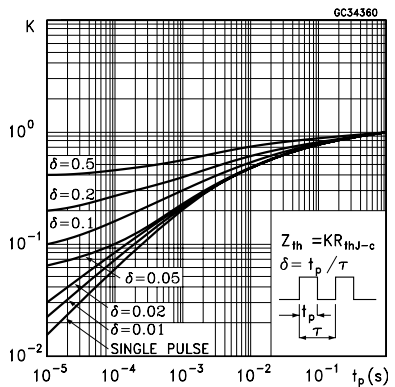


Figure 7: Transfer Characteristics

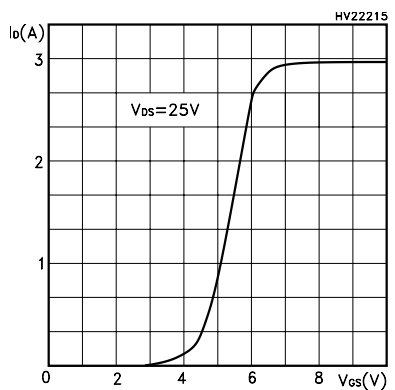


Figure 8: Static Drain-source On Resistance

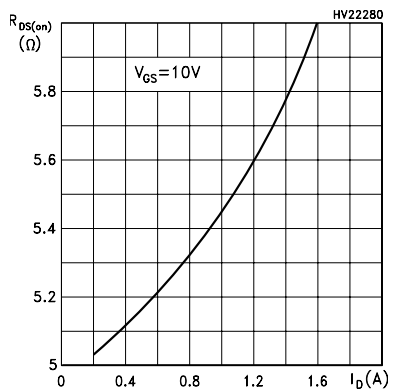


Figure 9: Gate Charge vs Gate-source Voltage

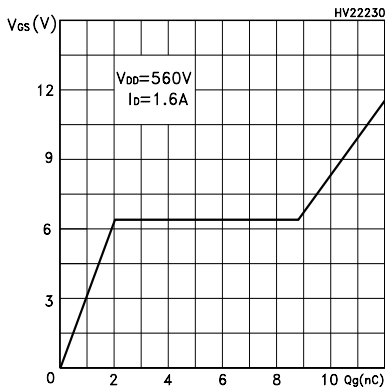


Figure 10: Normalized Gate Threshold Voltage vs Temperature

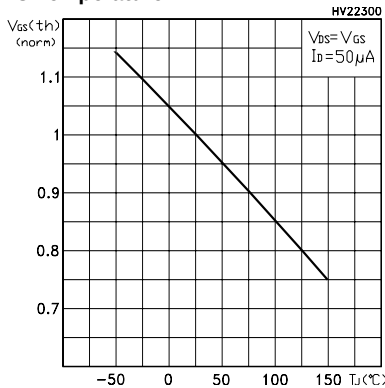


Figure 11: Dource-Drain Diode Forward Characteristics

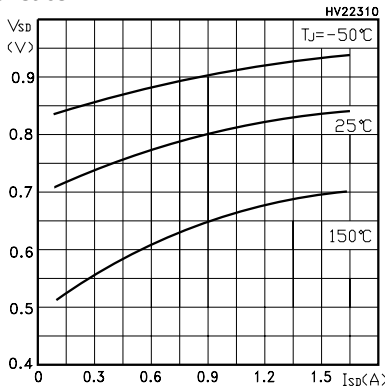


Figure 12: Capacitance Variations

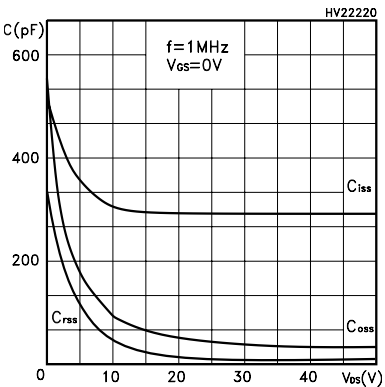


Figure 13: Normalized On Resistance vs Temperature

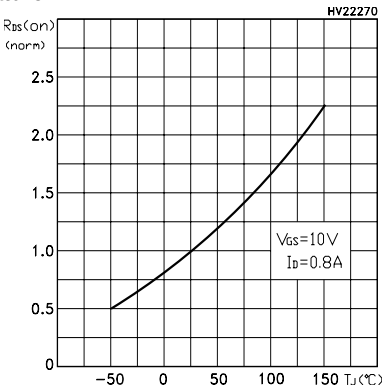


Figure 14: Normalized Breakdown Voltage vs Temperature

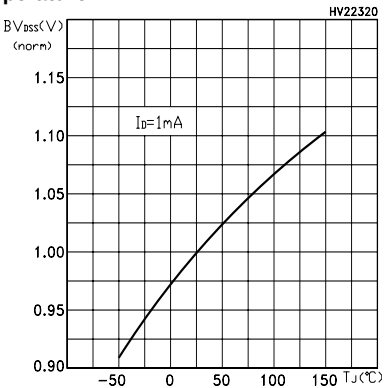


Figure 15: Maximum Avalanche Energy vs Temperature

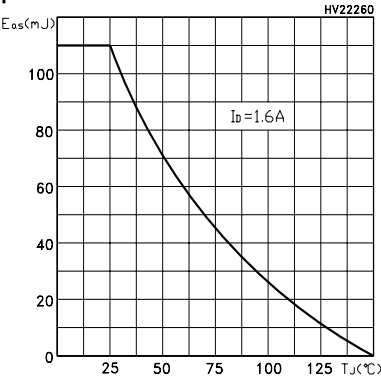


Figure 16: Unclamped Inductive Load Test Circuit

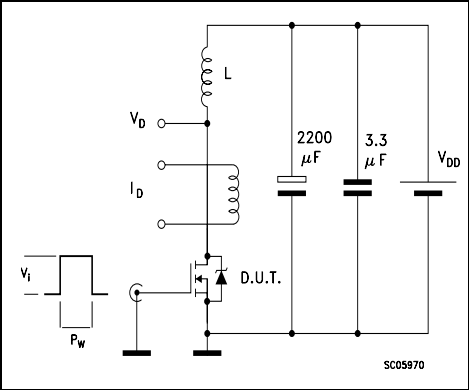


Figure 17: Switching Times Test Circuit For Resistive Load

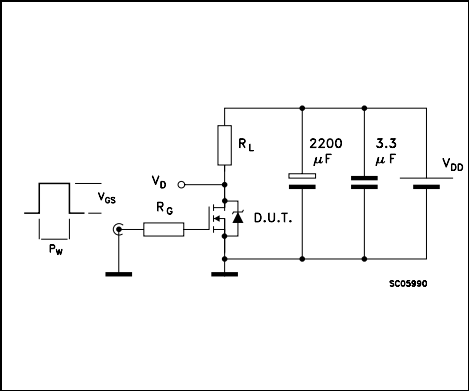


Figure 18: Test Circuit For Inductive Load Switching and Diode Recovery Times

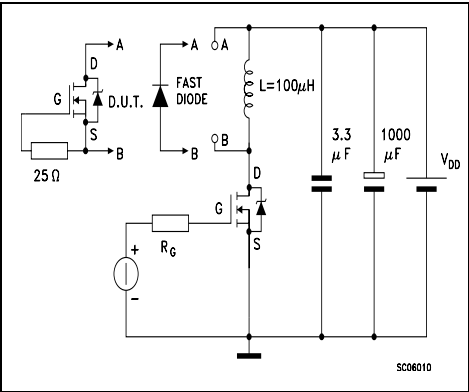


Figure 19: Unclamped Inductive Waferform

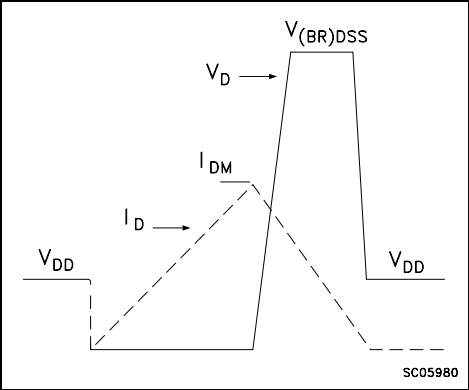
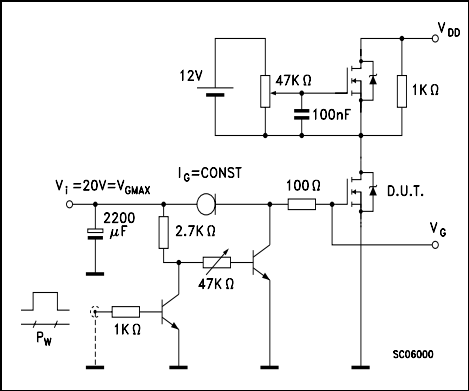
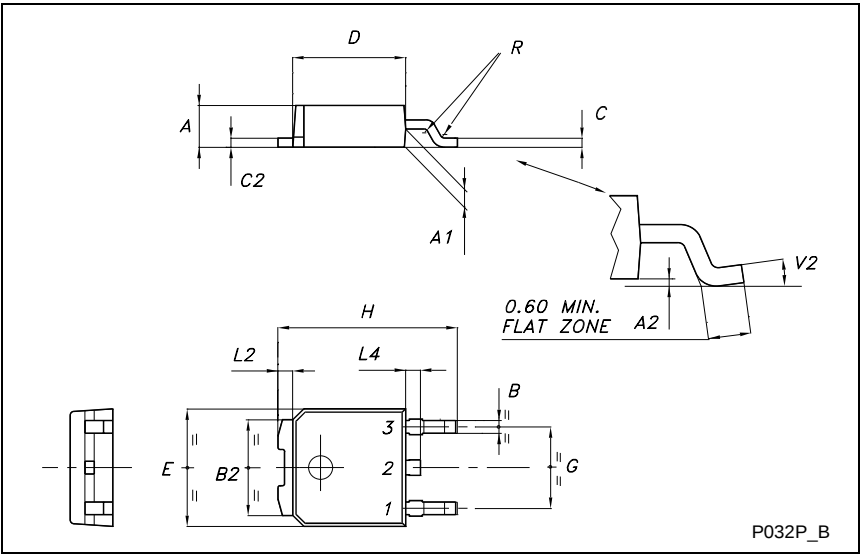


Figure 20: Gate Charge Test Circuit



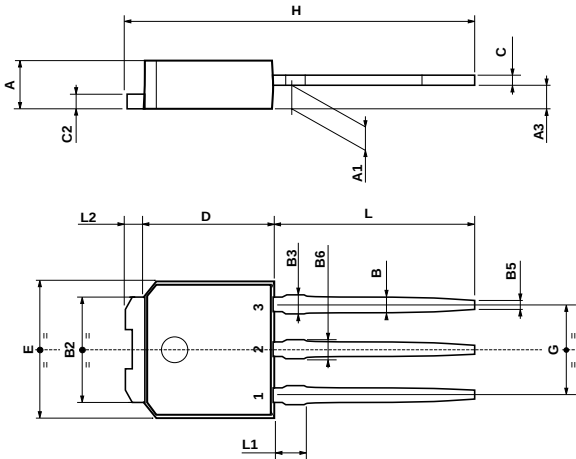
TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
C	0.45		0.60	0.018		0.024
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.60	0.252		0.260
G	4.40		4.60	0.173		0.181
H	9.35		10.10	0.368		0.398
L2		0.8			0.031	
L4	0.60		1.00	0.024		0.039
V2	0°		8°	0°		0°



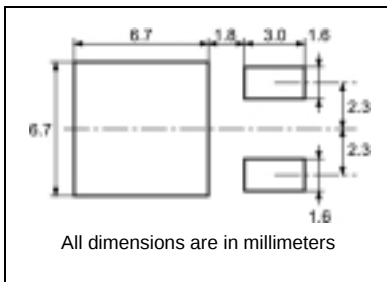
TO-251 (IPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039

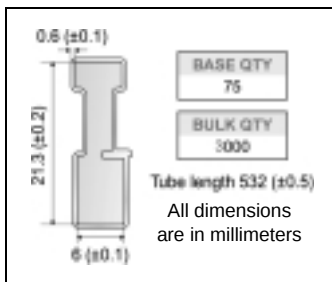
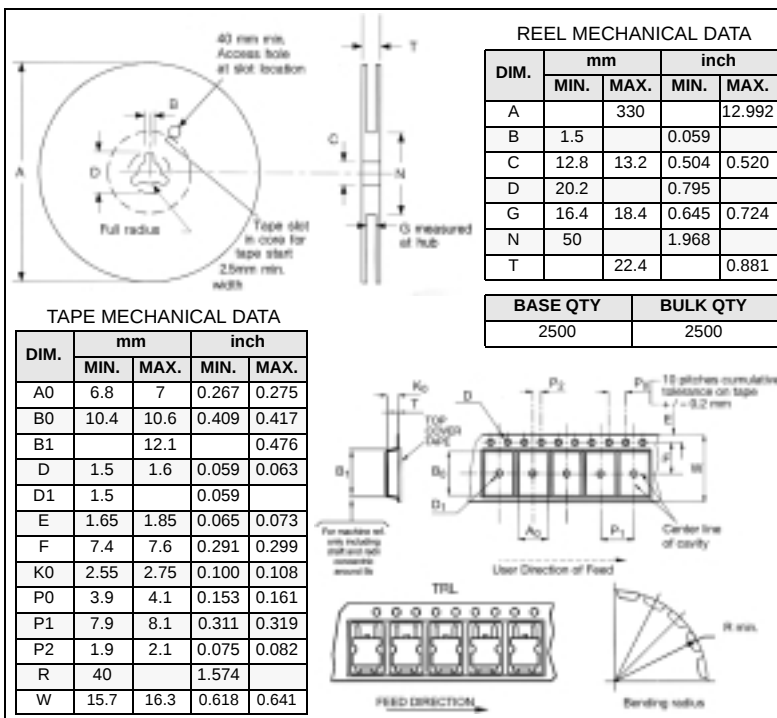


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DPAK FOOTPRINT



TUBE SHIPMENT (no suffix)*

**TAPE AND REEL SHIPMENT (suffix "T4")***

* on sales type

Table 10: Revision History

Date	Revision	Description of Changes
07-Sep-2004	1	First Release, complete document.
24-Jan-2005	2	New curve, figure 3, and new Rds(on) value Max.

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