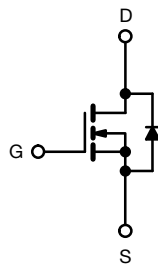
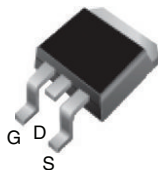


Power MOSFET

D²PAK (TO-263)


N-Channel MOSFET

PRODUCT SUMMARY

V_{DS} (V)	200	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	0.80
Q_g (Max.) (nC)	16	
Q_{gs} (nC)	2.9	
Q_{gd} (nC)	9.6	
Configuration	Single	

FEATURES

- Surface-mount
- Available in tape and reel
- Dynamic dV/dt rating
- Repetitive avalanche rated
- Logic level gate drive
- $R_{DS(on)}$ specified at $V_{GS} = 4\text{ V}$ and 5 V
- Fast switching
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details



RoHS*
Available
HALOGEN
FREE
Available

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D²PAK (TO-263) is a surface-mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface-mount package. The D²PAK (TO-263) is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.

ORDERING INFORMATION

Package	D ² PAK (TO-263)	D ² PAK (TO-263)
Lead (Pb)-free and Halogen-free	SiHL620S-GE3	SiHL620STRL-GE3 ^a
Lead (Pb)-free	IRL620SPbF	IRL620STRLPbF ^a

Note

a. See device orientation

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	200	V
Gate-Source Voltage	V_{GS}	± 10	
Continuous Drain Current	V_{GS} at 5 V	$T_C = 25\text{ }^\circ\text{C}$	A
		$T_C = 100\text{ }^\circ\text{C}$	
Pulsed Drain Current ^a	I_{DM}	21	W/ $^\circ\text{C}$
Linear Derating Factor		0.40	
Linear Derating Factor (PCB Mount) ^e		0.025	
Single Pulse Avalanche Energy ^b	E_{AS}	125	mJ
Repetitive Avalanche Current ^a	I_{AR}	5.2	A
Repetitive Avalanche Energy ^a	E_{AR}	5.0	mJ
Maximum Power Dissipation	P_D	$T_C = 25\text{ }^\circ\text{C}$	W
Maximum Power Dissipation (PCB Mount) ^e		$T_A = 25\text{ }^\circ\text{C}$	
Peak Diode Recovery dV/dt ^c	dV/dt	5.0	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s	300 ^d	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- $V_{DD} = 50\text{ V}$, starting $T_J = 25\text{ }^\circ\text{C}$, $L = 6.9\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 5.2\text{ A}$ (see fig. 12)
- $I_{SP} \leq 5.2\text{ A}$, $dI/dt \leq 95\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$
- 1.6 mm from case
- When mounted on 1" square PCB (FR-4 or G-10 material)

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Maximum Junction-to-Ambient (PCB)	R_{thJA}	-	40	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	2.5	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material)

SPECIFICATIONS ($T_J = 25^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0, I _D = 250 μA		200	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.27	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		1.0	-	2.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 10 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 200 V, V _{GS} = 0 V		-	-	25	μA
		V _{DS} = 320 V, V _{GS} = 0 V, T _J = 125 °C		-	-	250	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 3.1 A ^b	-	-	0.80	Ω
		V _{GS} = 4.0 V	I _D = 2.6 A ^b	-	-	1.0	
Forward Transconductance	g _{fs}	V _{DS} = 50 V, I _D = 3.1 A ^b		1.2	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	360	-	pF
Output Capacitance	C _{oss}			-	91	-	
Reverse Transfer Capacitance	C _{rss}			-	27	-	
Total Gate Charge	Q _g	V _{GS} = 5.0 V	I _D = 5.2 A, V _{DS} = 160 V, see fig. 6 and 13 ^b	-	-	16	nC
Gate-Source Charge	Q _{gs}			-	-	2.9	
Gate-Drain Charge	Q _{gd}			-	-	9.6	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 100 V, I _D = 5.2 A, R _g = 9.0 Ω, R _D = 20 Ω, see fig. 10 ^b		-	4.2	-	ns
Rise Time	t _r			-	31	-	
Turn-Off Delay Time	t _{d(off)}			-	18	-	
Fall Time	t _f			-	17	-	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal Source Inductance	L _S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	5.2	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	21	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 5.2 A, V _{GS} = 0 V ^b		-	-	1.8	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 5.2 A, dI/dt = 100 A/μs ^b		-	180	270	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	1.1	1.7	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. Pulse width $\leq 300\ \mu\text{s}$; duty cycle $\leq 2\ \%$



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

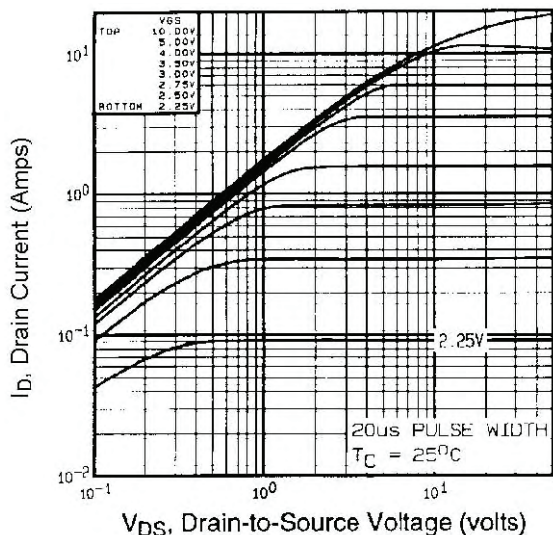


Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^{\circ}\text{C}$

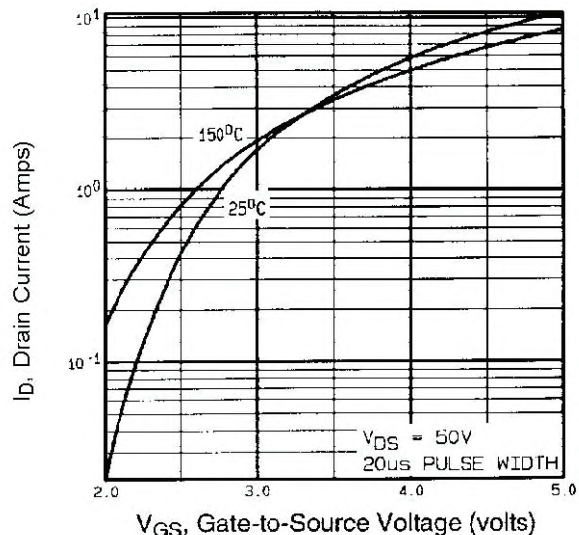


Fig. 2 - Typical Transfer Characteristics

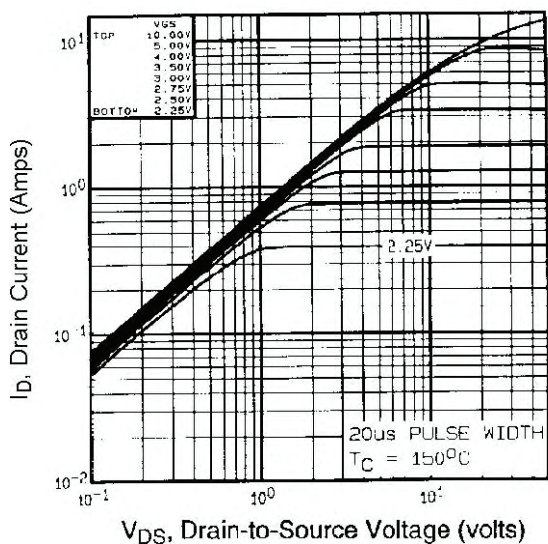


Fig. 1 - Typical Output Characteristics, $T_C = 150\text{ }^{\circ}\text{C}$

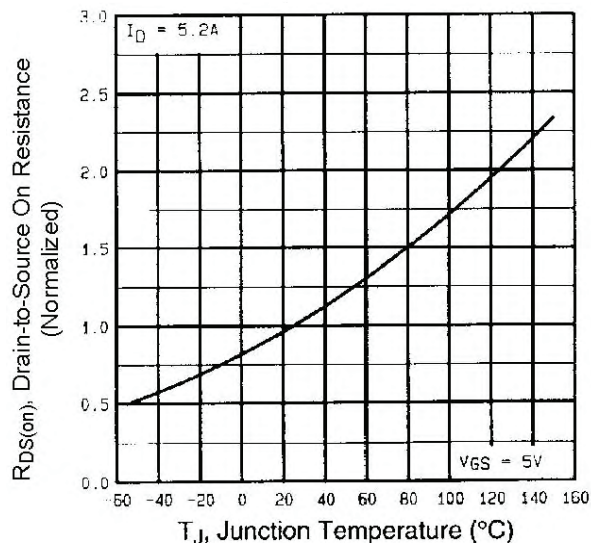
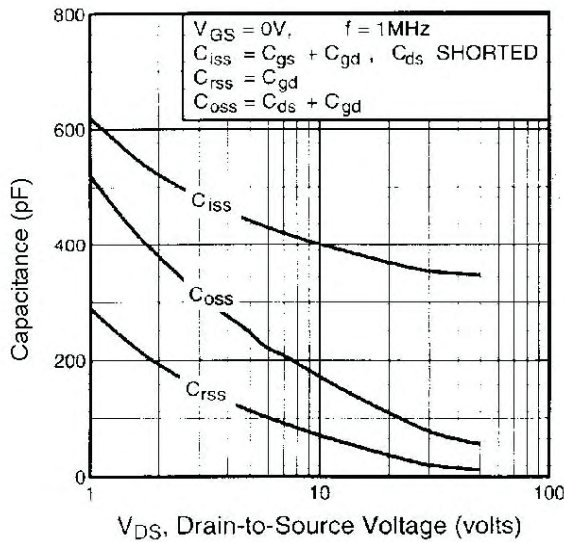
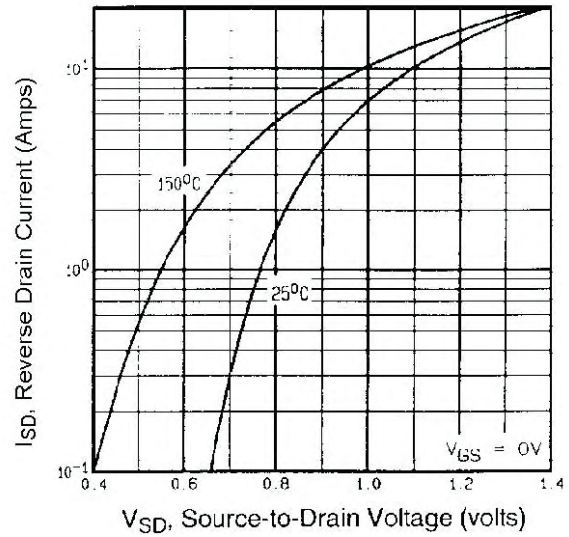
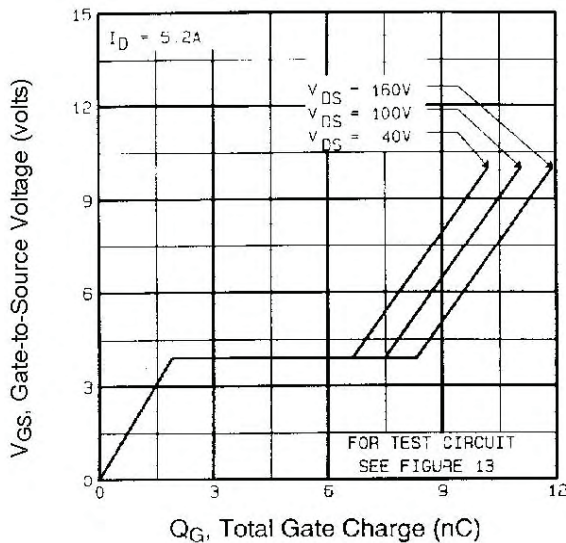
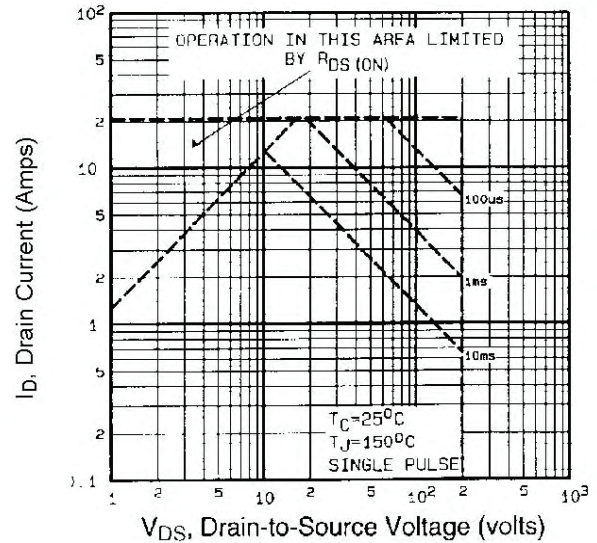
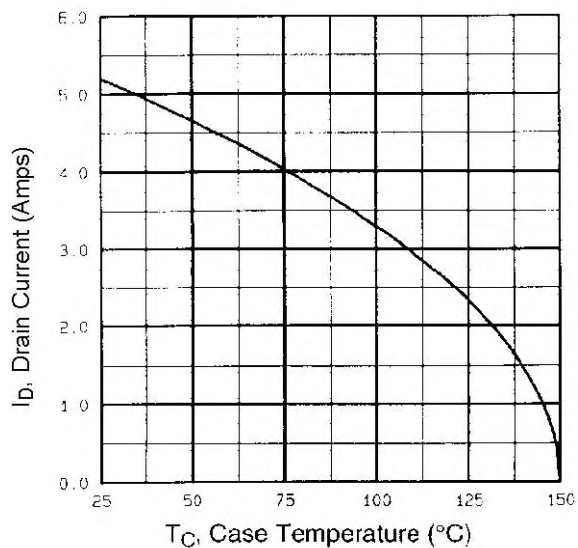
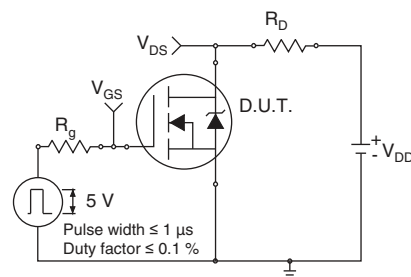
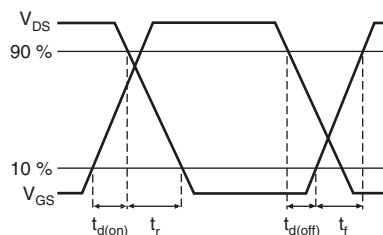
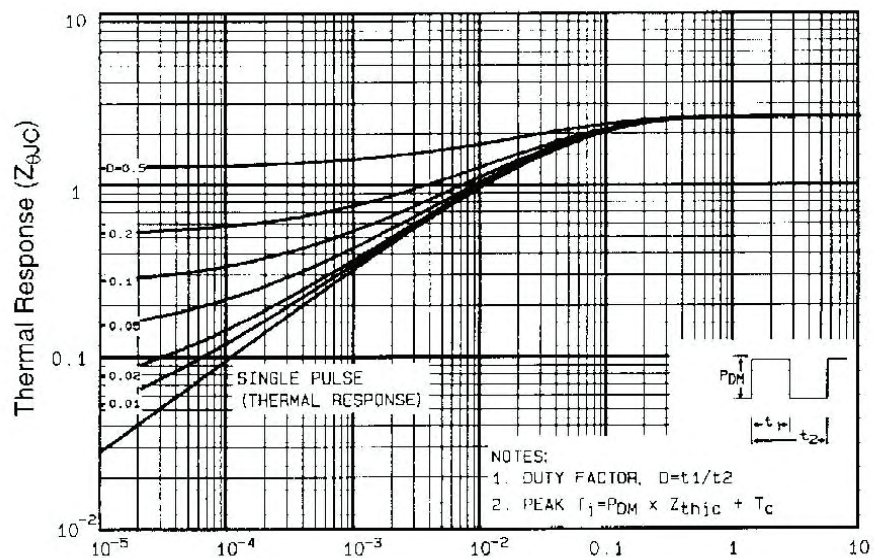
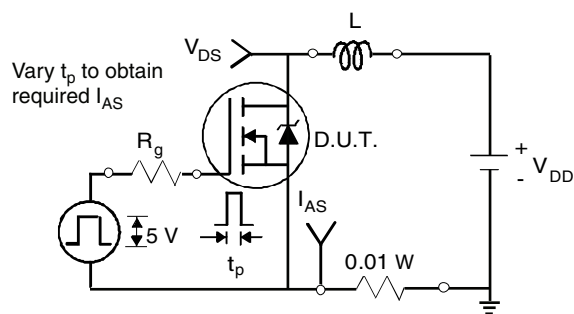
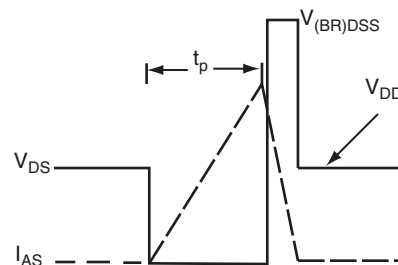
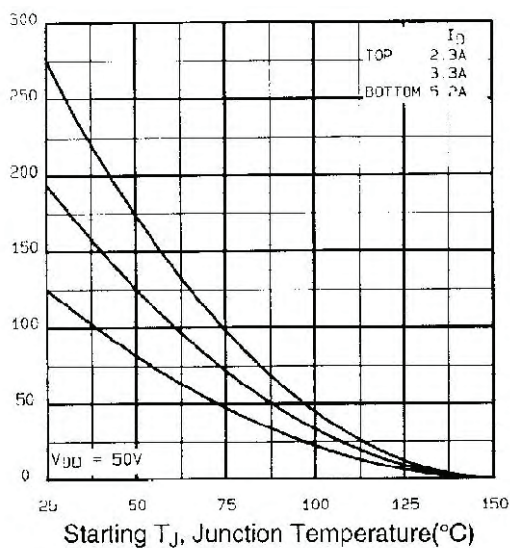
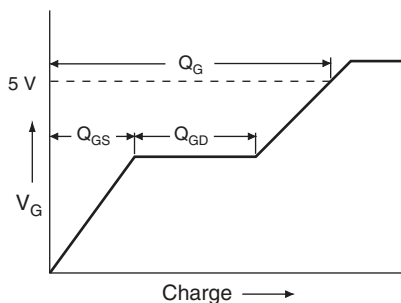
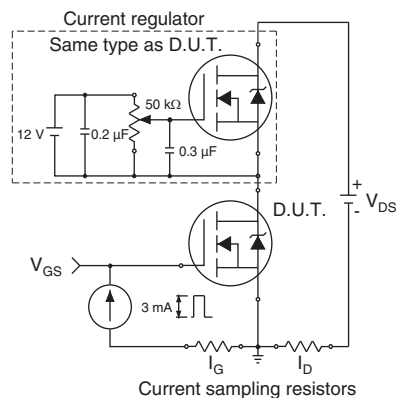
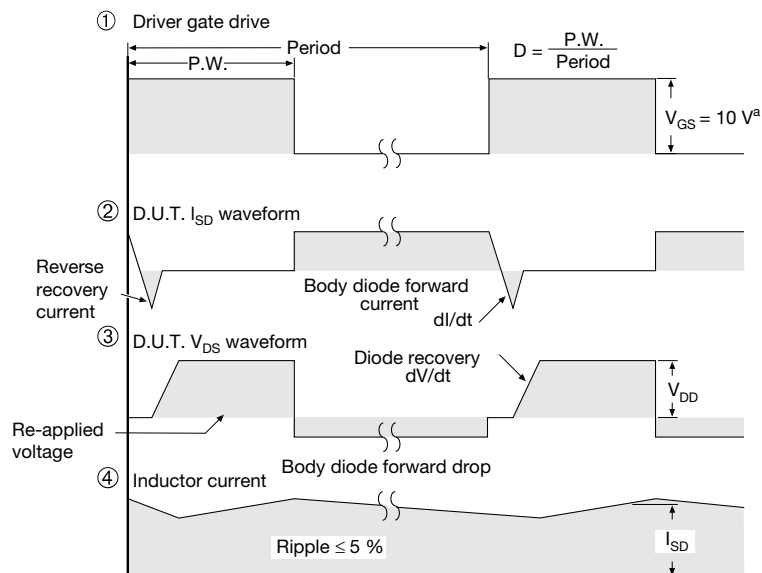
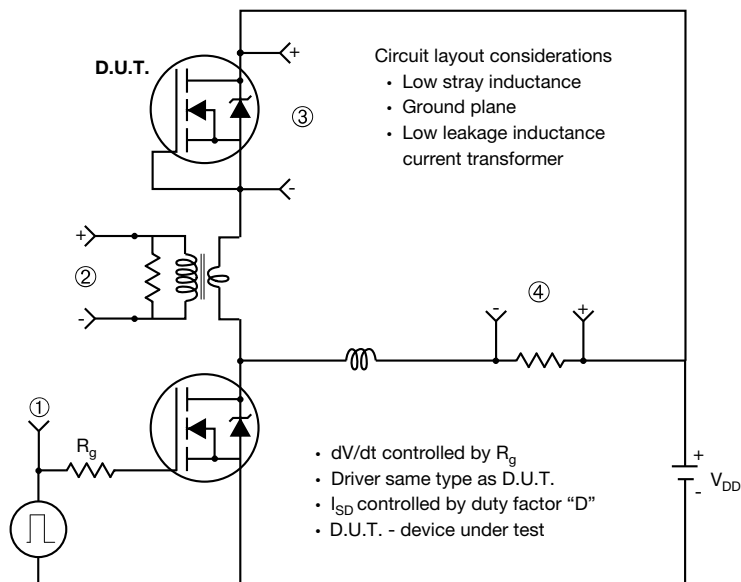


Fig. 3 - Normalized On-Resistance vs. Temperature


Fig. 4 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 6 - Typical Source-Drain Diode Forward Voltage

Fig. 5 - Typical Gate Charge vs. Gate-to-Source Voltage

Fig. 7 - Maximum Safe Operating Area


Fig. 8 - Maximum Drain Current vs. Case Temperature

Fig. 10a - Switching Time Test Circuit

Fig. 10b - Switching Time Waveforms

Fig. 9 - Maximum Effective Transient Thermal Impedance, Junction-to-Case


Fig. 12a - Unclamped Inductive Test Circuit

Fig. 12b - Unclamped Inductive Waveforms

Fig. 12c - Maximum Avalanche Energy vs. Drain Current

Fig. 13a - Basic Gate Charge Waveform

Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

Note

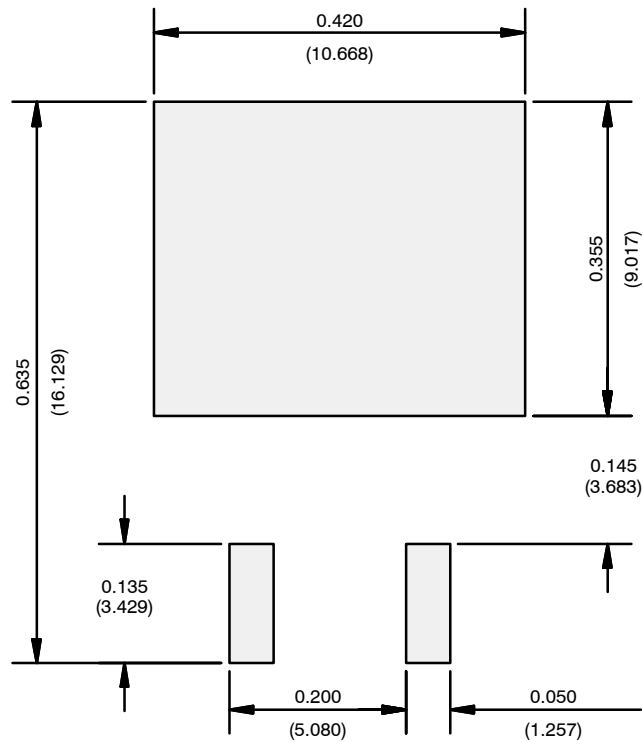
a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 10 - For N-Channel

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	MILLIMETERS		INCHES	
DIM.	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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