CY7C109BN, CY7C1009BN

128K x 8 Static RAM

Features

- High Speed
  - t_{AA} = 15 ns
- Low Active Power
  - 440 mW (maximum 15 ns)
- Low CMOS Standby Power
  - 55 mW (maximum) 4 mW
- 2.0V Data Retention
- Automatic Power Down when deselected
- TTL-compatible Inputs and Outputs
- Easy Memory Expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ options

Functional Description

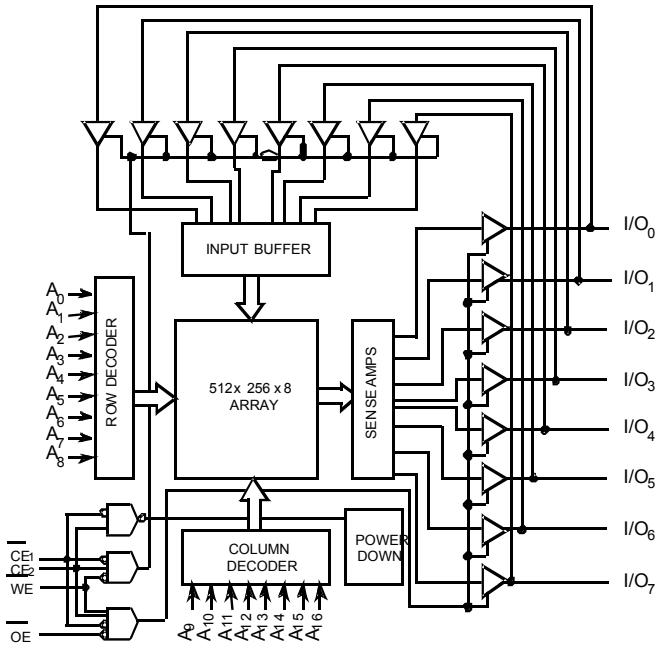
The CY7C109BN/CY7C1009BN[1] is a high performance CMOS static RAM organized as 131,072 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}_1$), an active HIGH Chip Enable (CE_2), an active LOW Output Enable ($\overline{OE}$), and three-state drivers. Writing to the device is accomplished by taking Chip Enable One ($\overline{CE}_1$) and Write Enable ($\overline{WE}$) inputs LOW and Chip Enable Two (CE_2) input HIGH. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking Chip Enable One ($\overline{CE}_1$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) and Chip Enable Two (CE_2) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high impedance state when the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW).

The CY7C109BN is available in standard 400-mil-wide SOJ and 32-pin TSOP type I packages. The CY7C1009BN is available in a 300-mil-wide SOJ package. The CY7C1009BN and CY7C109BN are functionally equivalent in all other respects.

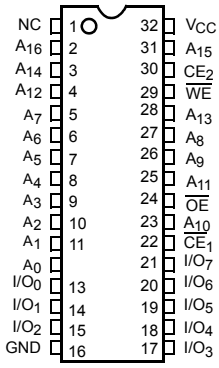
Logic Block Diagram



Note
1. For guidelines on SRAM system design, refer to the 'System Design Guidelines' Cypress application note, available on the internet at www.cypress.com.

Pin Configurations

Figure 1. 32-Pin SOJ (TopView)



Selection Guide

Description		7C109B-15 7C1009B-15	7C109B-20 7C1009B-20	Unit
Maximum Access Time		15	20	ns
Maximum Operating Current		80	75	mA
Maximum CMOS Standby Current		10	10	mA
	L	2	2	mA

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[2] .....–0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State[2] ..... –0.5V to V_{CC} + 0.5V

DC Input Voltage[2] ..... –0.5V to V_{CC} + 0.5V

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	–40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		7C109BN-15 7C1009BN-15		7C109BN-20 7C1009BN-20		Unit
				Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = –4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[2]			–0.3	0.8	–0.3	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		–1	+1	–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		–5	+5	–5	+5	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max, V_{OUT} = GND			–300		–300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max, I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$			80		75	mA
I_{SB1}	Automatic CE Power Down Current —TTL Inputs	Max V_{CC}, $\overline{CE}_1$ ≥ V_{IH} or CE_2 ≤ V_{IL}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}			40		30	mA
I_{SB2}	Automatic CE Power Down Current —CMOS Inputs	Max V_{CC}, $\overline{CE}_1$ ≥ V_{CC} – 0.3V, or CE_2 ≤ 0.3V, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, f = 0			10		10	mA
			L		2		2	mA

Capacitance

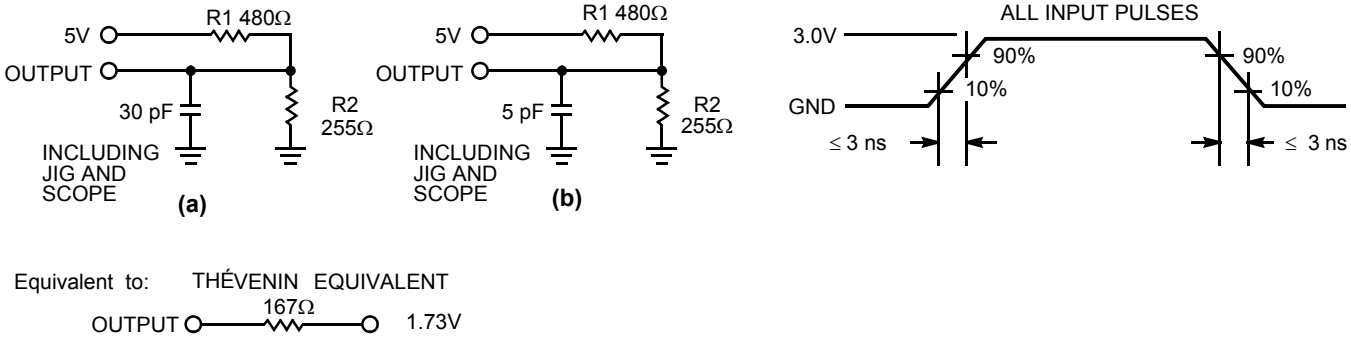
The following are the input and outpiut capacitance test conditions.[4]

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	9	pF
C_{OUT}	Output Capacitance		8	pF

Notes
2. Minimum voltage is –2.0V for pulse durations of less than 20 ns.
3. Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.

[+] Feedback

Figure 2. AC Test Loads and Waveforms



Switching Characteristics[5] Over the Operating Range

Parameter	Description	7C109BN-15 7C1009BN-15		7C109BN-20 7C1009BN-20		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read Cycle Time	15		20		ns
t_{AA}	Address to Data Valid		15		20	ns
t_{OHA}	Data Hold from Address Change	3		3		ns
t_{ACE}	$\overline{CE}_1$ LOW to Data Valid, CE_2 HIGH to Data Valid		15		20	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		7		8	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6, 7]		7		8	ns
t_{LZCE}	$\overline{CE}_1$ LOW to Low Z, CE_2 HIGH to Low Z[7]	3		3		ns
t_{HZCE}	$\overline{CE}_1$ HIGH to High Z, CE_2 LOW to High Z[6, 7]		7		8	ns
t_{PU}	$\overline{CE}_1$ LOW to Power Up, CE_2 HIGH to Power Up	0		0		ns
t_{PD}	$\overline{CE}_1$ HIGH to Power Down, CE_2 LOW to Power Down		15		20	ns
Write Cycle[8]						
t_{WC}	Write Cycle Time[9]	15		20		ns
t_{SCE}	$\overline{CE}_1$ LOW to Write End, CE_2 HIGH to Write End	12		15		ns
t_{AW}	Address Setup to Write End	12		15		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Setup to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	12		12		ns
t_{SD}	Data Setup to Write End	8		10		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6, 7]		7		8	ns

Notes

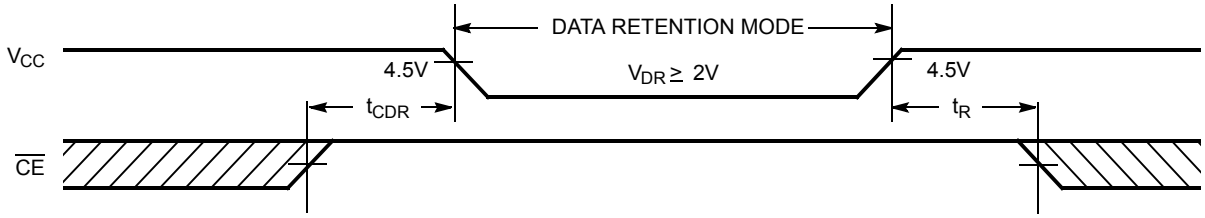
5. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
6. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}_1$ LOW, CE_2 HIGH, and $\overline{WE}$ LOW. $\overline{CE}_1$ and $\overline{WE}$ must be LOW and CE_2 HIGH to initiate a write, and the transition of any of these signals can terminate the write. The input data setup and hold timing should be referenced to the leading edge of the signal that terminates the write.
9. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

[+] Feedback

Data Retention Characteristics Over the Operating Range **(Low Power version only)**

Parameter	Description	Conditions	Min	Max	Unit
V_{DR}	V_{CC} for Data Retention	No input may exceed V_{CC} + 0.5V $V_{CC} = V_{DR} = 2.0V$, $\overline{CE}_1 \geq V_{CC} - 0.3V$ or $CE_2 \leq 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	2.0		V
I_{CCDR}	Data Retention Current			150	µA
t_{CDR}	Chip Deselect to Data Retention Time		0		ns
t_R	Operation Recovery Time		200		µs

Figure 3. Data Retention Waveform



Switching Waveforms

Figure 4. Read Cycle No. 1[10, 11]

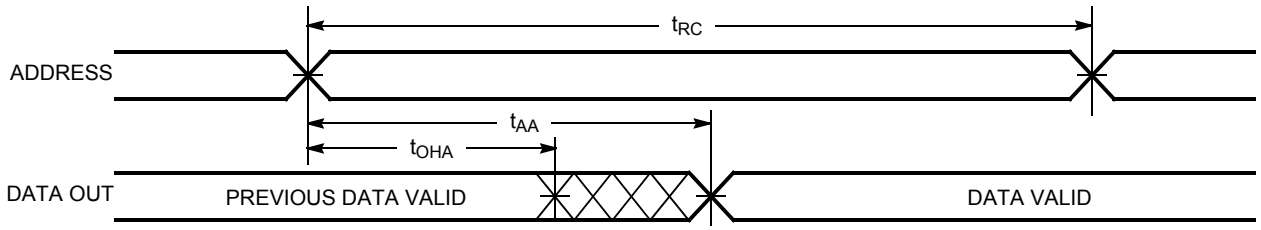
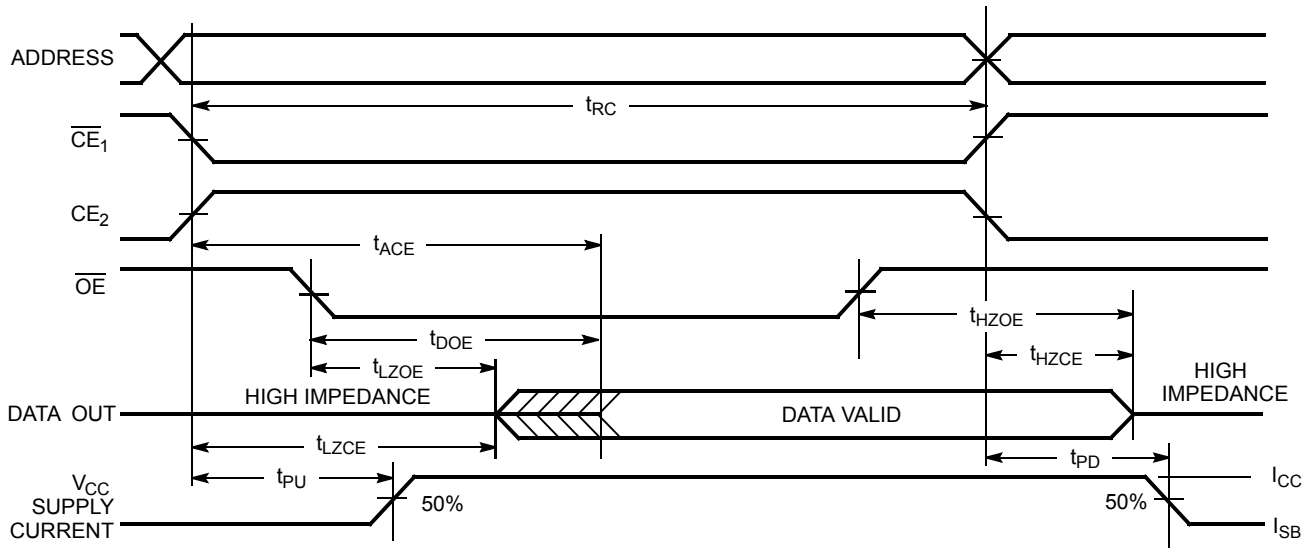


Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled)[11, 12]



Notes
10. Device is continuously selected. $\overline{OE}$, $\overline{CE}_1 = V_{IL}$, $CE_2 = V_{IH}$.
11. $\overline{WE}$ is HIGH for read cycle.
12. Address valid prior to or coincident with $\overline{CE}_1$ transition LOW and CE_2 transition HIGH.

[+] Feedback

Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 ($\overline{CE}_1$ or CE_2 Controlled)[13, 14]

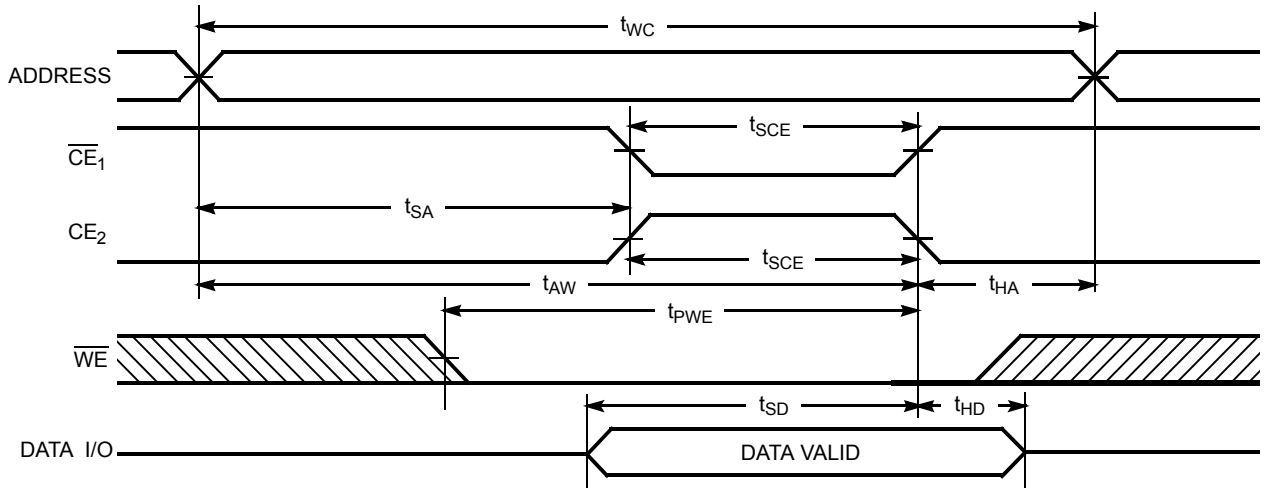
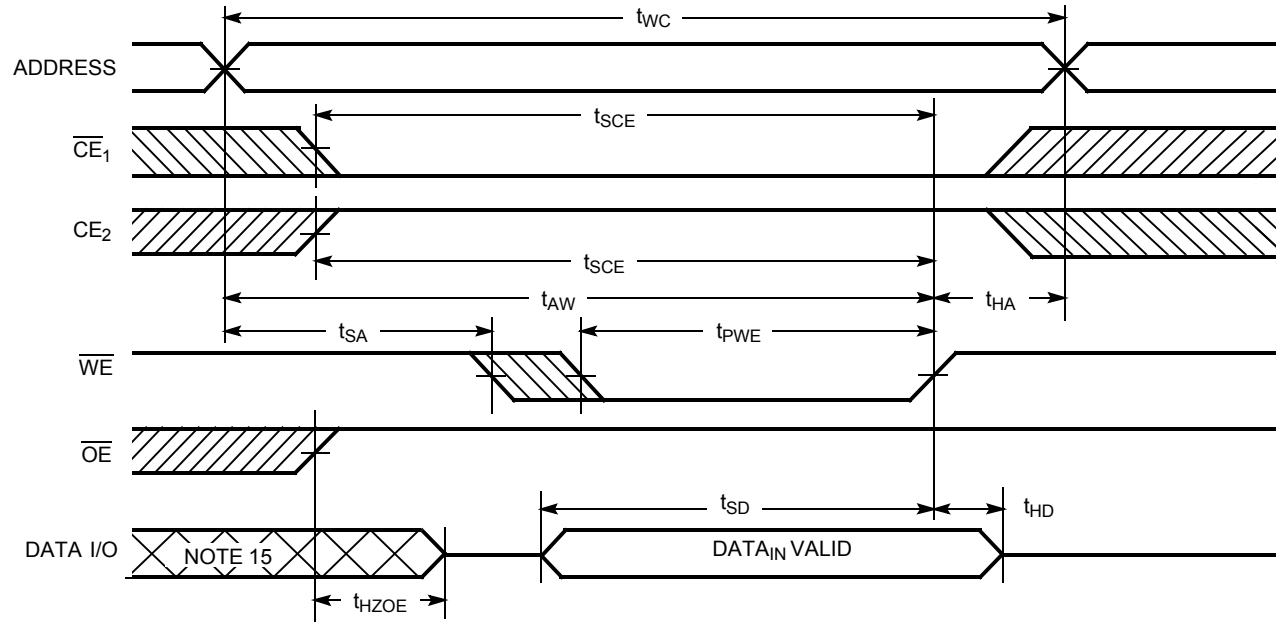


Figure 7. Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)[13, 14]

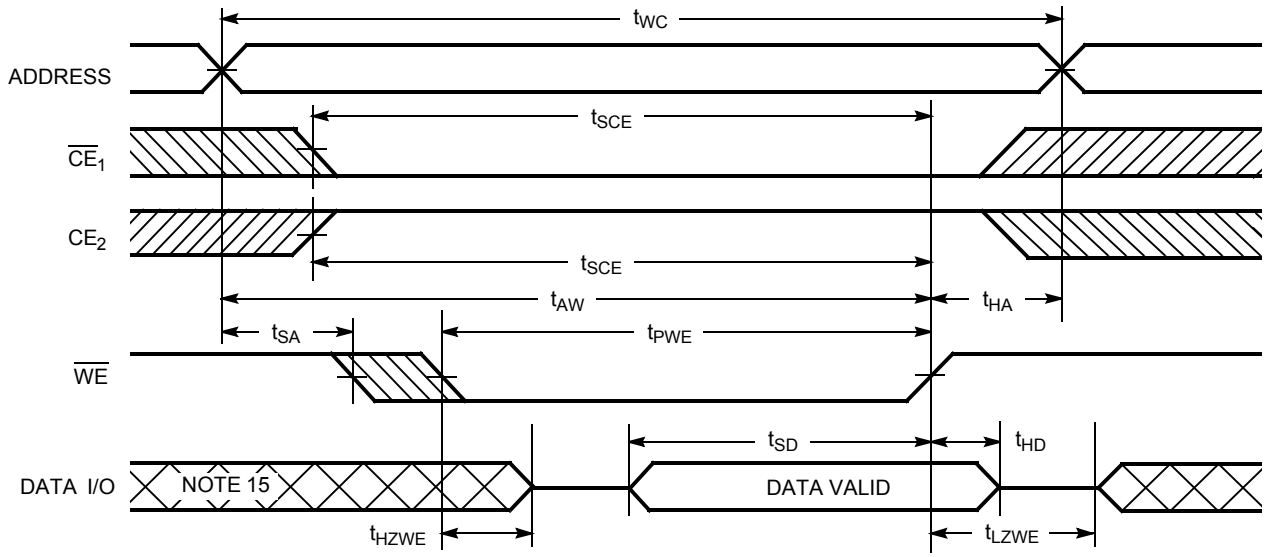


Notes
13. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
14. If $\overline{CE}_1$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.
15. During this period the I/Os are in the output state and input signals should not be applied.

[+] Feedback

Switching Waveforms (continued)

Figure 8. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[14]



Truth Table

$\overline{CE_1}$	CE_2	$\overline{OE}$	$\overline{WE}$	I/O_0–I/O_7	Mode	Power
H	X	X	X	High Z	Power Down	Standby (I_{SB})
X	L	X	X	High Z	Power Down	Standby (I_{SB})
L	H	L	H	Data Out	Read	Active (I_{CC})
L	H	X	L	Data In	Write	Active (I_{CC})
L	H	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
15	CY7C1009BN-15VI	51-85041	32-Pin (300-Mil) Molded SOJ	Industrial
20	CY7C109BN-20VI	51-85033	32-Pin (400-Mil) Molded SOJ	Industrial

Contact your local sales representative regarding availability of these parts

Package Diagrams

Figure 9. 32-Pin (300-Mil) Molded

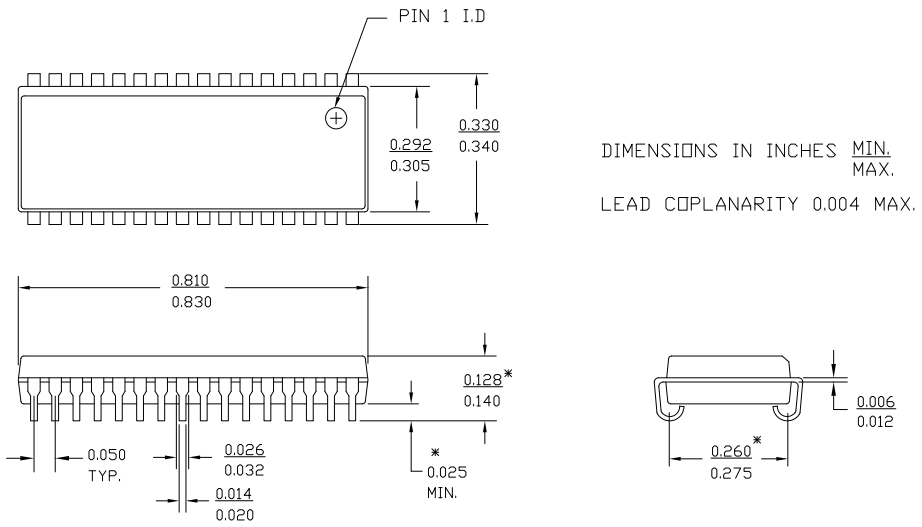
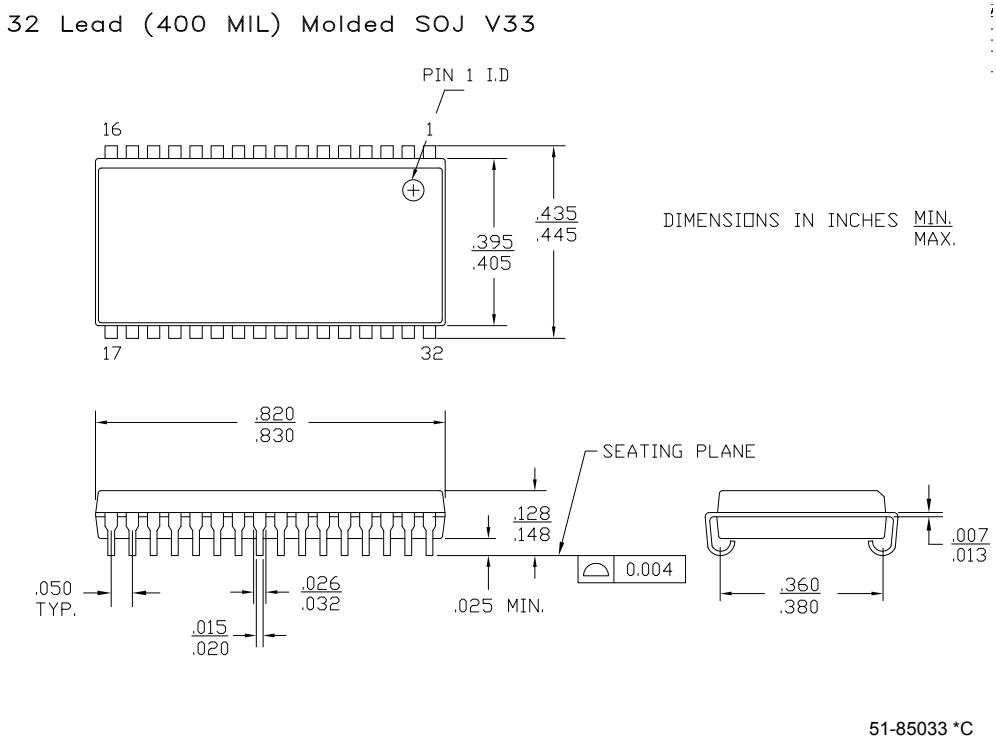


Figure 10. 32-Pin (400-Mil) Molded SOJ



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Document History Page

Document Title: CY7C109BN/CY7C1009BN 128K x 8 Static RAM Document Number: 001-06430				
REV.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	423847	NXR	See ECN	New Data Sheet
*A	2755340	NXR	08/24/2009	Removed -12 from product offering as 12ns parts are not active Corrected Package Diagram Updated ordering Information
*B	2904565	AJU	04/05/10	Removed inactive part number from the ordering information table.Updated package diagrams.

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