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March 2015

FDD6637

35V P-Channel PowerTrench[®] MOSFET

General Description

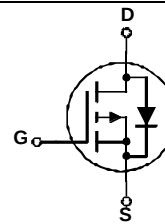
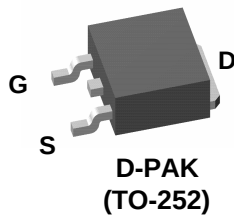
This P-Channel MOSFET has been produced using Fairchild Semiconductor's proprietary PowerTrench technology to deliver low $R_{DS(on)}$ and optimized B_{vds} capability to offer superior performance benefit in the applications.

Applications

- Inverter
- Power Supplies

Features

- 55 A, –35 V $R_{DS(on)} = 11.6 \text{ m}\Omega$ @ $V_{GS} = -10 \text{ V}$
 $R_{DS(on)} = 18 \text{ m}\Omega$ @ $V_{GS} = -4.5 \text{ V}$
- High performance trench technology for extremely low $R_{DS(on)}$
- RoHS Compliant



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain-Source Voltage	–35	V
$V_{DS(Avalanche)}$	Drain-Source Avalanche Voltage (maximum) (Note 4)	–40	V
V_{GS}	Gate-Source Voltage	± 25	V
I_D	Continuous Drain Current $@T_C = 25^\circ\text{C}$ (Note 3) $@T_A = 25^\circ\text{C}$ (Note 1a) Pulsed (Note 1a)	–55	A
		–13	
		–100	
P_D	Power Dissipation $@T_C = 25^\circ\text{C}$ (Note 3) $@T_A = 25^\circ\text{C}$ (Note 1a) $@T_A = 25^\circ\text{C}$ (Note 1b)	57	W
		3.1	
		1.3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	–55 to +150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	2.2	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	40	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1b)	96	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape width	Quantity
FDD6637	FDD6637	D-PAK (TO-252)	13"	16mm	2500 units

Electrical Characteristics

 $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Drain-Source Avalanche Ratings						
E_{AS}	Drain-Source Avalanche Energy (Single Pulse)	$V_{DD} = -35\text{ V}$, $I_D = -11\text{ A}$, $L=1\text{mH}$		61		mJ
I_{AS}	Drain-Source Avalanche Current			-14		A
Off Characteristics (Note 2)						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}$, $I_D = -250\text{ }\mu\text{A}$	-35			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -28\text{ V}$, $V_{GS} = 0\text{ V}$			-1	μA
I_{GSS}	Gate-Body Leakage	$V_{GS} = \pm 25\text{ V}$, $V_{DS} = 0\text{ V}$			± 100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = -250\text{ }\mu\text{A}$	-1	-1.6	-3	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10\text{ V}$, $I_D = -14\text{ A}$ $V_{GS} = -4.5\text{ V}$, $I_D = -11\text{ A}$ $V_{GS} = -10\text{ V}$, $I_D = -14\text{ A}$, $T_J=125^\circ\text{C}$		9.7 14.4 14.7	11.6 18 19	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS} = -5\text{ V}$, $I_D = -14\text{ A}$		35		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = -20\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1.0\text{ MHz}$		2370		pF
C_{oss}	Output Capacitance			470		pF
C_{rss}	Reverse Transfer Capacitance			250		pF
R_G	Gate Resistance	$f = 1.0\text{ MHz}$		3.6		Ω
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -20\text{ V}$, $I_D = -1\text{ A}$, $V_{GS} = -10\text{ V}$, $R_{GEN} = 6\text{ }\Omega$		18	32	ns
t_r	Turn-On Rise Time			10	20	ns
$t_{d(off)}$	Turn-Off Delay Time			62	100	ns
t_f	Turn-Off Fall Time			36	58	ns
Q_g	Total Gate Charge, $V_{GS} = -10\text{V}$	$V_{DS} = -20\text{ V}$, $I_D = -14\text{ A}$		45	63	nC
Q_g	Total Gate Charge, $V_{GS} = -5\text{V}$			25	35	nC
Q_{gs}	Gate-Source Charge			7		nC
Q_{gd}	Gate-Drain Charge			10		nC

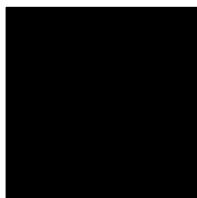
Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Drain–Source Diode Characteristics						
V_{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = -14\text{ A}$ (Note 2)		–0.8	–1.2	V
t_{rr}	Diode Reverse Recovery Time	$I_F = -14\text{ A}$, $diF/dt = 100\text{ A}/\mu\text{s}$		28		ns
Q_{rr}	Diode Reverse Recovery Charge			15		nC

Notes:

- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) $R_{\theta JA} = 40^\circ\text{C/W}$ when mounted on a 1 in^2 pad of 2 oz copper



b) $R_{\theta JA} = 96^\circ\text{C/W}$ when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%

- Maximum current is calculated as:
$$\sqrt{\frac{P_D}{R_{DS(ON)}}}$$

where P_D is maximum power dissipation at $T_C = 25^\circ\text{C}$ and $R_{DS(on)}$ is at $T_{J(max)}$ and $V_{GS} = 10\text{V}$. Package current limitation is 21A

- BV(avalanche) Single-Pulse rating is guaranteed if device is operated within the UIS SOA boundary of the device.

Typical Characteristics

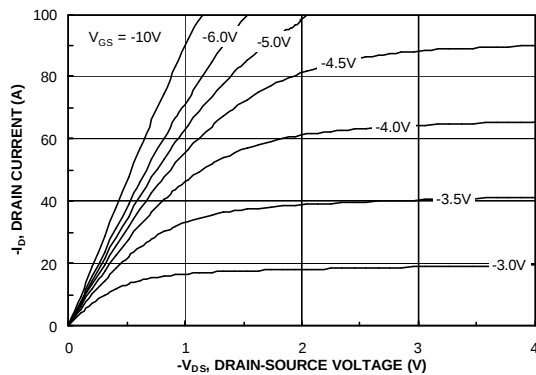


Figure 1. On-Region Characteristics

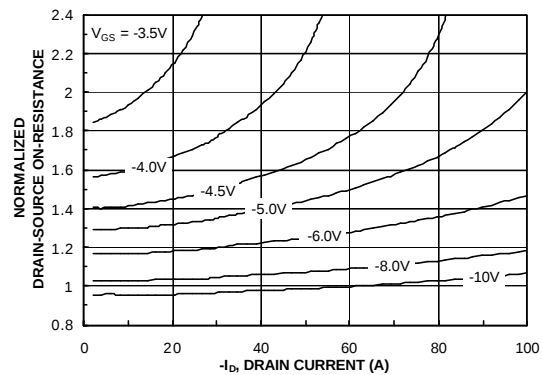


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

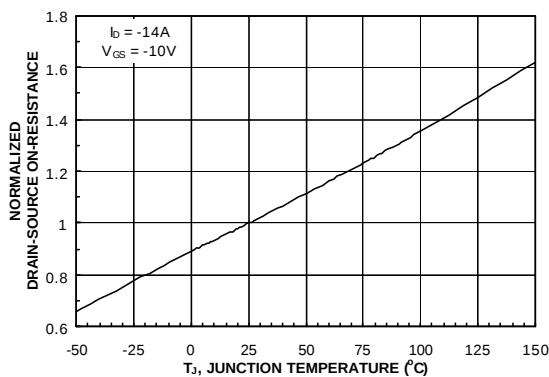


Figure 3. On-Resistance Variation with Temperature

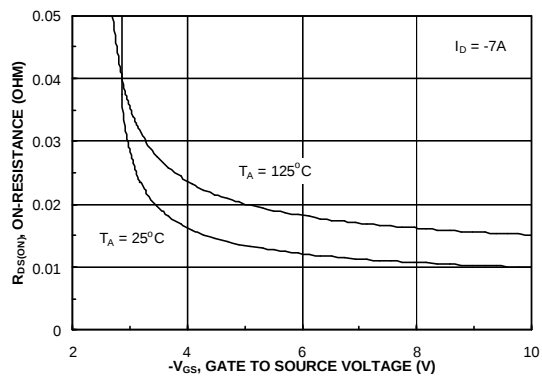


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

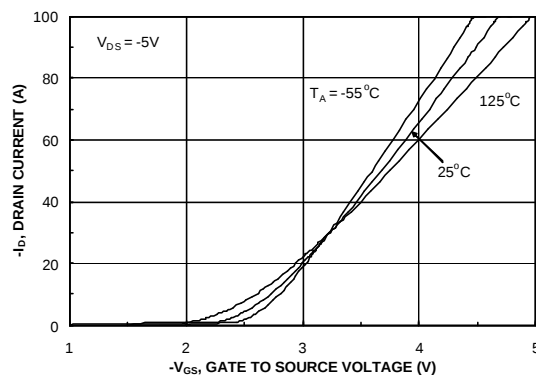


Figure 5. Transfer Characteristics

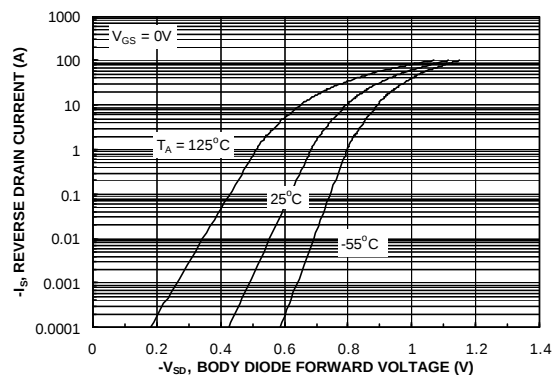


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

Typical Characteristics

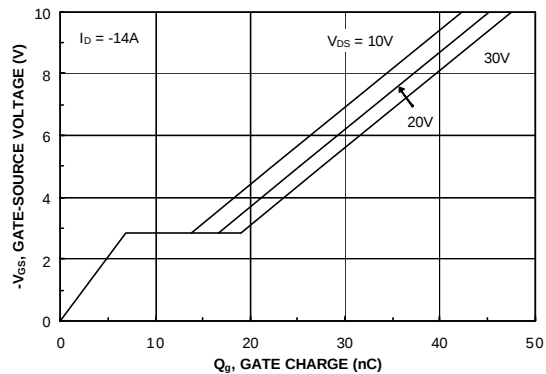


Figure 7. Gate Charge Characteristics

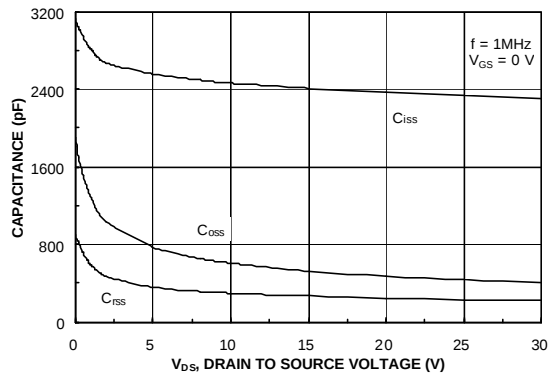


Figure 8. Capacitance Characteristics

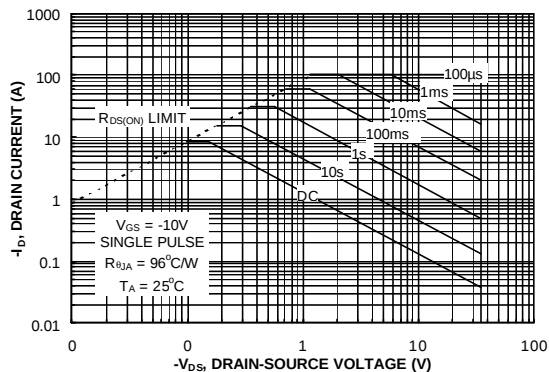


Figure 9. Maximum Safe Operating Area

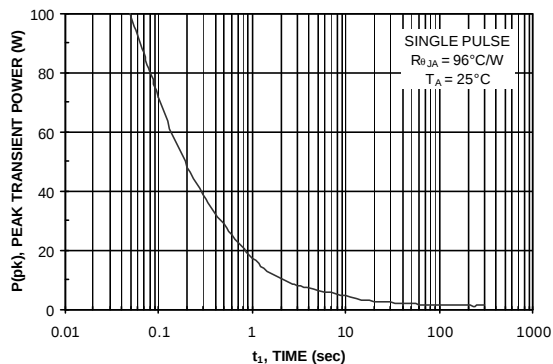


Figure 10. Single Pulse Maximum Power Dissipation

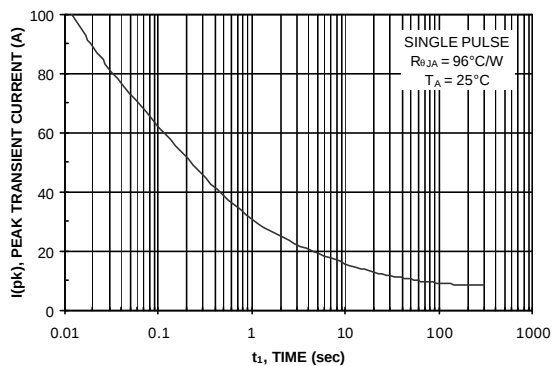


Figure 11. Single Pulse Maximum Peak Current

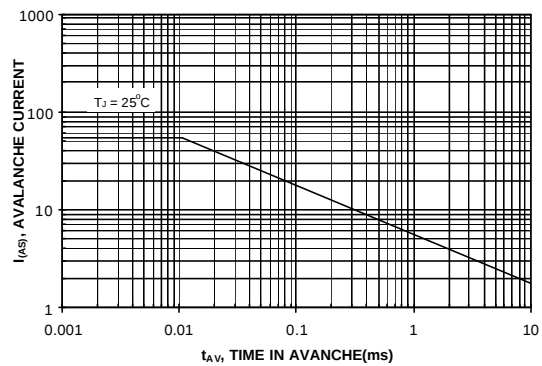


Figure 12. Unclamped Inductive Switching Capability

Typical Characteristics

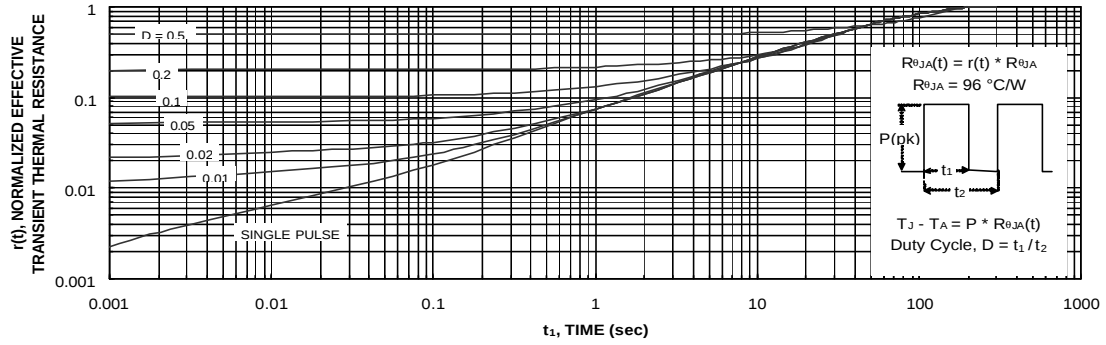


Figure 13. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

Test Circuits and Waveforms

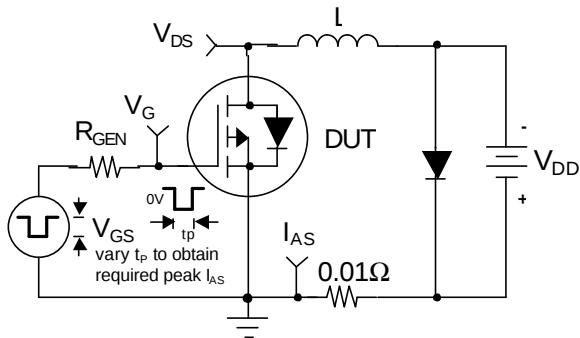


Figure 14. Unclamped Inductive Load Test Circuit

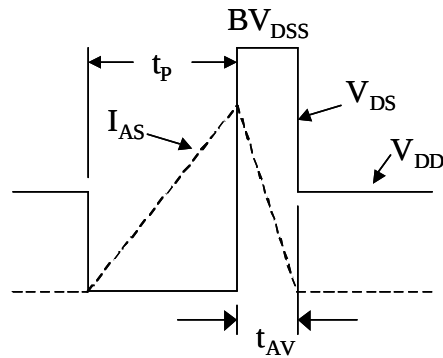


Figure 15. Unclamped Inductive Waveforms

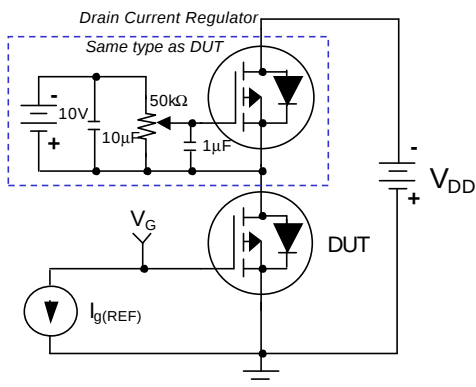


Figure 16. Gate Charge Test Circuit

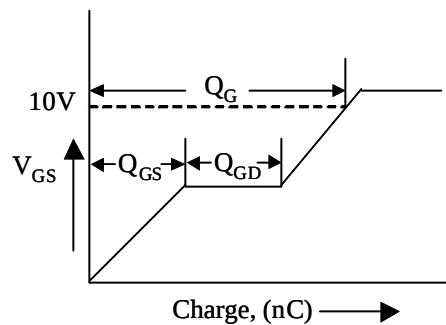


Figure 17. Gate Charge Waveform

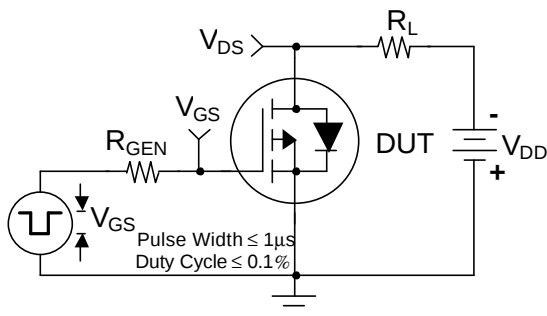


Figure 18. Switching Time Test Circuit

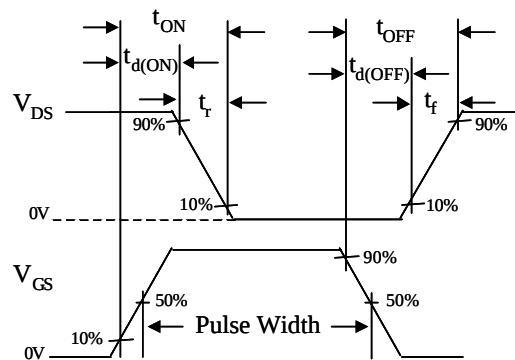
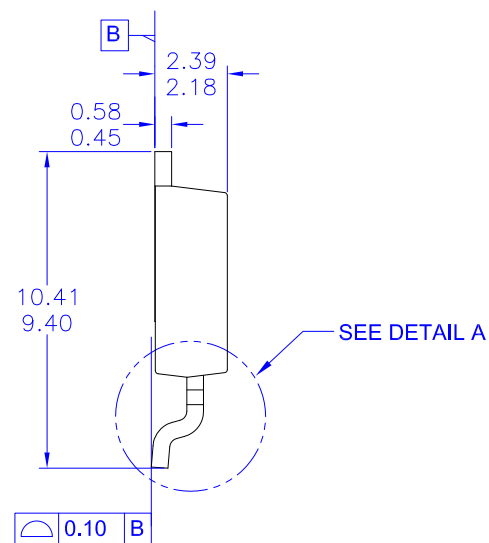
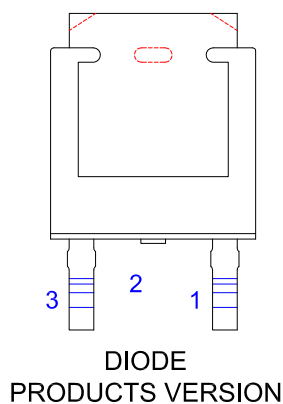
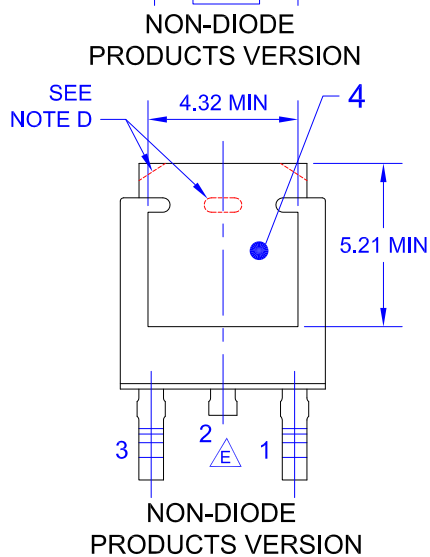
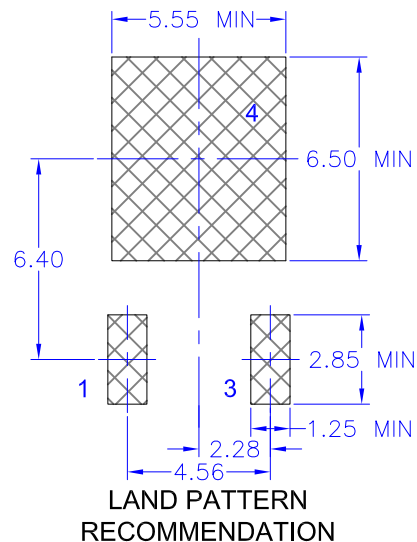
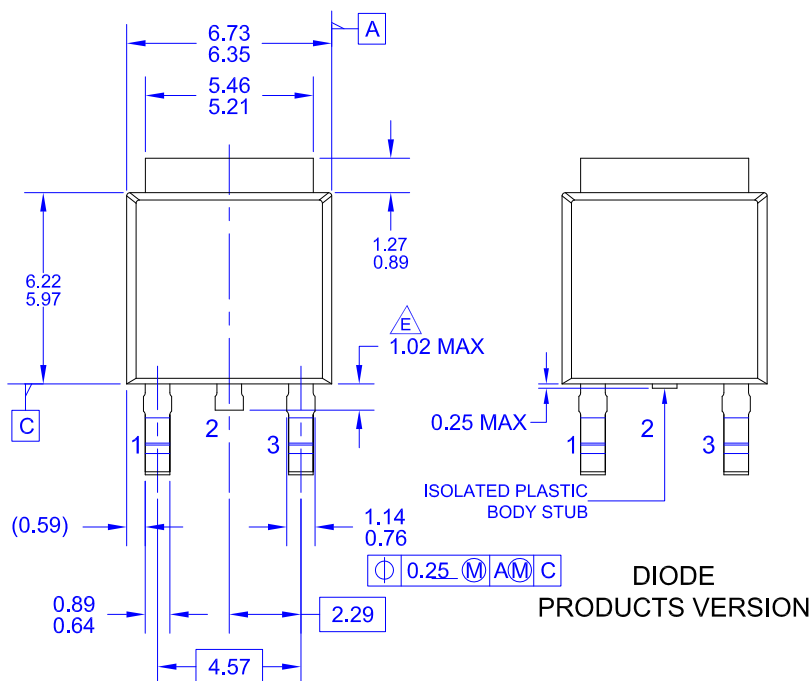
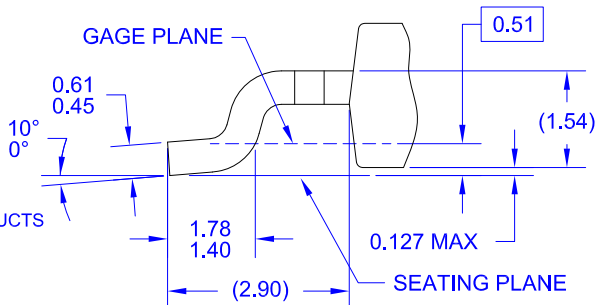


Figure 19. Switching Time Waveforms



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
- E) TRIMMED METAL CENTER LEAD IS PRESENT ON FOR NON-DIODE PRODUCTS
- F) DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
- H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV11



DETAIL A
(ROTATED -90°)
SCALE: 12X



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