

NTGS3136P, NVGS3136P

MOSFET – Power, Single, P-Channel, TSOP-6 -20 V, -5.8 A

Features

- Low $R_{DS(on)}$ in TSOP-6 Package
- 1.8 V Gate Rating
- Fast Switching
- NV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Optimized for Battery and Load Management Applications in Portable Equipment
- High Side Load Switch
- Switching Circuits for Game Consoles, Camera Phone, etc.

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	−20	V
Gate-to-Source Voltage			V_{GS}	± 8.0	V
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^{\circ}\text{C}$	I_D	−5.1	A
		$T_A = 85^{\circ}\text{C}$		−3.6	
	$t \leq 5 \text{ s}$	$T_A = 25^{\circ}\text{C}$		−5.8	
Power Dissipation (Note 1)	Steady State	$T_A = 25^{\circ}\text{C}$	P_D	1.25	W
	$t \leq 5 \text{ s}$			1.6	
Continuous Drain Current (Note 2)	Steady State	$T_A = 25^{\circ}\text{C}$	I_D	−3.7	A
		$T_A = 85^{\circ}\text{C}$		−2.7	
Power Dissipation (Note 2)	Steady State	$T_A = 25^{\circ}\text{C}$	P_D	0.7	W
Pulsed Drain Current		$t_p = 10 \mu\text{s}$	I_{DM}	−20	A
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to 150	$^{\circ}\text{C}$
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces)
2. Surface-mounted on FR4 board using the minimum recommended pad size (Cu area = 0.0775 in sq).

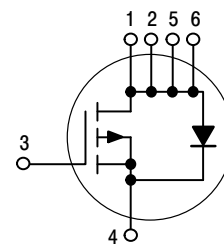


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$V_{(BR)DS}$	$R_{DS(ON)}$ TYP	I_D MAX
-20 V	25 m Ω @ -4.5 V	-5.1 A
	32 m Ω @ -2.5 V	-4.5 A
	41 m Ω @ -1.8 V	-2.5 A

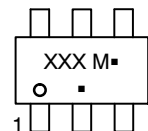
P-Channel



MARKING DIAGRAM



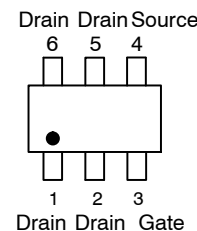
TSOP-6
CASE 318G
STYLE 1



XXX = Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

NTGS3136P, NVGS3136P

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	100	°C/W
Junction-to-Ambient – $t = 5$ s (Note 3)	$R_{\theta JA}$	77	
Junction-to-Ambient – Steady State (Note 4)	$R_{\theta JA}$	185	

3. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces)
4. Surface-mounted on FR4 board using the minimum recommended pad size (Cu area = 0.0775 in sq).

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0$ V, $I_D = -250$ μ A	-20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = -250$ μ A, Reference 25°C		-13		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0$ V, $V_{DS} = -20$ V			-1.0	μ A
					-5.0	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 8.0$ V			± 0.1	μ A

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = -250$ μ A	-0.4		-1.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			3		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = -4.5$ V, $I_D = -5.1$ A		25	33	m Ω
		$V_{GS} = -2.5$ V, $I_D = -4.5$ A		32	40	
		$V_{GS} = -1.8$ V, $I_D = -2.5$ A		41	51	
Forward Transconductance	g_{FS}	$V_{DS} = -5.0$ V, $I_D = -5.1$ A		22		S

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0$ V, $f = 1$ MHz, $V_{DS} = -10$ V		1901		pF
Output Capacitance	C_{OSS}			274		
Reverse Transfer Capacitance	C_{RSS}			175		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -4.5$ V, $V_{DS} = -10$ V; $I_D = -5.1$ A		18	29	nC
Threshold Gate Charge	$Q_{G(TH)}$			0.7		
Gate-to-Source Charge	Q_{GS}			2.4		
Gate-to-Drain Charge	Q_{GD}			4.3		
Gate Resistance	R_G			7.6		Ω

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -4.5$ V, $V_{DD} = -10$ V, $I_D = -1.0$ A, $R_G = 6.0$ Ω		9	19	ns
Rise Time	T_r			9	19	
Turn-Off Delay Time	$t_{d(OFF)}$			99	160	
Fall Time	T_f			48	79	

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0$ V, $I_S = -1.7$ A	$T_J = 25^\circ\text{C}$		-0.7	-1.2	V
			$T_J = 125^\circ\text{C}$		-0.6		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0$ V, $dI_S/dt = 100$ A/ μ s, $I_S = -1.7$ A			37	60	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: pulse width ≤ 300 μ s, duty cycle $\leq 2\%$
6. Switching characteristics are independent of operating junction temperatures

NTGS3136P, NVGS3136P

TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

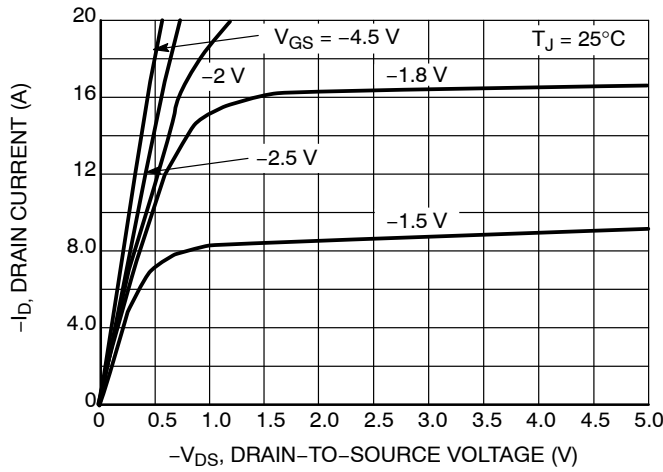


Figure 1. On-Region Characteristics

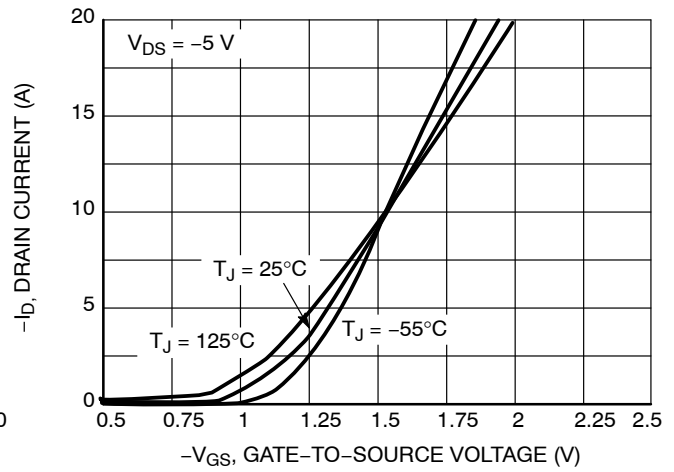


Figure 2. Transfer Characteristics

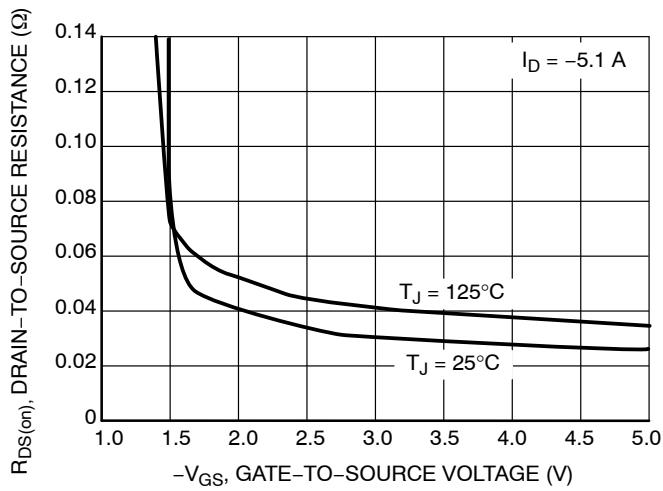


Figure 3. On-Resistance vs. Gate-to-Source Voltage

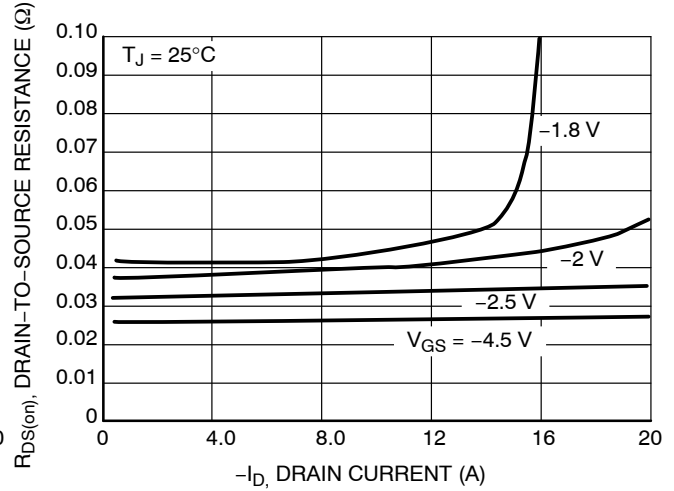


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

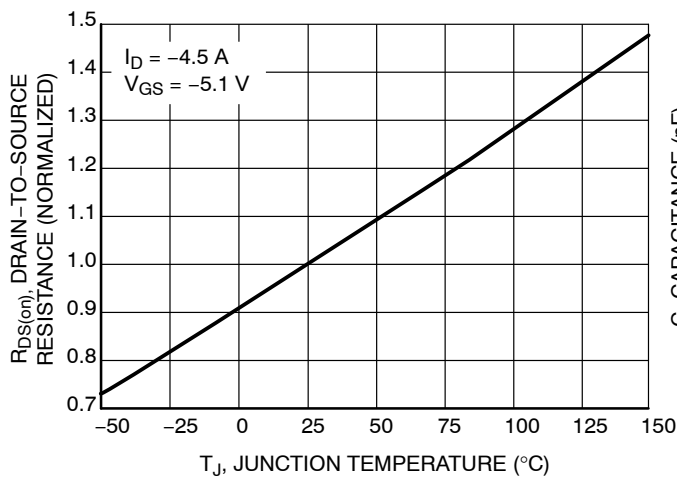


Figure 5. On-Resistance Variation with Temperature

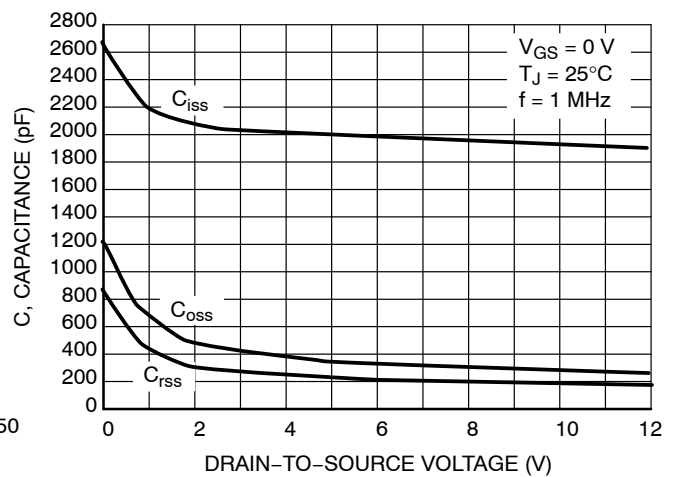


Figure 6. Capacitance Variation

NTGS3136P, NVGS3136P

TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

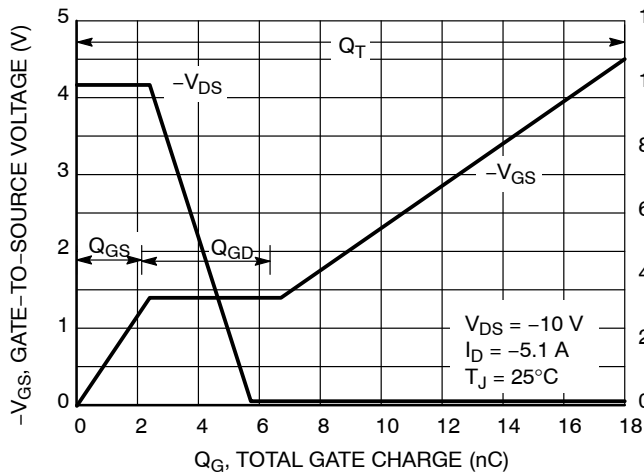


Figure 7. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

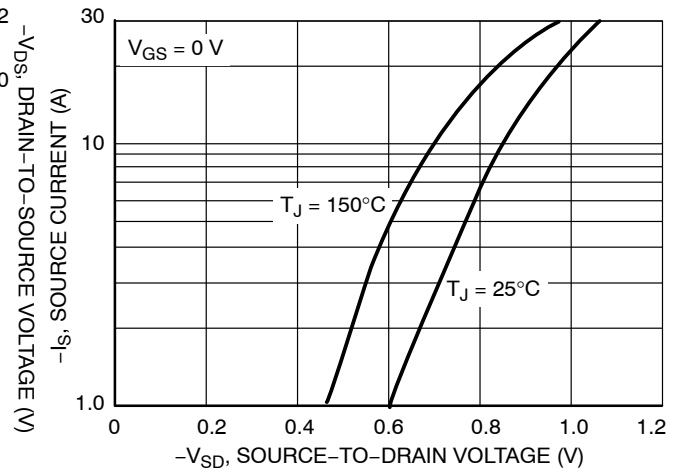


Figure 8. Diode Forward Voltage vs. Current

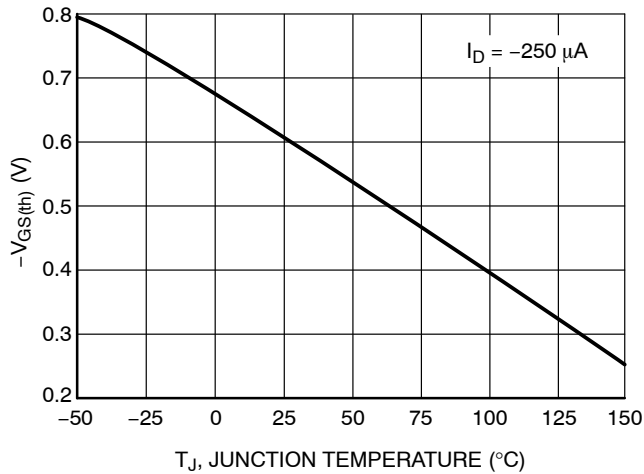


Figure 9. Threshold Voltage

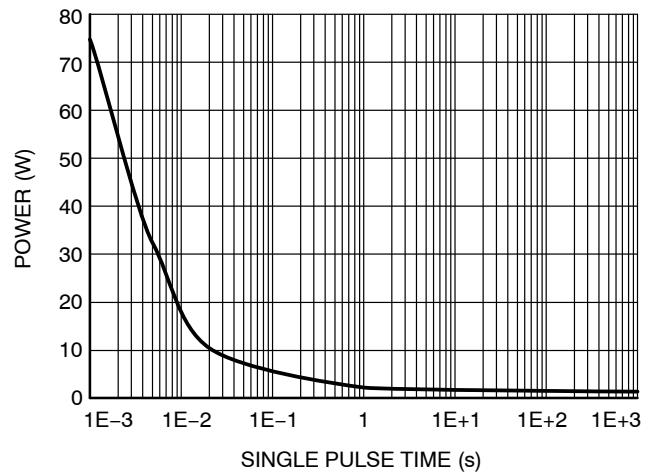


Figure 10. Single Pulse Maximum Power Dissipation

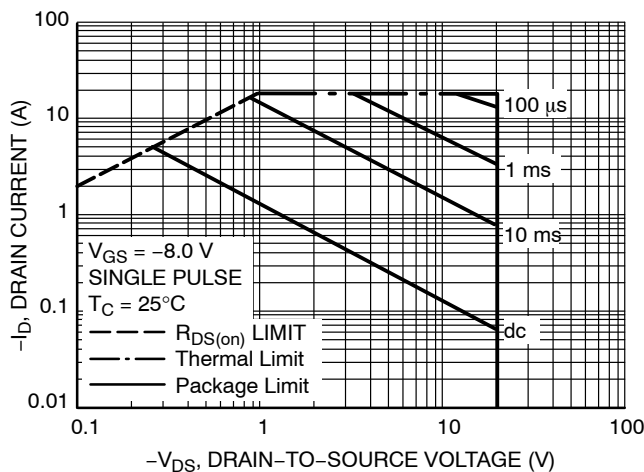


Figure 11. Maximum Rated Forward Biased Safe Operating Area

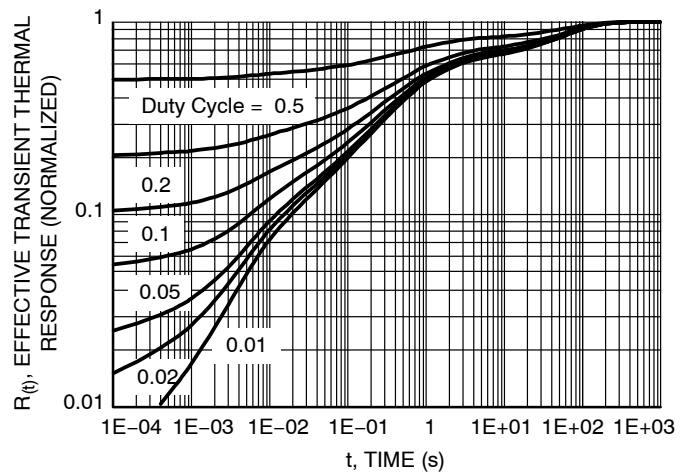


Figure 12. FET Thermal Response

NTGS3136P, NVGS3136P

ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NTGS3136PT1G	SD	TSOP-6 (Pb-Free)	3000 / Tape & Reel
NVGS3136PT1G*	VSD		

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



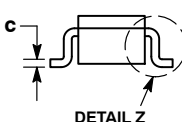
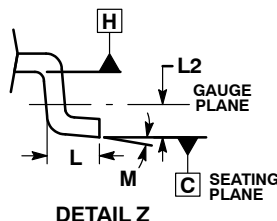
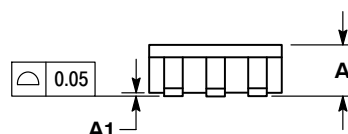
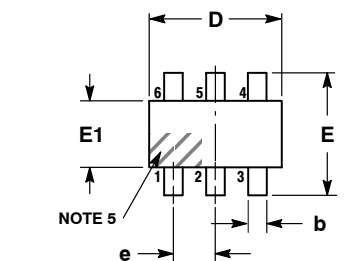
SCALE 2:1

TSOP-6

CASE 318G-02

ISSUE V

DATE 12 JUN 2012



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	—	10°

STYLE 1:

- PIN 1. DRAIN
- PIN 2. DRAIN
- PIN 3. GATE
- PIN 4. SOURCE
- PIN 5. DRAIN
- PIN 6. DRAIN

STYLE 2:

- PIN 1. EMITTER 2
- PIN 2. BASE 1
- PIN 3. COLLECTOR 1
- PIN 4. EMITTER 1
- PIN 5. BASE 2
- PIN 6. COLLECTOR 2

STYLE 3:

- PIN 1. ENABLE
- PIN 2. N/C
- PIN 3. R BOOST
- PIN 4. Vz
- PIN 5. V in
- PIN 6. V out

STYLE 4:

- PIN 1. N/C
- PIN 2. V in
- PIN 3. NOT USED
- PIN 4. GROUND
- PIN 5. ENABLE
- PIN 6. LOAD

STYLE 5:

- PIN 1. EMITTER 2
- PIN 2. BASE 2
- PIN 3. COLLECTOR 1
- PIN 4. EMITTER 1
- PIN 5. BASE 1
- PIN 6. COLLECTOR 2

STYLE 6:

- PIN 1. COLLECTOR
- PIN 2. COLLECTOR
- PIN 3. BASE
- PIN 4. EMITTER
- PIN 5. COLLECTOR
- PIN 6. COLLECTOR

STYLE 7:

- PIN 1. COLLECTOR
- PIN 2. COLLECTOR
- PIN 3. BASE
- PIN 4. N/C
- PIN 5. COLLECTOR
- PIN 6. EMITTER

STYLE 8:

- PIN 1. Vbus
- PIN 2. D(in)
- PIN 3. D(in)+
- PIN 4. D(out)+
- PIN 5. D(out)
- PIN 6. GND

STYLE 9:

- PIN 1. LOW VOLTAGE GATE
- PIN 2. DRAIN
- PIN 3. SOURCE
- PIN 4. DRAIN
- PIN 5. DRAIN
- PIN 6. HIGH VOLTAGE GATE

STYLE 10:

- PIN 1. D(OUT)+
- PIN 2. GND
- PIN 3. D(OUT)-
- PIN 4. D(IN)-
- PIN 5. VBUS
- PIN 6. D(IN)+

STYLE 11:

- PIN 1. SOURCE 1
- PIN 2. DRAIN 2
- PIN 3. DRAIN 2
- PIN 4. SOURCE 2
- PIN 5. GATE 1
- PIN 6. DRAIN 1/GATE 2

STYLE 12:

- PIN 1. I/O
- PIN 2. GROUND
- PIN 3. I/O
- PIN 4. I/O
- PIN 5. VCC
- PIN 6. I/O

STYLE 13:

- PIN 1. GATE 1
- PIN 2. SOURCE 2
- PIN 3. GATE 2
- PIN 4. DRAIN 2
- PIN 5. SOURCE 1
- PIN 6. DRAIN 1

STYLE 14:

- PIN 1. ANODE
- PIN 2. SOURCE
- PIN 3. GATE
- PIN 4. CATHODE/DRAIN
- PIN 5. CATHODE/DRAIN
- PIN 6. CATHODE/DRAIN

STYLE 15:

- PIN 1. ANODE
- PIN 2. SOURCE
- PIN 3. GATE
- PIN 4. DRAIN
- PIN 5. N/C
- PIN 6. CATHODE

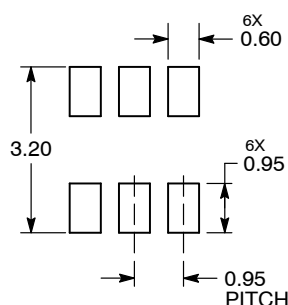
STYLE 16:

- PIN 1. ANODE/CATHODE
- PIN 2. BASE
- PIN 3. EMITTER
- PIN 4. COLLECTOR
- PIN 5. ANODE
- PIN 6. CATHODE

STYLE 17:

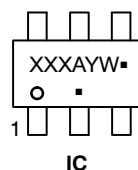
- PIN 1. EMITTER
- PIN 2. BASE
- PIN 3. ANODE/CATHODE
- PIN 4. ANODE
- PIN 5. CATHODE
- PIN 6. COLLECTOR

RECOMMENDED SOLDERING FOOTPRINT*

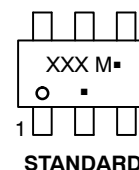


DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



IC



STANDARD

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb-Free Package

XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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