

FDBL86062-F085

N-Channel POWERTRENCH[®] MOSFET

100 V, 300 A, 2.0 m Ω

Features

- Typical $R_{DS(on)}$ = 1.5 m Ω at V_{GS} = 10 V, I_D = 80 A
- Typical $Q_{g(tot)}$ = 95 nC at V_{GS} = 10 V, I_D = 80 A
- UIS Capability
- Qualified to AEC Q101
- This Device is Pb-Free and is RoHS Compliant

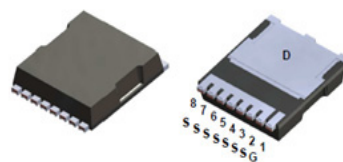
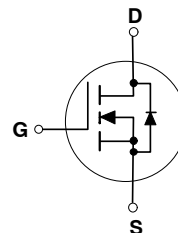
Applications

- Automotive Engine Control
- PowerTrain Management
- Solenoid and Motor Drivers
- Integrated Starter/Alternator
- Primary Switch for 12 V Systems



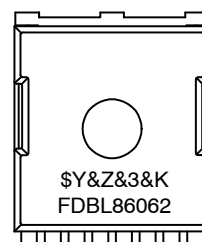
ON Semiconductor[®]

www.onsemi.com



**H-PSOF8L 11.68x9.80
CASE 100CU**

MARKING DIAGRAM



\$Y	= ON Semiconductor Logo
&Z&3	= Data Code (Year & Week)
&K	= Lot
FDBL86062	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FDBL86062–F085

MOSFET MAXIMUM RATINGS $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Rating	Units
V_{DS}	Drain-to-Source Voltage	100	V
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D	Drain Current - Continuous ($V_{GS} = 10$) (Note 1)	$T_C = 25^\circ\text{C}$	A
	Pulsed Drain Current	$T_C = 25^\circ\text{C}$	
E_{AS}	Single Pulse Avalanche Energy (Note 2)	352	mJ
P_D	Power Dissipation	429	W
	Derate Above 25°C	2.9	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature	-55 to $+175$	$^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.35	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient (Note 3)	43	$^\circ\text{C}/\text{W}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Current is limited by silicon.
- Starting $T_J = 25^\circ\text{C}$, $L = 0.1$ mH, $I_{AS} = 84$ A, $V_{DD} = 100$ V during inductor charging and $V_{DD} = 0$ V during time in avalanche.
- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2oz copper.

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDBL86062	FDBL86062–F085	MO–299A	13"	24 mm	2000 Units

ELECTRICAL CHARACTERISTICS $T_J = 25^\circ\text{C}$, unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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OFF CHARACTERISTICS

B_{VDS}	Drain-to-Source Breakdown Voltage	$I_D = 250 \mu\text{A}$, $V_{GS} = 0$ V	100	–	–	V
I_{DSS}	Drain-to-Source Leakage Current	$V_{DS} = 100$ V, $V_{GS} = 0$ V	$T_J = 25^\circ\text{C}$	–	–	5 μA
			$T_J = 175^\circ\text{C}$ (Note 4)	–	–	2 mA
I_{GSS}	Gate-to-Source Leakage Current	$V_{GS} = \pm 20$ V	–	–	± 100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250 \mu\text{A}$	2.0	3.1	4.5	V
$R_{DS(on)}$	Drain to Source On Resistance	$I_D = 80$ A, $V_{GS} = 10$ V	$T_J = 25^\circ\text{C}$	–	1.5	2.0 m Ω
			$T_J = 175^\circ\text{C}$ (Note 4)	–	3.3	4.3

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 50$ V, $V_{GS} = 0$ V, $f = 1$ MHz	–	6970	–	pF
C_{oss}	Output Capacitance		–	3950	–	
C_{rss}	Reverse Transfer Capacitance		–	29	–	
R_g	Gate Resistance	$f = 1$ MHz	–	0.4	–	Ω
$Q_{g(ToT)}$	Total Gate Charge at 10 V	$V_{GS} = 0$ to 10 V	$V_{DD} = 80$ V $I_D = 80$ A	–	95	nC
$Q_{g(th)}$	Threshold Gate Charge	$V_{GS} = 0$ to 2 V		–	13	
Q_{gs}	Gate-to-Source Gate Charge			–	31	
Q_{gd}	Gate-to-Drain "Miller" Charge			–	20	

FDBL86062–F085

ELECTRICAL CHARACTERISTICS (continued) $T_J = 25^\circ\text{C}$, unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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SWITCHING CHARACTERISTICS

t_{on}	Turn-On Time	$V_{DD} = 50\text{ V}$, $I_D = 80\text{ A}$, $V_{GS} = 10\text{ V}$, $R_{GEN} = 6\ \Omega$	–	–	73	ns
$t_{d(on)}$	Turn-On Delay		–	31	–	
t_r	Rise Time		–	25	–	
$t_{d(off)}$	Turn-Off Delay		–	36	–	
t_f	Fall Time		–	9	–	
t_{off}	Turn-Off Time		–	–	59	

DRAIN–SOURCE DIODE CHARACTERISTICS

V_{SD}	Source-to-Drain Diode Voltage	$I_{SD} = 80\text{ A}$, $V_{GS} = 0\text{ V}$	–	–	1.25	V
		$I_{SD} = 40\text{ A}$, $V_{GS} = 0\text{ V}$	–	–	1.2	
t_{rr}	Reverse-Recovery Time	$I_F = 80\text{ A}$, $dI_{SD}/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 80\text{ V}$	–	115	150	ns
Q_{rr}	Reverse-Recovery Charge		–	172	224	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at $T_J = 175^\circ\text{C}$. Product is not tested to this condition in production.

TYPICAL CHARACTERISTICS

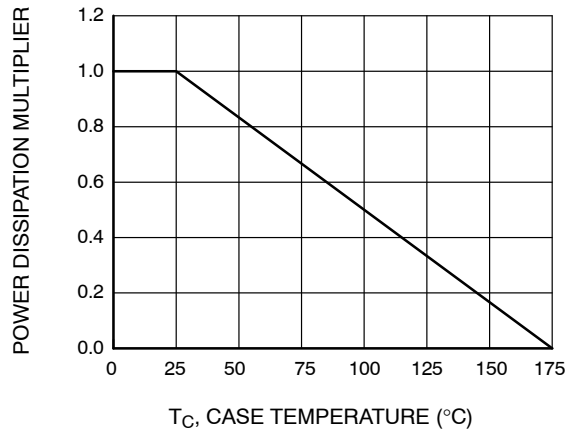


Figure 1. Normalized Power Dissipation vs. Case Temperature

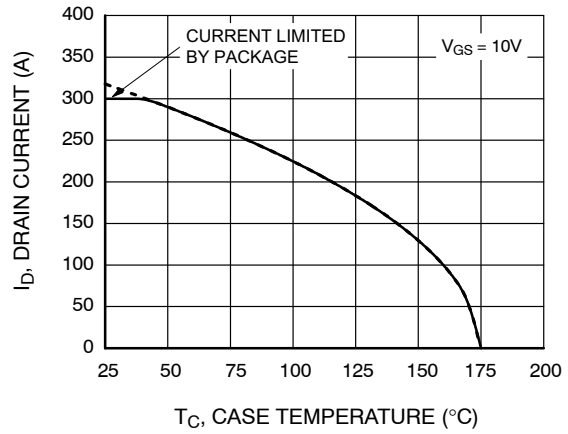


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

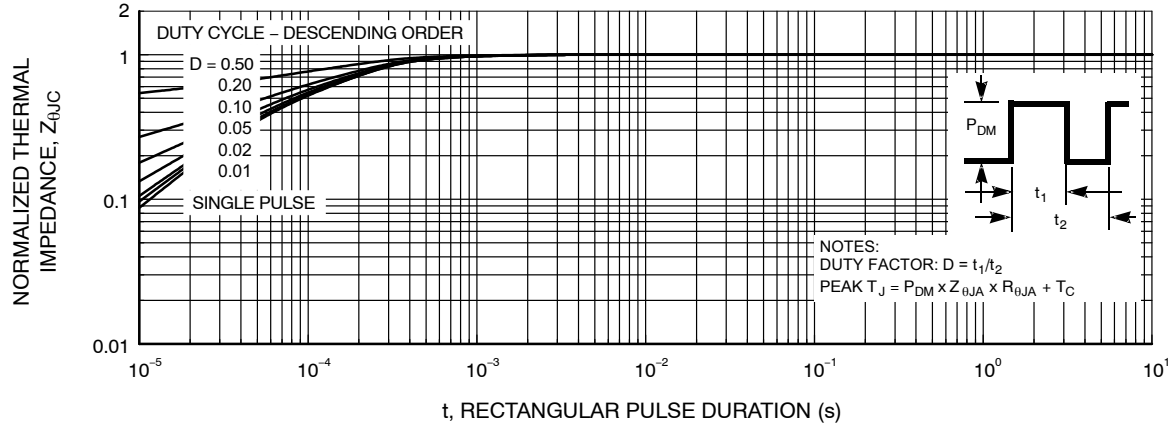


Figure 3. Normalized Maximum Transient Thermal Impedance

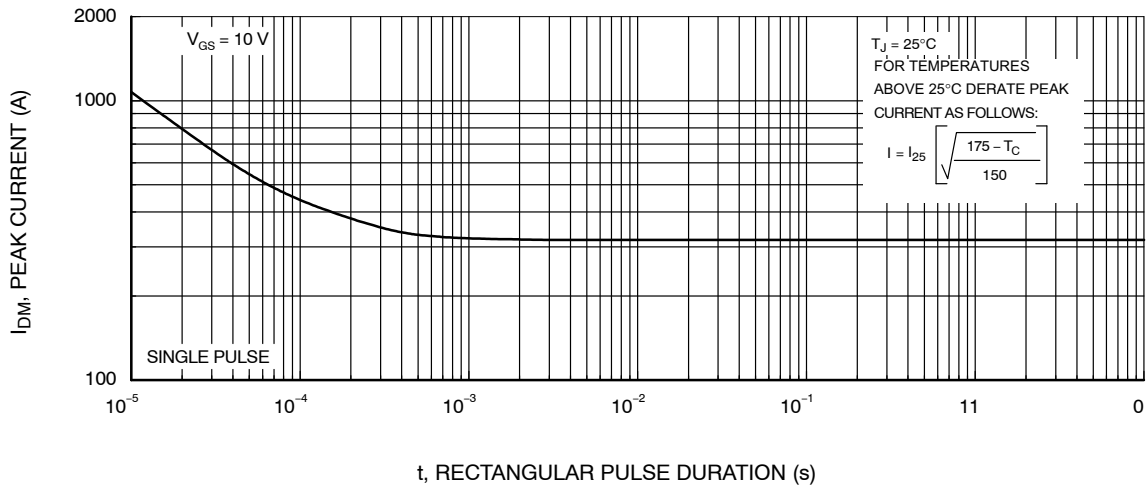


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS (continued)

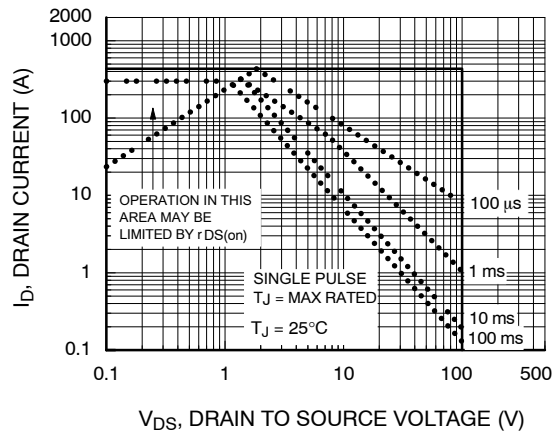
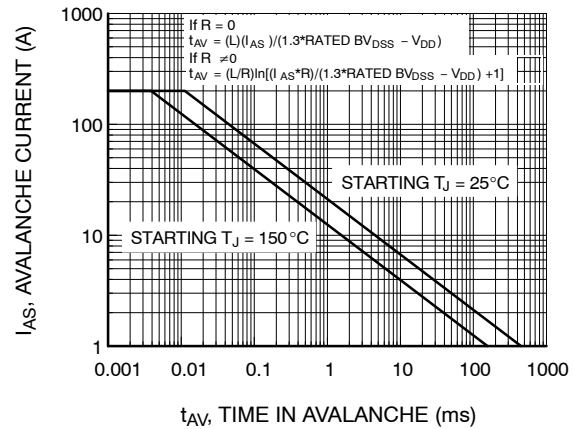


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to ON Semiconductor Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

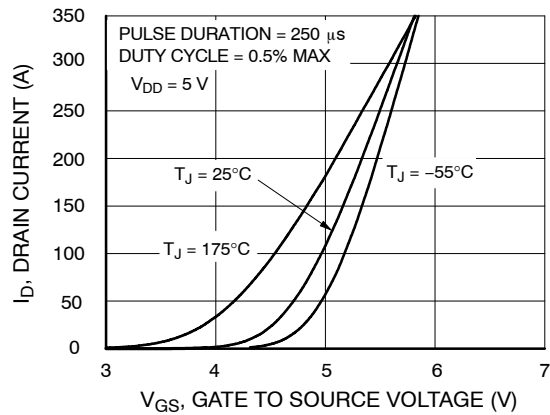


Figure 7. Transfer Characteristics

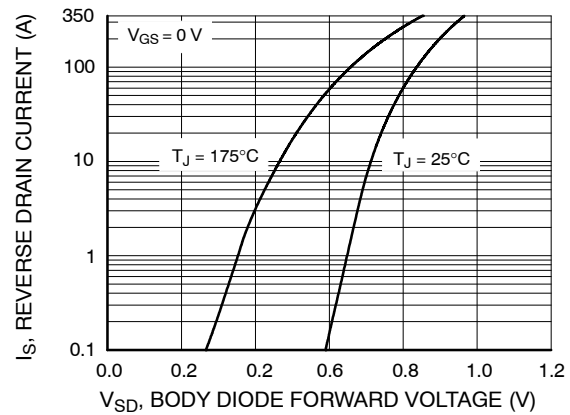


Figure 8. Forward Diode Characteristics

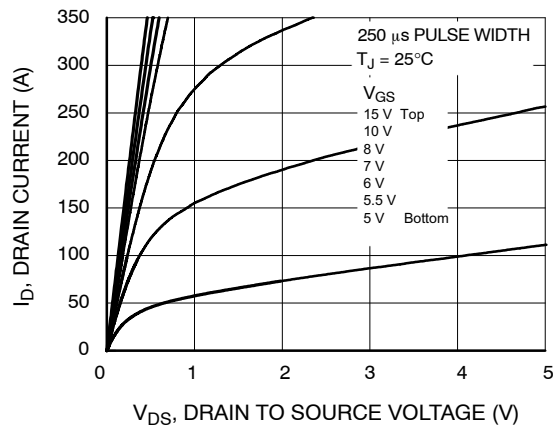


Figure 9. Saturation Characteristics

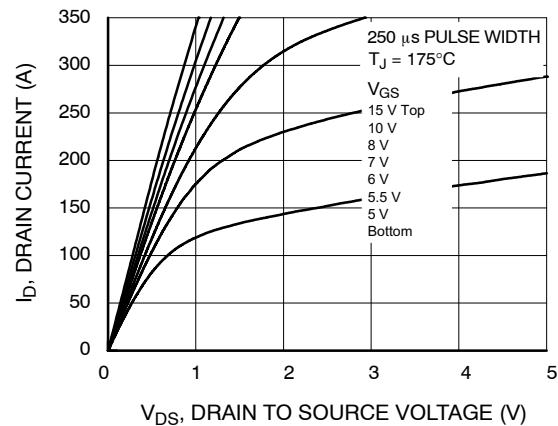


Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS (continued)

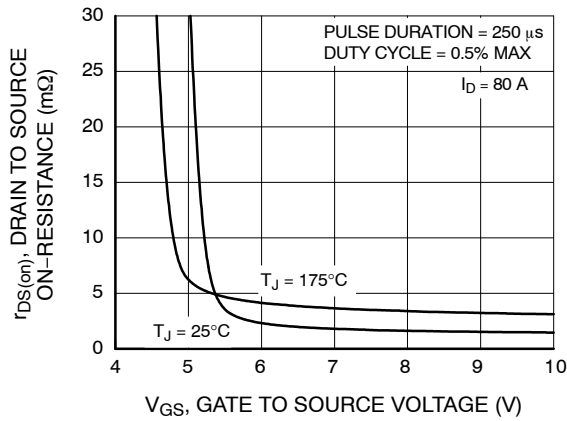


Figure 11. $R_{DS(on)}$ vs. Gate Voltage

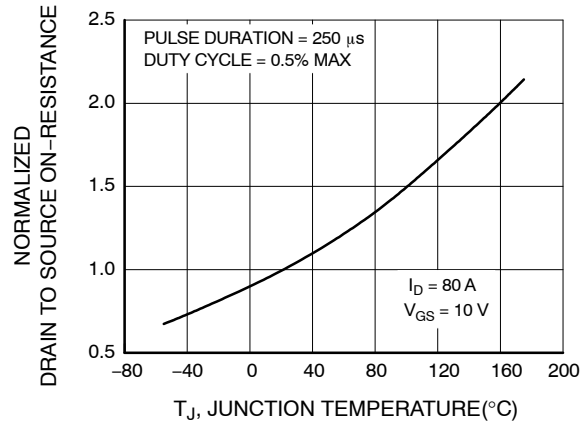


Figure 12. Normalized $R_{DS(on)}$ vs. Junction Temperature

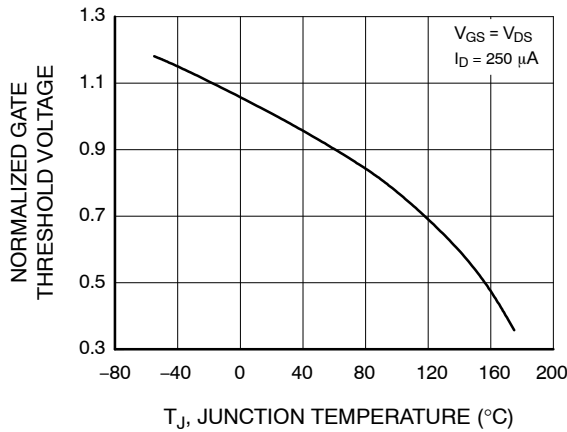


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

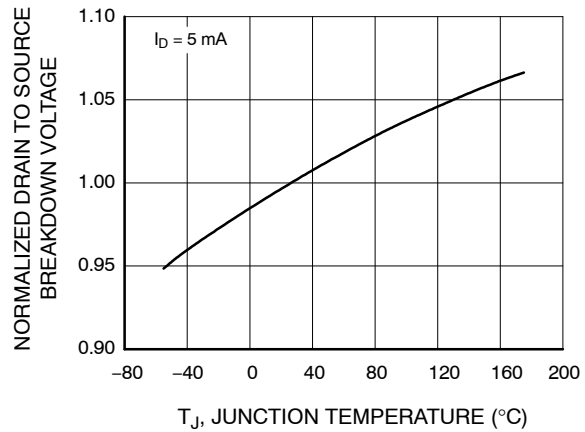


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

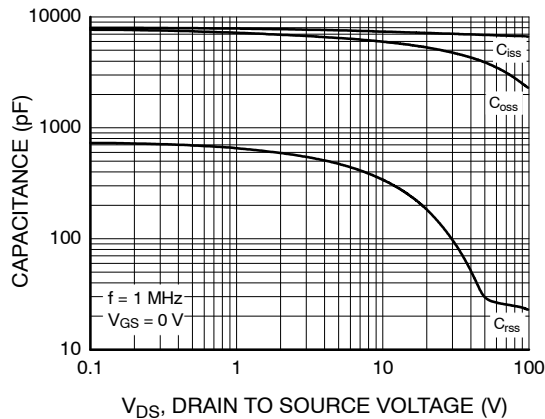


Figure 15. Capacitance vs. Drain to Source Voltage

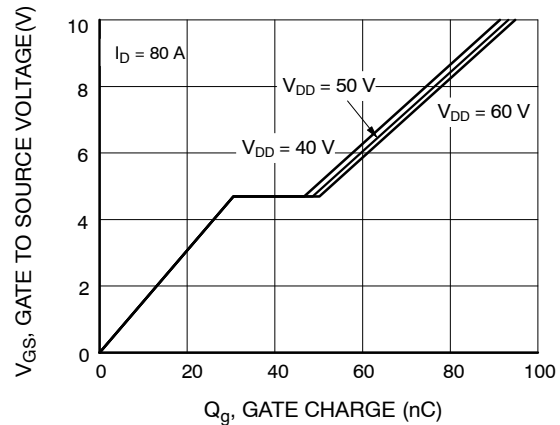


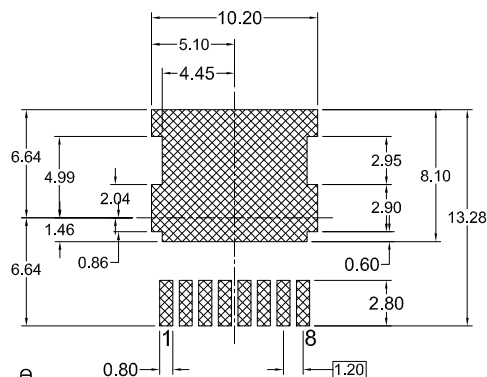
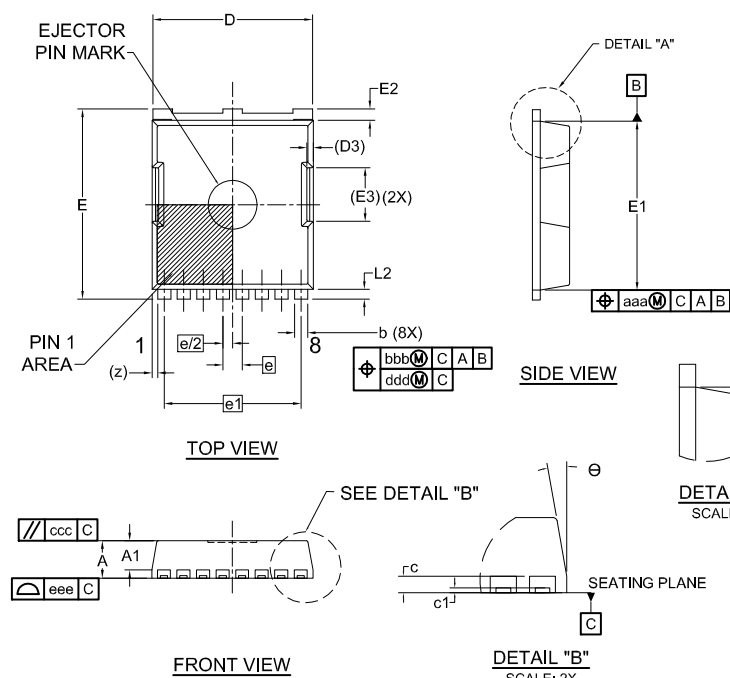
Figure 16. Gate Charge vs. Gate to Source Voltage

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



H-PSOF8L 11.68x9.80 CASE 100CU ISSUE B

DATE 20 MAY 2022

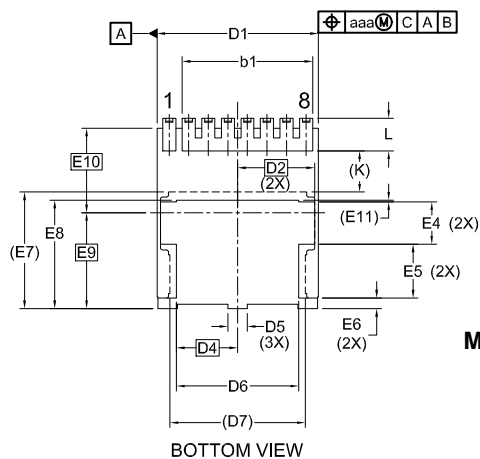


LAND PATTERN RECOMMENDATION

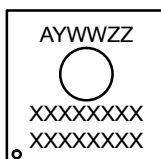
*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

NOTES:

1. PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE A.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
3. CONTROLLING DIMENSION: MILLIMETERS.
4. COPLANARITY APPLIES TO THE EXPOSED WELL AS THE TERMINALS.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



GENERIC MARKING DIAGRAM*



A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code
XXXX = Specific Device Code

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	8.00 REF		
c	0.40	0.50	0.60
c1	0.10	---	---
D	9.70	9.80	9.90
D1	9.80	9.90	10.00
D2	4.73 BSC		
D3	0.40 REF		
D4	3.75 BSC		
D5	---	1.20	---
D6	7.40	7.50	7.60
D7	8.30 REF		
E	11.58	11.68	11.78
E1	10.28	10.38	10.48
E2	0.60	0.70	0.80
E3	3.30 REF		
E4	---	2.60	---
E5	---	3.30	---

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
E6	---	0.65	---
E7	7.15 REF		
E8	6.55	6.65	6.75
E9	5.89 BSC		
E10	5.19 BSC		
E11	0.10 REF		
e	1.20 BSC		
e/2	0.60 BSC		
e1	8.40 BSC		
K	2.43	2.53	2.63
L	1.90	2.00	2.10
L2	0.50	0.60	0.70
z	0.35 REF		
θ	0°	---	12°
aaa	0.20		
bbb	0.25		
ccc	0.20		
ddd	0.20		
eee	0.10		

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "μ", may or may not be present. Some products may not follow the Generic Marking.

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