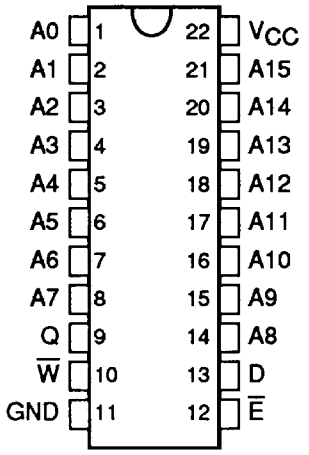
TMS6787
65,536-BIT HIGH-SPEED STATIC RANDOM-ACCESS MEMORY

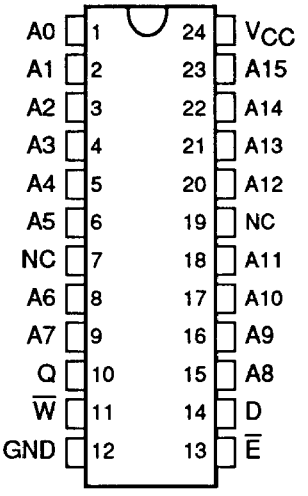
APRIL 1989–REVISED JANUARY 1990

- **Organization . . . 65,536 x 1**
- **Single 5-V Power Supply (10% Tolerance)**
- **High-Density 22-Pin and 24-Pin Packages**
- **All Inputs/Outputs Fully TTL Compatible**
- **Max Access/Min Cycle Time**
  TMS6787-15 . . . 15 ns
  TMS6787-20 . . . 20 ns
  TMS6787-25 . . . 25 ns
  TMS6787-30 . . . 30 ns
- **Power-Saving BiCMOS Technology**
- **3-State Output Buffers**
- **Low Power Dissipation (V_{CC} = 5.5 V)**
  TMS6787-15, TMS6787-20:
  — Active . . . 550 mW Worst Case
  — Standby . . . 55 mW Worst Case (CMOS Input Levels)
  — Standby . . . 165 mW Worst Case (TTL Input Levels)
- **Low Power Dissipation (V_{CC} = 5.5 V)**
  TMS6787-25, TMS6787-30:
  — Active . . . 550 mW Worst Case
  — Standby . . . 110 mW Worst Case (CMOS Input Levels)
  — Standby . . . 220 mW Worst Case (TTL Input Levels)

N PACKAGE
(TOP VIEW)



DJ PACKAGE†
(TOP VIEW)



†The DJ package is for TMS6787-15 and TMS6787-20 only.

description

The TMS6787 is a separate I/O, 65,536-bit, high-speed, static random-access memory organized as 65,536 words by 1 bit. The TMS6787 features maximum address access and minimum cycle times of 15 ns, 20 ns, 25 ns, and 30 ns.

The TMS6787 is fabricated using BiCMOS technology. The TMS6787-15 and TMS6787-20 have maximum power dissipation as low as 550 mW active. This reduces to a maximum of 55 mW (CMOS-input levels) and 165 mW (TTL-input levels) during standby operation. The TMS6787-25 and TMS6787-30 have maximum power dissipation as low as 550 mW active. This reduces to a maximum of 110 mW (CMOS-input levels) and 220 mW (TTL-input levels) during standby operation.

PIN NOMENCLATURE	
A0-A15	Address Inputs
D	Data In
$\overline{E}$	Chip Enable
NC	No Connect
GND	Ground
Q	Data Out
V_{CC}	5-V Power Supply
$\overline{W}$	Write Enable

TEXAS INSTRUMENTS
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All inputs and outputs are compatible with Series 54/74 TTL circuits without the use of external pull-up resistors. Each output can drive one Series 54/74 TTL circuit without external resistors. The data outputs are three-state for connecting multiple devices to a common bus.

The TMS6787-15, TMS6787-20, TMS6787-25, and TMS6787-30 are offered in a 300-mil, 22-pin plastic dual-in-line packages (N suffix). The TMS6787-15 and TMS6787-20 are offered in and a 24-pin plastic small outline J-lead packages (DJ suffix). Both are characterized for operation from 0°C to 70°C.

operation

addresses (A0-A15)

The 16 address lines select one of the 65,536 1-bit words in the RAM. The address inputs must be stable for the duration of a read or write cycle. The address inputs can be driven directly from standard Series 54/74 TTL without external pull-up resistors.

chip enable/powerdown ($\overline{E}$)

The chip enable/powerdown terminal ($\overline{E}$) can be driven directly by standard TTL circuits, and affects the powerdown/deselect function of a chip. When $\overline{E}$ is high, the device is put into a reduced power standby mode. Data is retained during the standby mode.

write enable ($\overline{W}$)

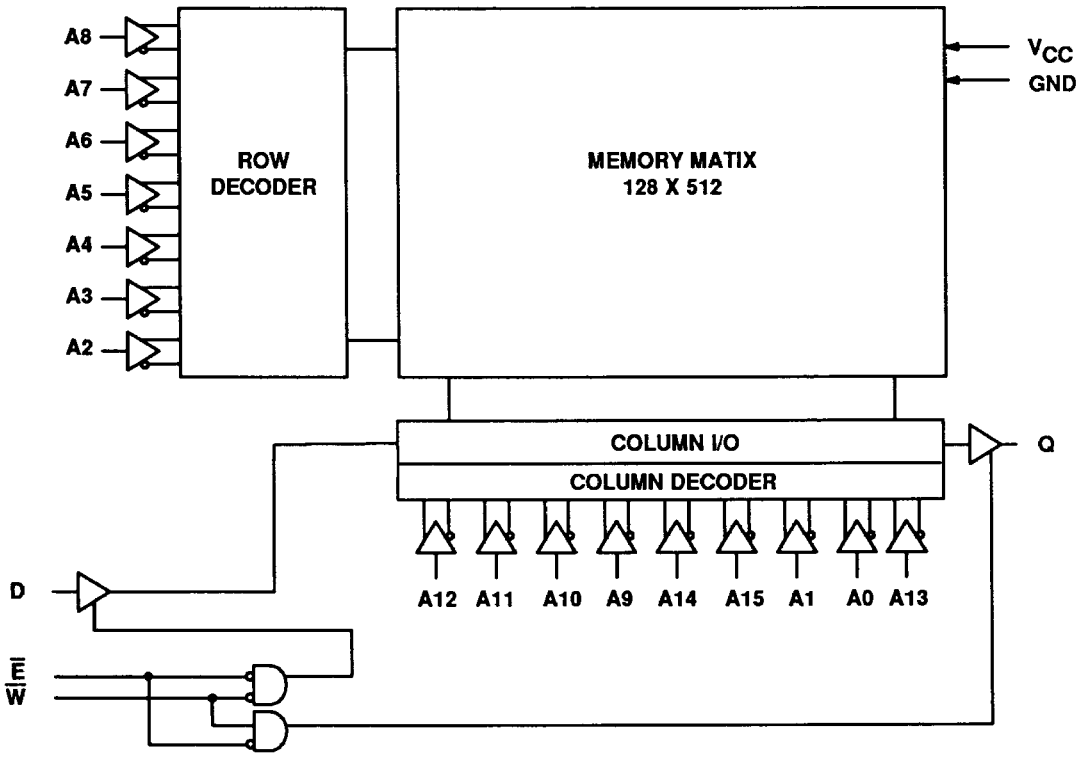
The read or write mode is selected through the write enable terminal ($\overline{W}$). A logic high selects the read mode; a logic low selects the write mode. $\overline{W}$ or $\overline{E}$ must be high when changing addresses to prevent inadvertently writing data into a memory location. The $\overline{W}$ input can be driven directly from standard TTL circuits.

function table

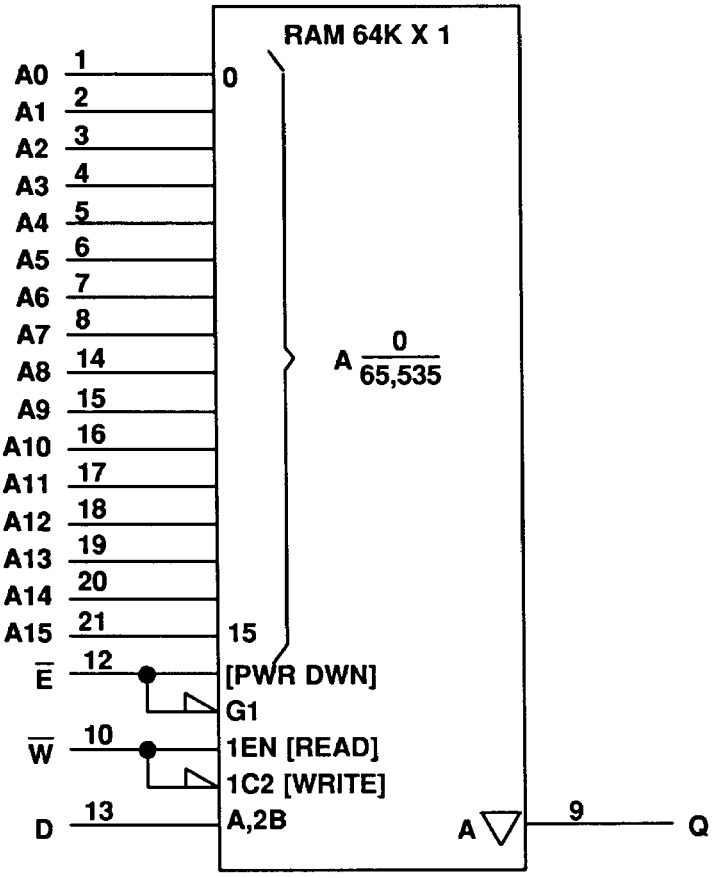
FUNCTION	MODE		
	Deselect	Read	Write
$\overline{W}$	X	H	L
$\overline{E}$	H	L	L
Q	HI-Z	D_{OUT}	HI-Z

X = Don't Care

functional block diagram



logic symbol†



†Symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range (see Note 1) . . . . . – 0.5 V to 7 V
Power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Temperature range powered down . . . . . – 10°C to 85°C
Storage temperature range . . . . . – 55°C to 125°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND terminal.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level Input voltage	2.2		6	V
V_{IL}	Low-level input voltage (see Note 2)	– 0.5		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The input voltage may go down to – 3.0 V for a maximum time interval of 10 ns for TMS6787-15 and TMS6787-20.
The input voltage may go down to – 3.0 V for a maximum time interval of 20 ns for TMS6787-25 and TMS6787-30.

electrical characteristics over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	TMS6787-15 TMS6787-20		TMS6787-25 TMS6787-30		UNIT
			MIN	MAX	MIN	MAX	
V_{OH}	High level output voltage	I_{OH} = – 4 mA	2.4		2.4		V
V_{OL}	Low level output voltage	I_{OL} = 8 mA ('6787-15 and '6787-25) I_{OL} = 16 mA ('6787-25 and '6787-30)		0.4		0.5	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_{in} = 0 to V_{CC}		2		2	µA
I_O	Output current (leakage)	$\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC}		10		2	µA
I_{CC1}	Operating power supply current	$\overline{E}$ = V_{IL}, $I_{i/o}$ = 0 mA		100		100	mA
I_{CC2}	Average operating current	Minimum cycle, Duty 100%, I_{out} = 0 mA		120		N/A	mA
$I_{CC(SB1)}$	Standby supply current (TTL levels)	$\overline{E}$ = V_{IH}		30		40	mA
$I_{CC(SB2)}$	Standby supply current (low-power CMOS levels)	$\overline{E}$ ≥ V_{CC} – 0.2 V, V_{in} ≤ 0.2 V or V_{in} ≥ V_{CC} – 0.2 V		10		20	mA

capacitance, T_A = 25°C, f = 1 MHz‡

PARAMETER		TEST CONDITIONS	TMS6787-15 TMS6787-20		TMS6787-25 TMS6787-30		UNIT
			MIN	MAX	MIN	MAX	
C_i	Input capacitance	V_{in} = 0 V		6		5	pF
C_o	Output capacitance	V_{out} = 0 V		10		7	pF

‡Capacitance measurements are made on a sample basis only.

timing requirements over recommended supply voltage range and operating temperature range (read cycle) (see Note 3)

		ALT. SYMBOL	TMS6787-15		TMS6787-20		TMS6787-25		TMS6787-30		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time	t_{RC}	15		20		25		30		ns

switching characteristics over full ranges of recommended operating conditions (read cycle) (see Note 3)

PARAMETER		ALT. SYMBOL	TMS6787-15		TMS6787-20		TMS6787-25		TMS6787-30		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	t_{AA}		15		20		25		30	ns
$t_{a(E)}$	Access time from $\overline{E}$	t_{ACS}		15		20		25		30	ns
$t_{en(E)}$	Output enable time from $\overline{E}$ (see Notes 4 and 5)	t_{LZ}	3		3		5		5		ns
$t_{dis(E)}$	Output disable time from $\overline{E}$ (see Notes 4 and 5)	t_{HZ}	0	6	0	8	0	15	0	15	ns
$t_{v(A)}$	Output data valid time after address change	t_{OH}	3		3		5		5		ns

NOTES: 3. Timing requirements and switching characteristics are defined under the following conditions:
Input pulse levels ..... GND to 3.0V
Input rise and fall time ..... 4 ns
Input timing reference level ..... 1.5 V
Output timing reference level ..... 1.5 V
Output load (including scope and jig) ..... see Figure 1
4. Transition is measured ± 200 mV from steady-state voltage with specified loading in Figure 1 Load B ('6787-15/'6787-20).
5. This parameter is sampled and not 100% tested.

timing requirements over recommended supply voltage range and operating temperature range (write cycle) (see Notes 3 and 7)

		ALT. SYMBOL	TMS6787-15		TMS6787-20		TMS6787-25		TMS6787-30		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(W)}$	Write cycle time (see Note 8)	t_{WC}	15		20		25		30		ns
$t_{su(A)}$	Address setup time	t_{AS}	0		0		0		0		ns
$t_{su(D)}$	Data setup time before write high	t_{DW}	12		15		20		25		ns
$t_{su(E)}$	Chip enable setup time	t_{CW}	10		15		20		25		ns
t_{AVWH}	Address valid time to write high	t_{AW}	10		15		20		25		ns
$t_{w(W)}$	Write pulse duration	t_{WP}	10		15		20		25		ns
$t_{rec(W)}$	Write recovery time	t_{WR}	3		3		5		5		ns
$t_{h(D)}$	Data hold time after write high	t_{DH}	0		0		0		0		ns
$t_{v(W)}$	Output data valid time after write high (see Notes 4, 5, and 6)	t_{OW}	0		0		0		0		ns

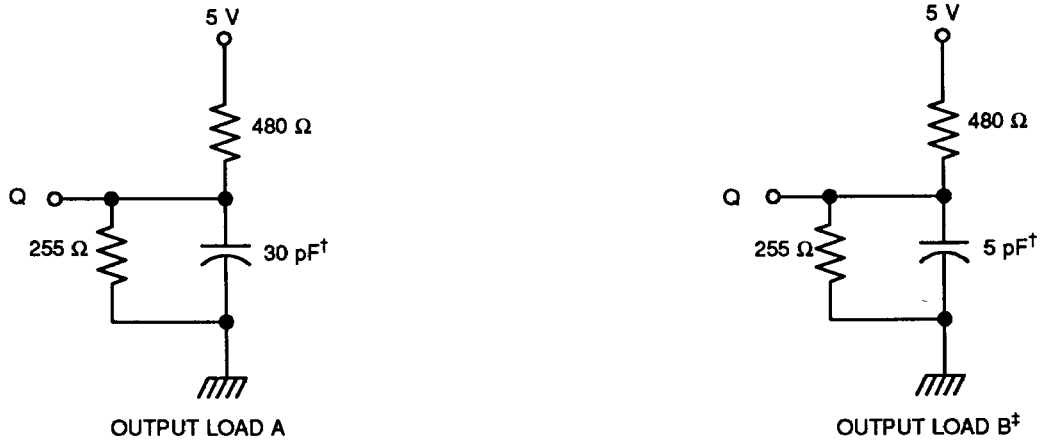
switching characteristics over full ranges of recommended operating conditions (write cycle) (see Note 3)

PARAMETER		ALT. SYMBOL	TMS6787-15		TMS6787-20		TMS6787-25		TMS6787-30		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{dis(W)}$	Output disable time from $\overline{W}$ (see Notes 4, 5, and 6)	t_{WZ}	0	6	0	8	0	15	0	15	ns

NOTES: 3. Timing requirements and switching characteristics are defined under the following conditions:
Input pulse levels ..... GND to 3.0 V
Input rise and fall time ..... 4 ns
Input timing reference level ..... 1.5 V
Output timing reference level ..... 1.5 V
Output load (including scope and jig) ..... see Figure 1

4. Transition is measured ± 200 mV from steady-state voltage with specified loading in Figure 1 Load B ('6787-15/'6787-20).
5. This parameter is sampled and not 100% tested.
6. Transition is measured ± 500 mV from steady-state voltage with specified loading in Figure 1 Load B ('6787-25/'6787-30).
7. If $\overline{E}$ goes high simultaneously with $\overline{W}$ high, the output remains in a high-impedance state.
8. All write cycle timings are referenced from the last valid address to the first transitioning address.

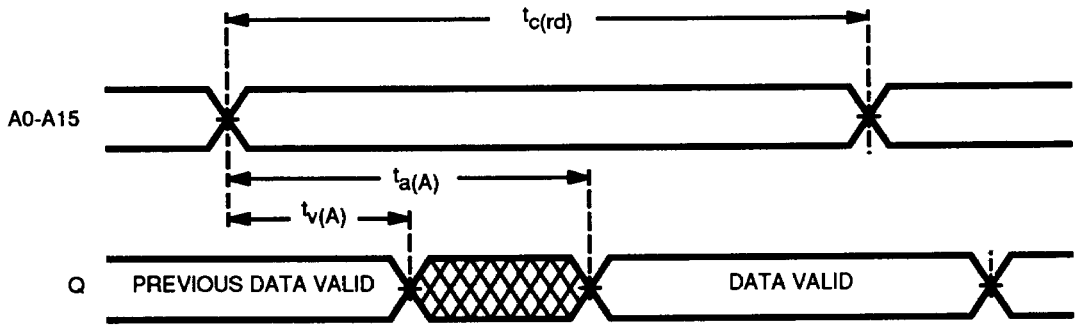
PARAMETER MEASUREMENT INFORMATION



†This value includes scope and jig capacitance.
‡This output load applies for $t_{dis(E)}$, $t_{en(E)}$, $t_{dis(W)}$, and $t_{v(W)}$.

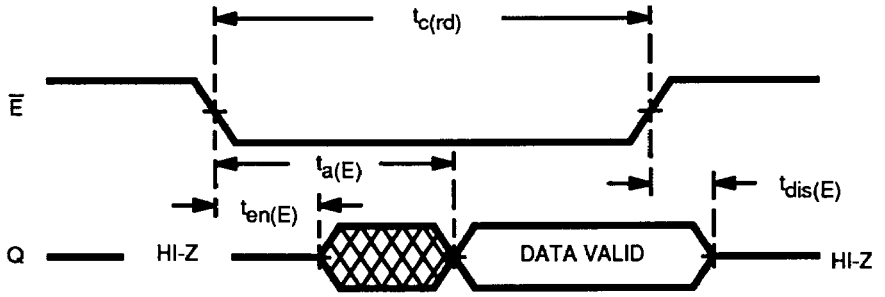
FIGURE 1. OUTPUT LOAD CIRCUIT

read cycle timing (type A)



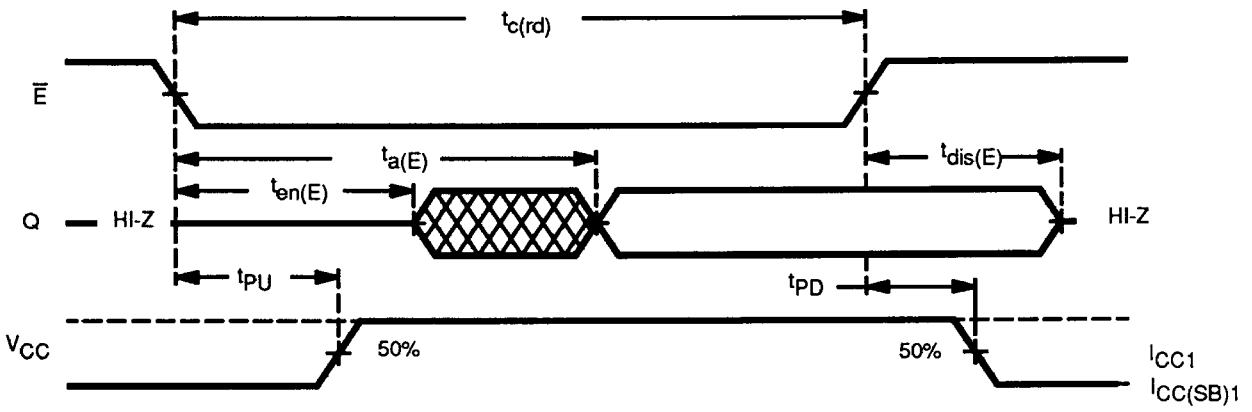
NOTES: 9. $\overline{W}$ is high $\overline{E}$ is low for read cycle.
10. Addresses are valid prior to or at the same time $\overline{E}$ goes low.

read cycle timing (type B)(TMS6787-15,TMS6787-20)



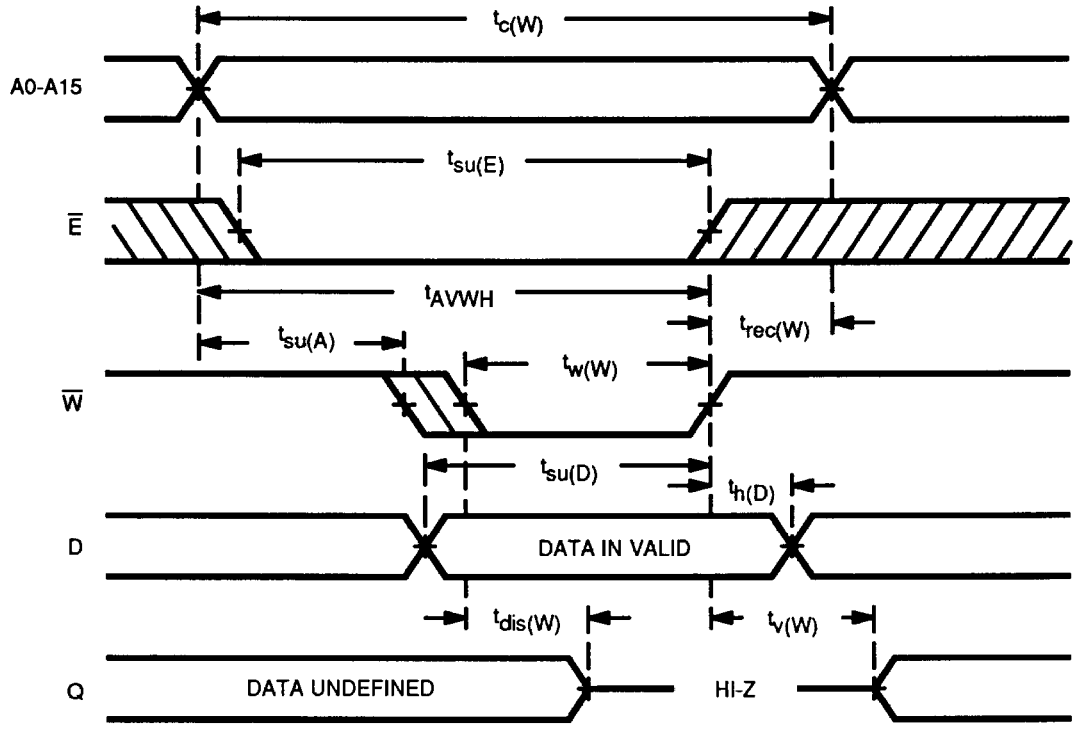
NOTES: 4. Transition is measured ± 200 mV from steady-state voltage with specified loading in Figure 1 Load B ('6787-15/'6787-20).
9. $\overline{W}$ is high and $\overline{E}$ is low for read cycle.

read cycle timing (type B) (TMS6787-25 and TMS6787-30)



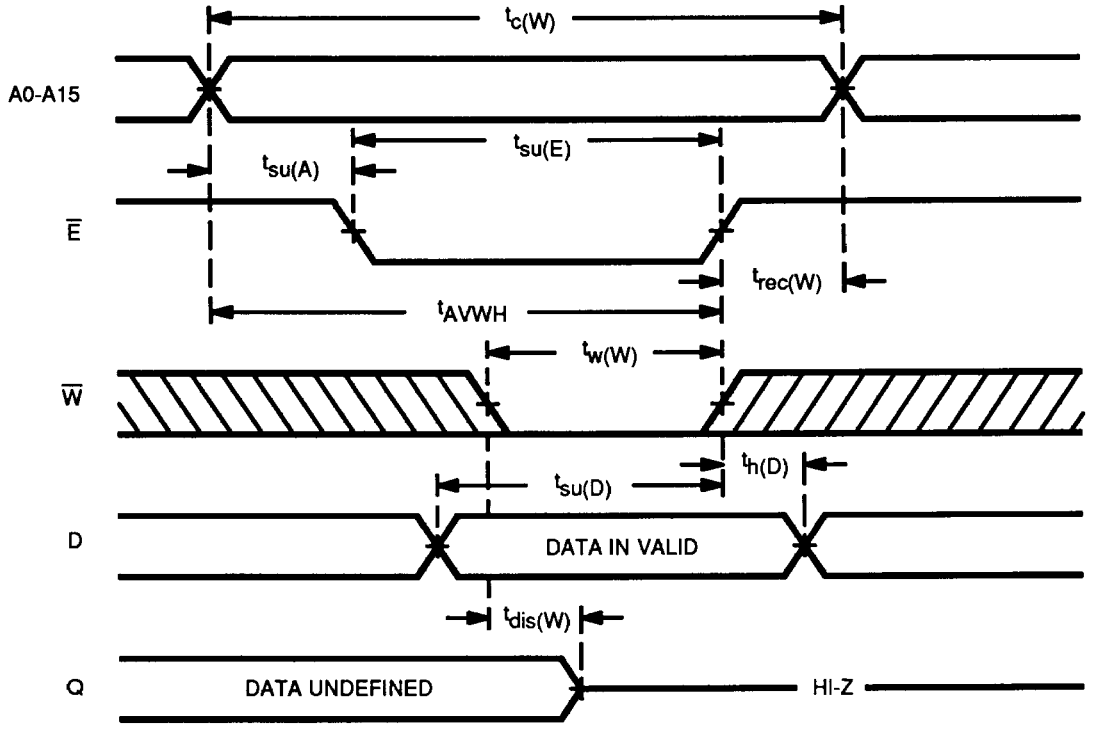
NOTES: 6. Transition is measured ± 500 mV from steady-state voltage with specified loading in Figure 1 Load B ('6787-25/'6787-30).
9. $\overline{W}$ is high and $\overline{E}$ is low for read cycle.

write cycle timing ($\overline{W}$ controlled)



NOTES: 4. Transition is measured ± 200 mV from steady-state voltage with specified loading in Figure 1 Load B ('6787-15/'6787-20).
6. Transition is measured ± 500 mV from steady-state voltage with specified loading in Figure 1 Load B ('6787-25/'6787-30).

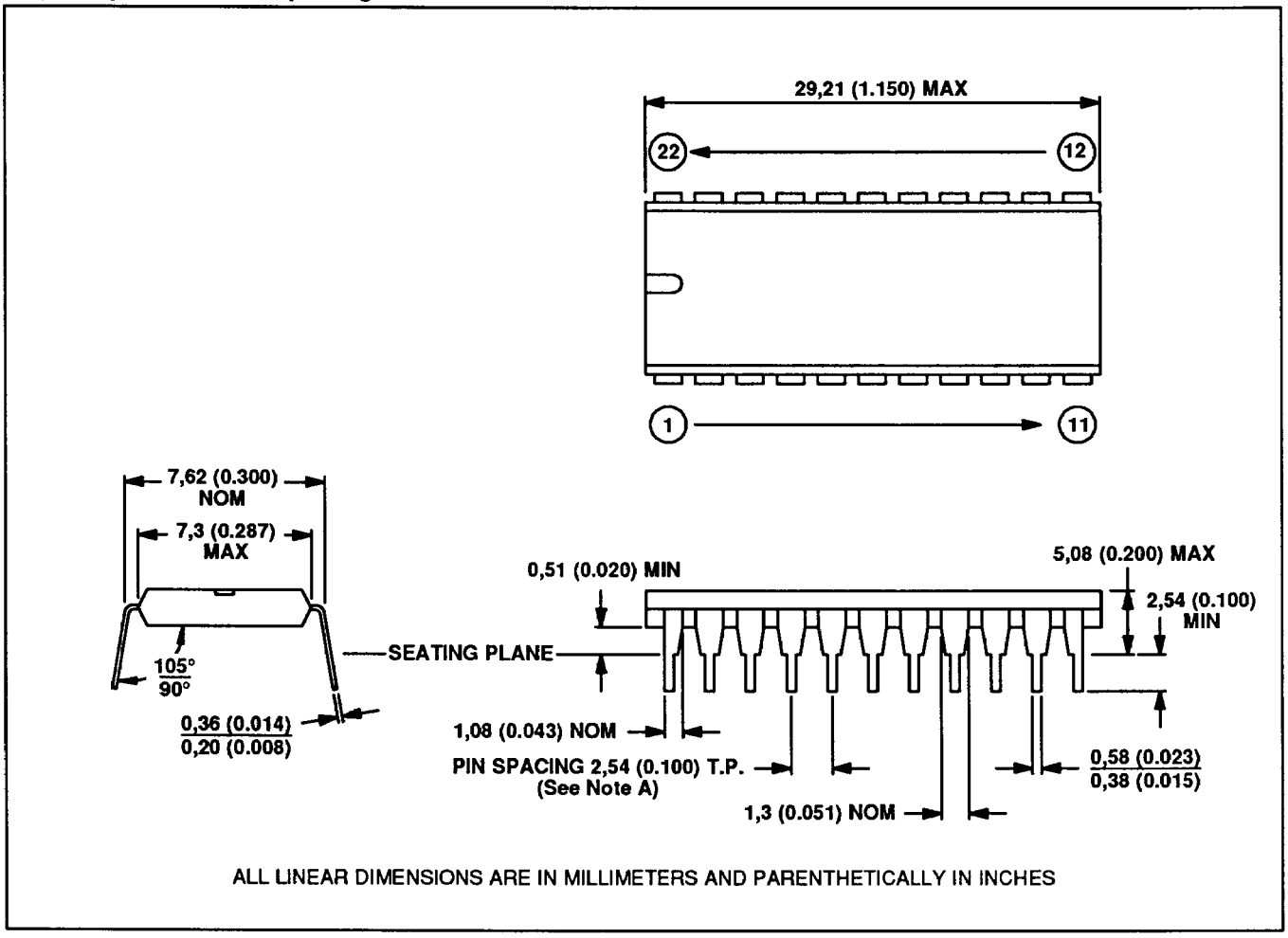
write cycle timing ($\overline{E}$ controlled)



NOTES: 4. Transition is measured ± 200 mV from steady-state voltage with specified loading in Figure 1 Load B ('6787-15/'6787-20).
6. Transition is measured ± 500 mV from steady-state voltage with specified loading in Figure 1 Load B ('6787-25/'6787-30).

MECHANICAL DATA

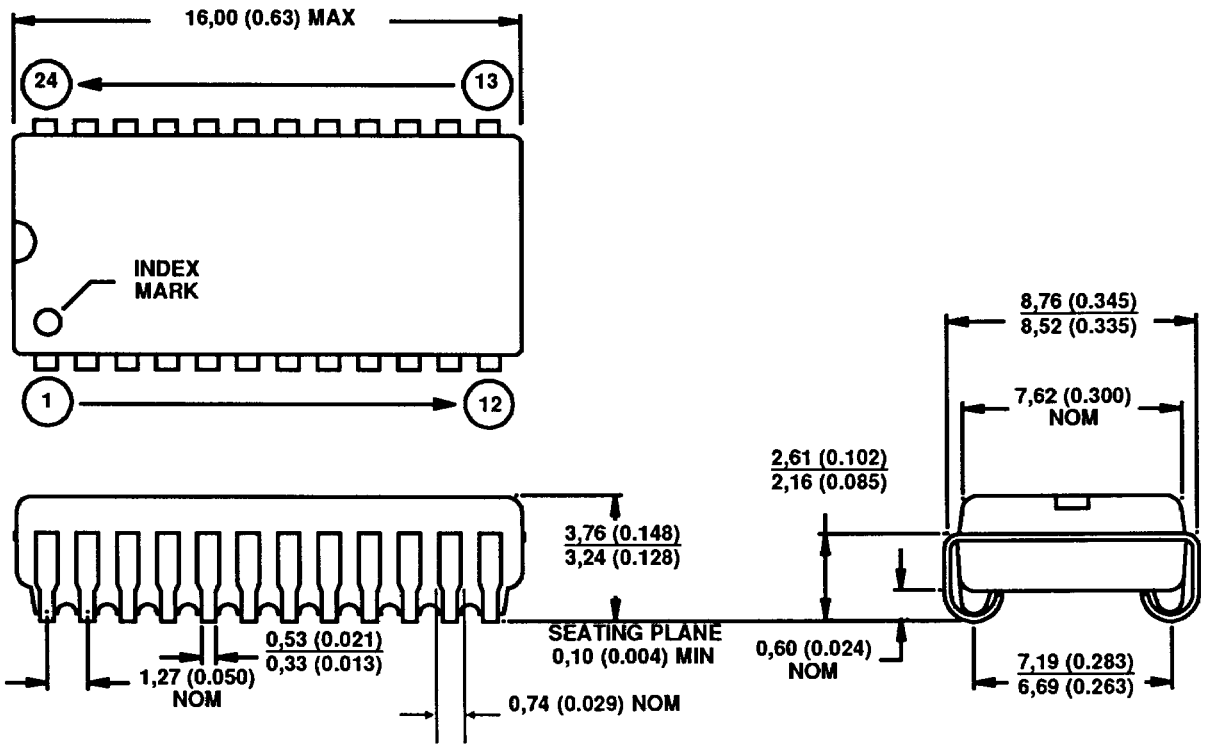
22-pin N plastic 300-mil package



NOTE A: Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.

MECHANICAL DATA

24-pin small outline J-lead surface mount package (DJ suffix)



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES