

FEATURES

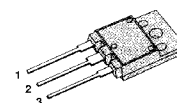
- Advanced New Design
- Advanced Rugged Technology
- Rugged Gate Oxide Technology
- Very Low Intrinsic Capacitances
- Excellent Switching Characteristics
- Unrivalled Gate Charge: 28nC (Typ.)
- Extended Safe Operating Area
- Lower $R_{DS(ON)}$: 0.58 Ω (Typ.)

$$BV_{DSS} = 500V$$

$$R_{DS(ON)} = 0.73\Omega$$

$$I_D = 7.2A$$

TO-3PF



1. Gate 2. Drain 3. Source

ABSOLUTE MAXIMUM RATINGS

Symbol	Characteristics	Value	Units
V_{DSS}	Drain-to-Source Voltage	500	V
I_D	Continuous Drain Current ($T_C = 25^\circ C$)	7.2	A
	Continuous Drain Current ($T_C = 100^\circ C$)	4.6	
I_{DM}	Drain Current-Pulsed ①	29	V
V_{GS}	Gate-to-Source Voltage	± 30	J
E_{AS}	Single Pulsed Avalanche Energy ②	370	mJ
I_{AR}	Avalanche Current ①	7.2	A
E_{AR}	Repetitive Avalanche Energy ①	9.0	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.5	V/ns
P_D	Total Power Dissipation ($T_C = 25^\circ C$)	90	W W/ $^\circ C$
	Linear Derating Factor	0.72	
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	$^\circ C$
T_L	Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5-seconds	300	

THERMAL RESISTANCE

Symbol	Characteristics	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.39	$^\circ C/W$
$R_{\theta JA}$	Junction-to-Ambient	—	40	

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristics	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-Source Breakdown Voltage	500	—	—	V	$V_{GS}=0V$, $I_D=250\mu A$
$\Delta BV/\Delta T_J$	Breakdown Voltage Temp. Coeff.	—	0.55	—	V/ $^\circ\text{C}$	$I_D=250\mu A$, See Fig 7
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS}=5V$, $I_D=250\mu A$
I_{GSS}	Gate-Source Leakage, Forward	—	—	100	nA	$V_{GS}=30V$
	Gate-Source Leakage, Reverse	—	—	–100		$V_{GS}= -30V$
I_{DSS}	Drain-to-Source Leakage Current	—	—	1	μA	$V_{DS}=500V$
		—	—	10		$V_{DS}=400V$, $T_C=125^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-State Resistance	—	0.58	0.73	Ω	$V_{GS}=10V$, $I_D=3.6A$ ④
g_{fs}	Forward Transconductance	—	6.9	—	S	$V_{DS}=50V$, $I_D=3.6A$ ④
C_{iss}	Input Capacitance	—	1100	1450	pF	$V_{GS}=0V$, $V_{DS}=25V$ $f=1\text{MHz}$ See Fig 5
C_{oss}	Output Capacitance	—	160	210		
C_{rss}	Reverse Transfer Capacitance	—	20	30		
$t_{d(on)}$	Turn-On Delay Time	—	25	60	ns	$V_{DD}=250V$, $I_D=9.0A$ $R_G=50\Omega$ See Fig 13 ④ ⑤
t_r	Rise Time	—	95	200		
$t_{d(off)}$	Turn-Off Delay Time	—	55	120		
t_f	Fall Time	—	60	130		
Q_g	Total Gate Charge	—	28	36	nC	$V_{DS}=400V$, $V_{GS}=10V$ $I_D=9.0A$ See Fig 6 & Fig 12 ④ ⑤
Q_{gs}	Gate-Source Charge	—	7.0	—		
Q_{gd}	Gate-Drain (Miller) Charge	—	12.5	—		

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristics	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current	—	—	14	A	Integral reverse pn-diode in the MOSFET
I_{SM}	Pulsed-Source Current ①	—	—	56		
V_{SD}	Diode Forward Voltage ④	—	—	1.5	V	$T_J=25^\circ\text{C}$, $I_S=7.2A$, $V_{GS}=0V$
Q_{rr}	Reverse Recovery Time	—	300	—	ns	$T_J=25^\circ\text{C}$, $I_F=9.0A$, $V_{DD}=400V$ $di_F/dt=100A/\mu s$ ④
	Reverse Recovery Charge	—	2.7	—	μC	

Notes:

- ① Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
 ② $L=13\text{mH}$, $I_{AS}=7.2A$, $V_{DD}=50V$, $R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$
 ③ $I_{SD} \leq 9.0A$, $di/dt \leq 200A/\mu s$, $V_{DD} \leq BV_{DSS}$, Starting $T_J=25^\circ\text{C}$
 ④ Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
 ⑤ Essentially Independent of Operating Temperature

Fig 1. Output Characteristics

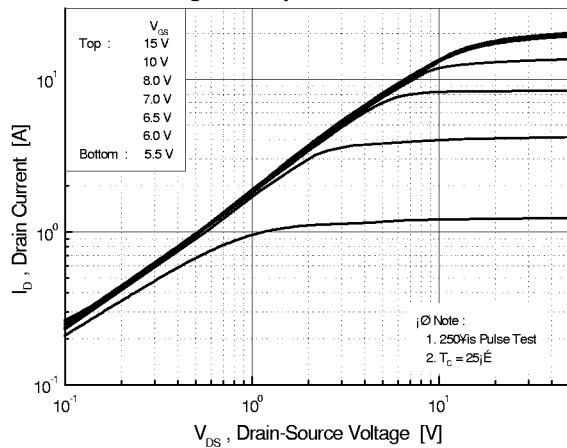


Fig 2. Transfer Characteristics

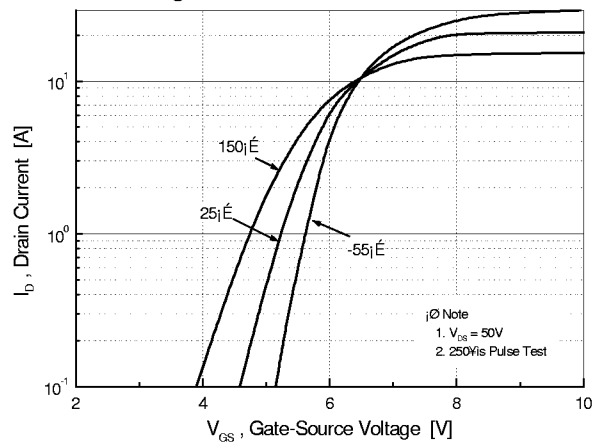


Fig 3. On-Resistance vs. Drain Current

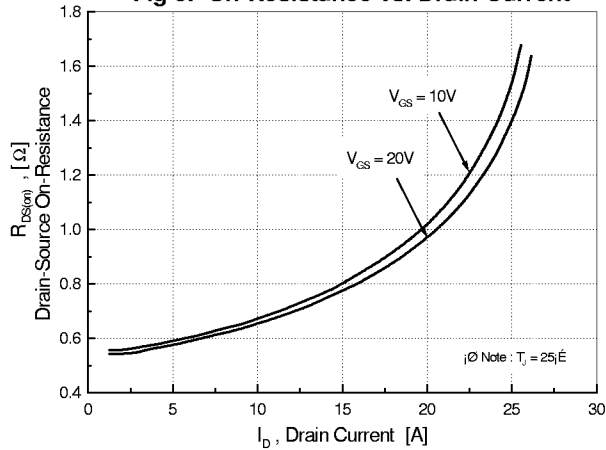


Fig 4. Source-Drain Diode Forward Voltage

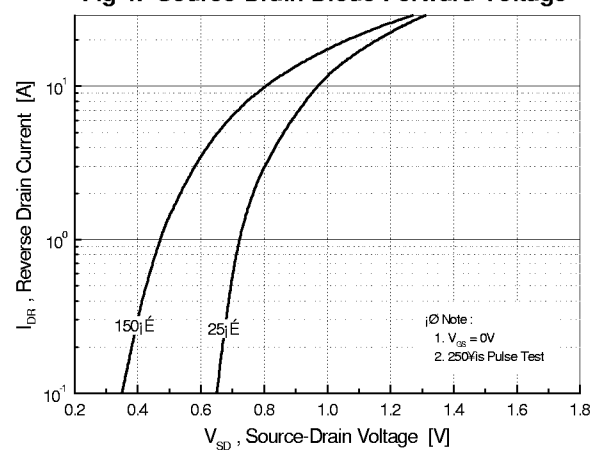


Fig 5. Capacitance vs. Drain-Source Voltage

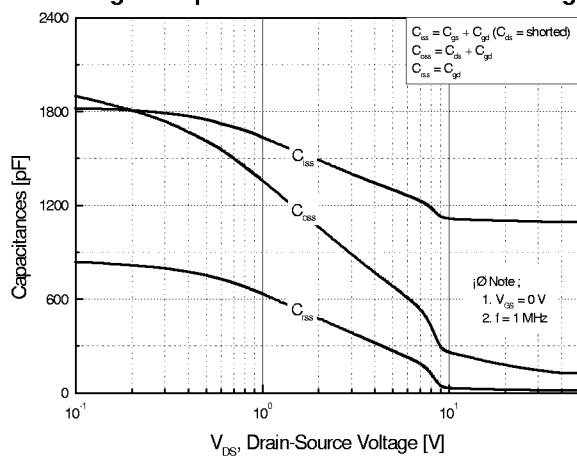


Fig 6. Gate Charge vs. Gate-Source Voltage

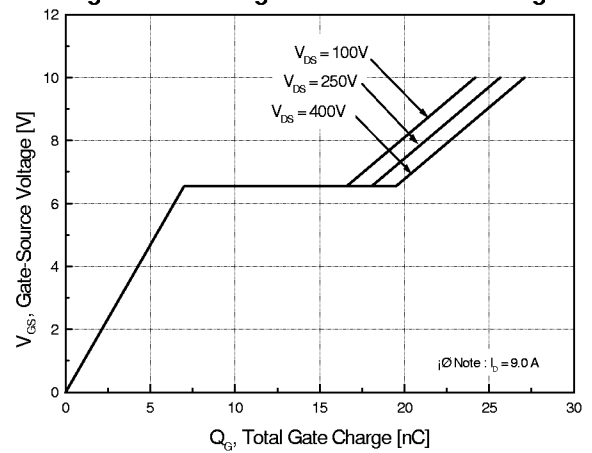


Fig 7. Breakdown Voltage vs. Temperature

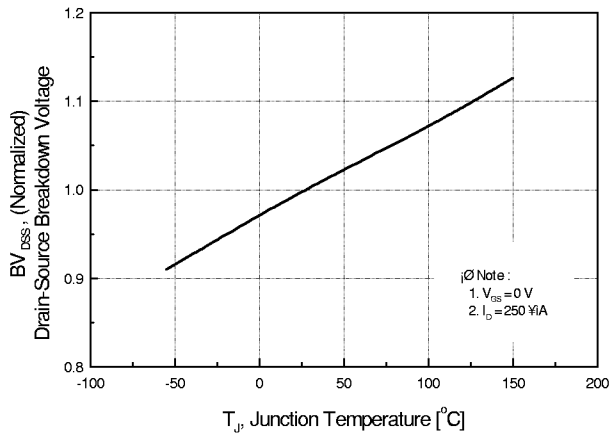


Fig 8. On-Resistance vs. Temperature

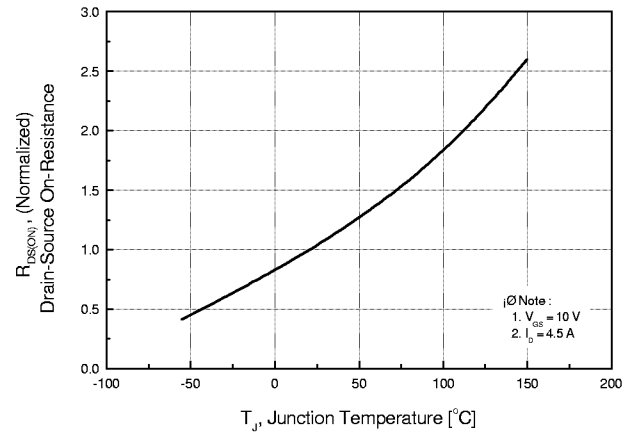


Fig 9. Max. Safe Operating Area

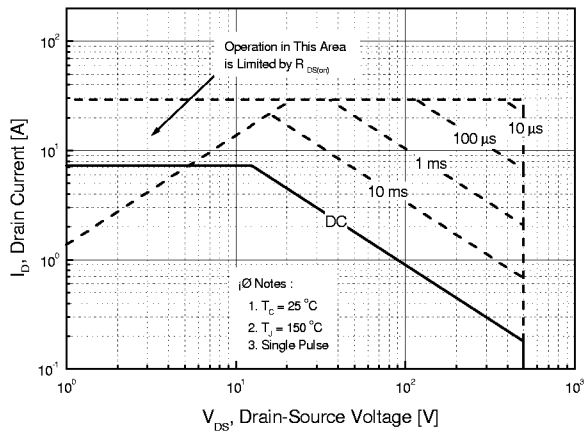


Fig 10. Max. Drain Current vs. Case Temperature

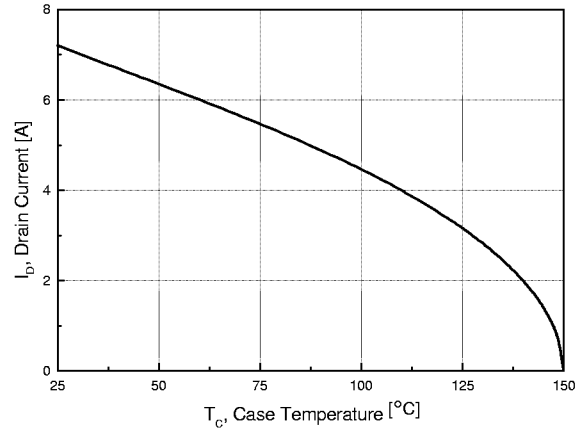


Fig 11. Thermal Response

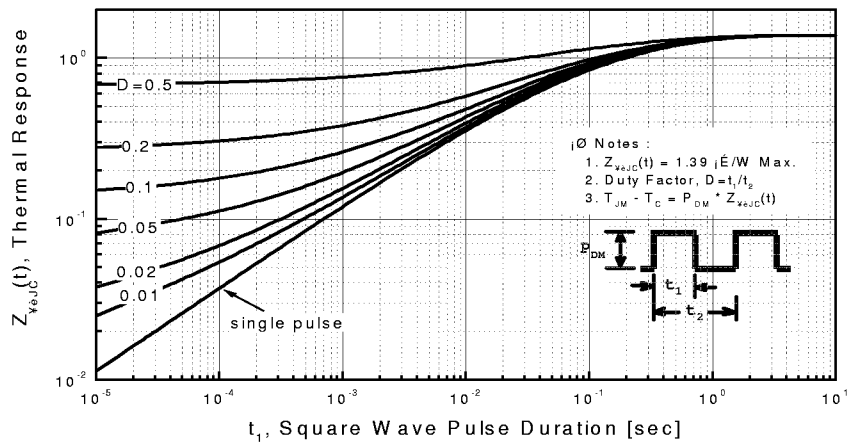


Fig 12. Gate Charge Test Circuit & Waveform

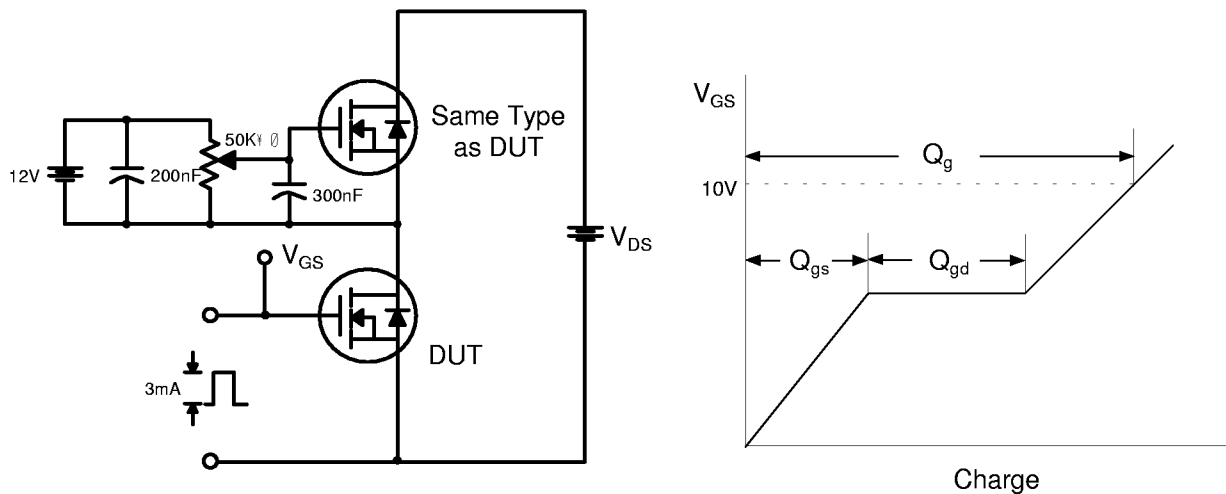


Fig 13. Resistive Switching Test Circuit & Waveforms

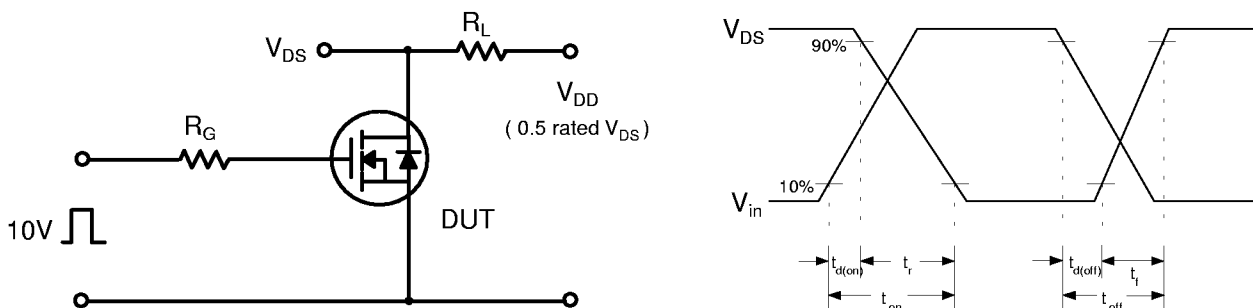


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

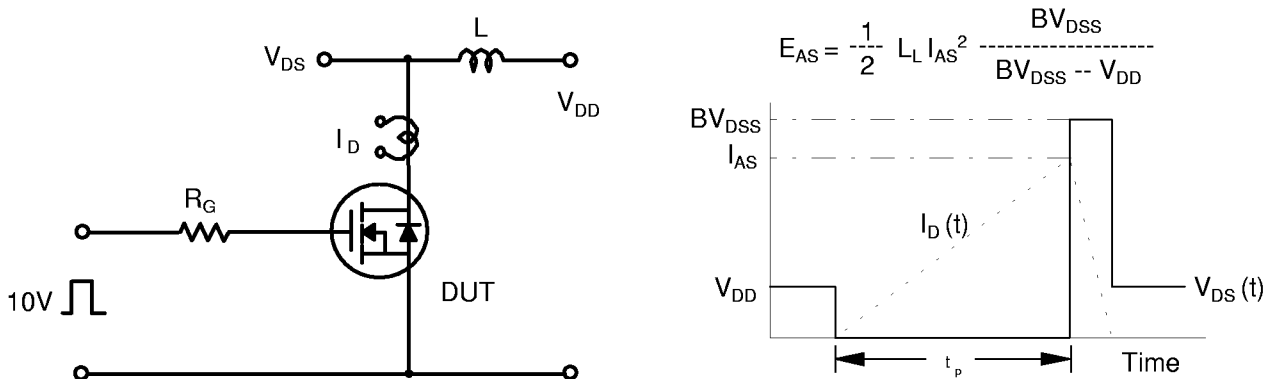


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

