

2-Mbit (128K x 16) Static RAM

Features

- **Very high speed**
 - 55 ns
- **Voltage range**
 - 2.7V – 3.3V
- **Pin-compatible with the CY62136V**
- **Ultra-low active power**
 - Typical active current: 1.5 mA @ f = 1 MHz
 - Typical active current: 7 mA @ f = f_{Max} (55 ns speed)
- **Low standby power**
- **Easy memory expansion with $\overline{\text{CE}}$ and $\overline{\text{OE}}$ features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Available in Pb-free and non Pb-free 48-ball VFBGA package**

Functional Description^[1]

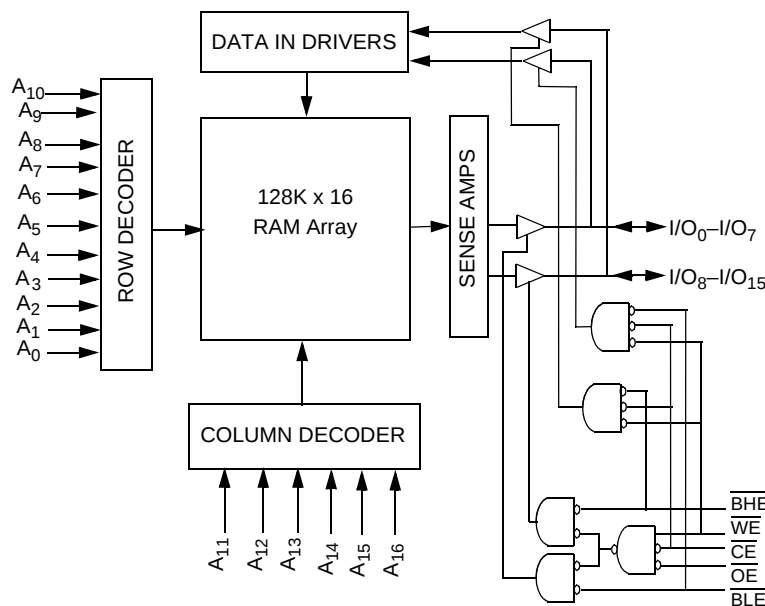
The CY62136CV30 is high-performance CMOS static RAM organized as 128K words by 16 bits. This device features advanced circuit design to provide ultra-low active current.

This is ideal for providing More Battery Life™ (MoBL[®]) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 80% when addresses are not toggling. The device can also be put into standby mode reducing power consumption by more than 99% when deselected (CE HIGH). The input/output pins (I/O₀ through I/O₁₅) are placed in a high-impedance state when: deselected (CE HIGH), outputs are disabled ($\overline{\text{OE}}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{\text{BHE}}$, BLE HIGH), or during a write operation (CE LOW, and WE LOW).

Writing to the device is accomplished by taking Chip Enable ($\overline{\text{CE}}$) and Write Enable (WE) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O₀ through I/O₇), is written into the location specified on the address pins (A₀ through A₁₆). If Byte High Enable ($\overline{\text{BHE}}$) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₆).

Reading from the device is accomplished by taking Chip Enable ($\overline{\text{CE}}$) and Output Enable ($\overline{\text{OE}}$) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O₀ to I/O₇. If Byte High Enable ($\overline{\text{BHE}}$) is LOW, then data from memory will appear on I/O₈ to I/O₁₅. See the truth table at the back of this data sheet for a complete description of read and write modes.

Logic Block Diagram



Note:

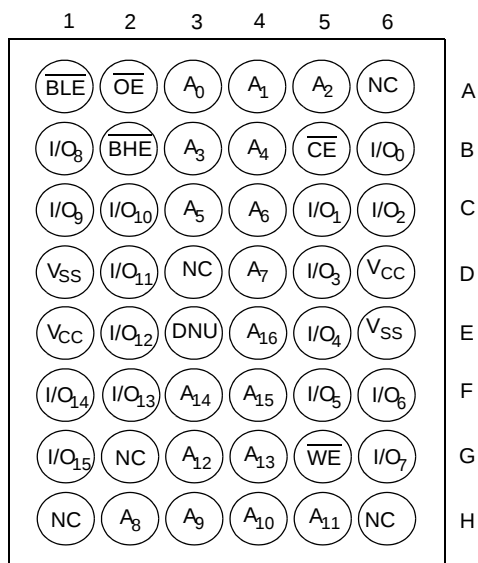
1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

Product Portfolio

Product	V _{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating, I _{CC} (mA)				Standby, I _{SB2} (μA)	
	f = 1 MHz		f = f _{Max}							
	V _{CC(min.)}	V _{CC(typ.)} ^[2]	V _{CC(max.)}		Typ. ^[2]	Max.	Typ. ^[2]	Max.	Typ. ^[2]	Max.
CY62136CV30LL	2.7	3.0	3.3	55	1.5	3	7	15	2	10
				70	1.5	3	5.5	12		

Pin Configuration^[3, 4]

48-ball VFBGA
Top View



Notes:

- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ.)}, T_A = 25°C.
- NC pins are not connected to the die.
- E3 (DNU) pin have to be left floating or tied to V_{SS} to ensure proper operation.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature–65°C to +150°C

Ambient Temperature with

Power Applied.....–55°C to +125°C

Supply Voltage to Ground Potential–0.5V to $V_{CC(max)}$ + 0.5V

DC Voltage Applied to Outputs

in High-Z State^[5]–0.5V to V_{CC} + 0.3V

DC Input Voltage^[5]–0.5V to V_{CC} + 0.3V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... > 2001V
(per MIL-STD-883, Method 3015)

Latch-up Current..... > 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}
CY62136CV30	Industrial	–40°C to +85°C	2.7V to 3.3V

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CY62136CV30-55			CY62136CV30-70			Unit
			Min.	Typ. ^[2]	Max.	Min.	Typ. ^[2]	Max.	
V_{OH}	Output HIGH Voltage	$I_{OH} = -1.0$ mA $V_{CC} = 2.7$ V	2.4			2.4			V
V_{OL}	Output LOW Voltage	$I_{OL} = 2.1$ mA $V_{CC} = 2.7$ V			0.4			0.4	V
V_{IH}	Input HIGH Voltage		2.2		$V_{CC} + 0.3$ V	2.2		$V_{CC} + 0.3$ V	V
V_{IL}	Input LOW Voltage		–0.3		0.8	–0.3		0.8	V
I_{IX}	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	–1		+1	–1		+1	μA
I_{OZ}	Output Leakage Current	$GND \leq V_O \leq V_{CC}$, Output Disabled	–1		+1	–1		+1	μA
I_{CC}	V_{CC} Operating Supply Current	$f = f_{Max} = 1/t_{RC}$ $V_{CC} = 3.3$ V $I_{OUT} = 0$ mA CMOS Levels		7	15		5.5	12	mA
		$f = 1$ MHz		1.5	3		1.5	3	
I_{SB1}	Automatic CE Power-down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2$ V $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, $f = f_{Max}$ (Address and Data Only), $f = 0$ ($\overline{OE}$, $\overline{WE}$, $\overline{BHE}$, and $\overline{BLE}$)		2	10		2	10	μA
I_{SB2}	Automatic CE Power-down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2$ V $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, $f = 0$, $V_{CC} = 3.3$ V		2	10		2	10	μA

Capacitance^[7]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}$, $f = 1$ MHz, $V_{CC} = V_{CC(typ.)}$	6	pF
C_{OUT}	Output Capacitance		8	pF

Thermal Resistance^[7]

Parameter	Description	Test Conditions	VFBGA	Unit
θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 x 4.5 inch, 2-layer printed circuit board	55	°C/W
θ_{JC}	Thermal Resistance (Junction to Case)		16	°C/W

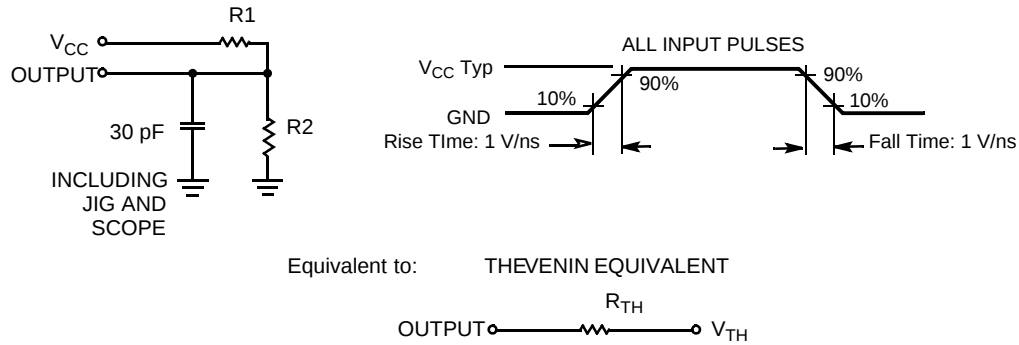
Notes:

5. $V_{IL(min.)} = -2.0$ V for pulse durations less than 20 ns.

6. Tested initially and after any design or process changes that may affect these parameters.

7. Full Device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} > 100$ μs or stable at $V_{CC(min.)} > 100$ μs.

AC Test Loads and Waveforms

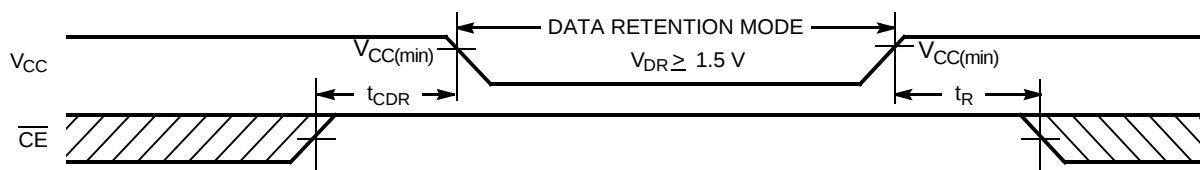


Parameters	3.0V	Unit
R1	1105	Ω
R2	1550	Ω
R_{TH}	645	Ω
V_{TH}	1.75	V

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ. ^[2]	Max.	Unit
V_{DR}	V_{CC} for Data Retention		1.5		$V_{CC(max)}$	V
I_{CCDR}	Data Retention Current	$V_{CC} = 1.5V, \overline{CE} \geq V_{CC} - 0.2V, V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		1	6	μA
$t_{CDR}^{[7]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[7]}$	Operation Recovery Time		t_{RC}			ns

Data Retention Waveform



Switching Characteristics Over the Operating Range^[8]

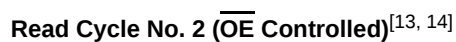
Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t _{RC}	Read Cycle Time	55		70		ns
t _{AA}	Address to Data Valid		55		70	ns
t _{OHA}	Data Hold from Address Change	10		10		ns
t _{ACE}	$\overline{CE}$ LOW to Data Valid		55		70	ns
t _{DOE}	$\overline{OE}$ LOW to Data Valid		25		35	ns
t _{LZOE}	$\overline{OE}$ LOW to Low-Z ^[9]	5		5		ns
t _{HZOE}	$\overline{OE}$ HIGH to High-Z ^[9, 10]		20		25	ns
t _{LZCE}	$\overline{CE}$ LOW to Low-Z ^[9]	10		10		ns
t _{HZCE}	$\overline{CE}$ HIGH to High-Z ^[9, 10]		20		25	ns
t _{PU}	$\overline{CE}$ LOW to Power-up	0		0		ns
t _{PD}	$\overline{CE}$ HIGH to Power-down		55		70	ns
t _{DBE}	$\overline{BHE}/\overline{BLE}$ LOW to Data Valid		25		35	ns
t _{LZBE}	$\overline{BHE}/\overline{BLE}$ LOW to Low-Z ^[9]	5		5		ns
t _{HZBE}	$\overline{BHE}/\overline{BLE}$ HIGH to High-Z ^[9, 10]		20		25	ns
Write Cycle ^[11]						
t _{WC}	Write Cycle Time	55		70		ns
t _{SCE}	$\overline{CE}$ LOW to Write End	45		60		ns
t _{AW}	Address Set-up to Write End	45		60		ns
t _{HA}	Address Hold from Write End	0		0		ns
t _{SA}	Address Set-up to Write Start	0		0		ns
t _{PWE}	$\overline{WE}$ Pulse Width	40		45		ns
t _{BW}	$\overline{BHE}/\overline{BLE}$ Pulse Width	50		60		ns
t _{SD}	Data Set-up to Write End	25		30		ns
t _{HD}	Data Hold from Write End	0		0		ns
t _{HZWE}	$\overline{WE}$ LOW to High-Z ^[9, 10]		20		25	ns
t _{LZWE}	$\overline{WE}$ HIGH to Low-Z ^[9]	10		10		ns

Notes:

8. Test conditions assume signal transition time of 5 ns or less, timing reference levels of $V_{CC(typ.)}/2$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
9. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
10. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
11. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE} = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.



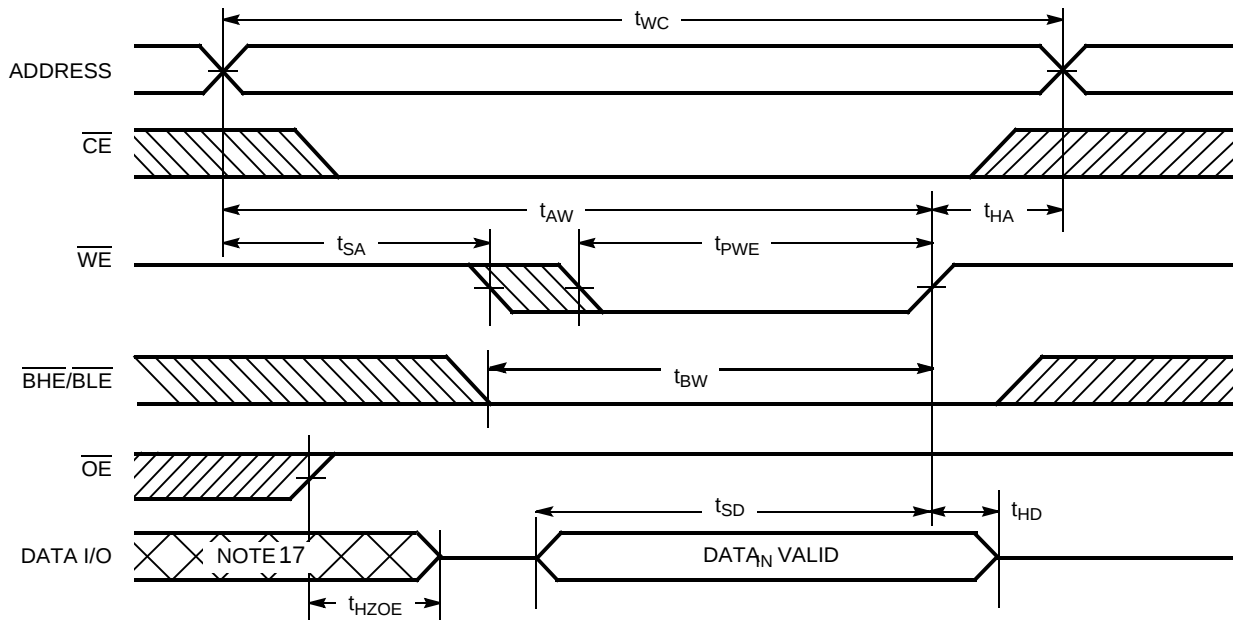
Read Cycle No. 1(Address Transition Controlled)^[12, 13]



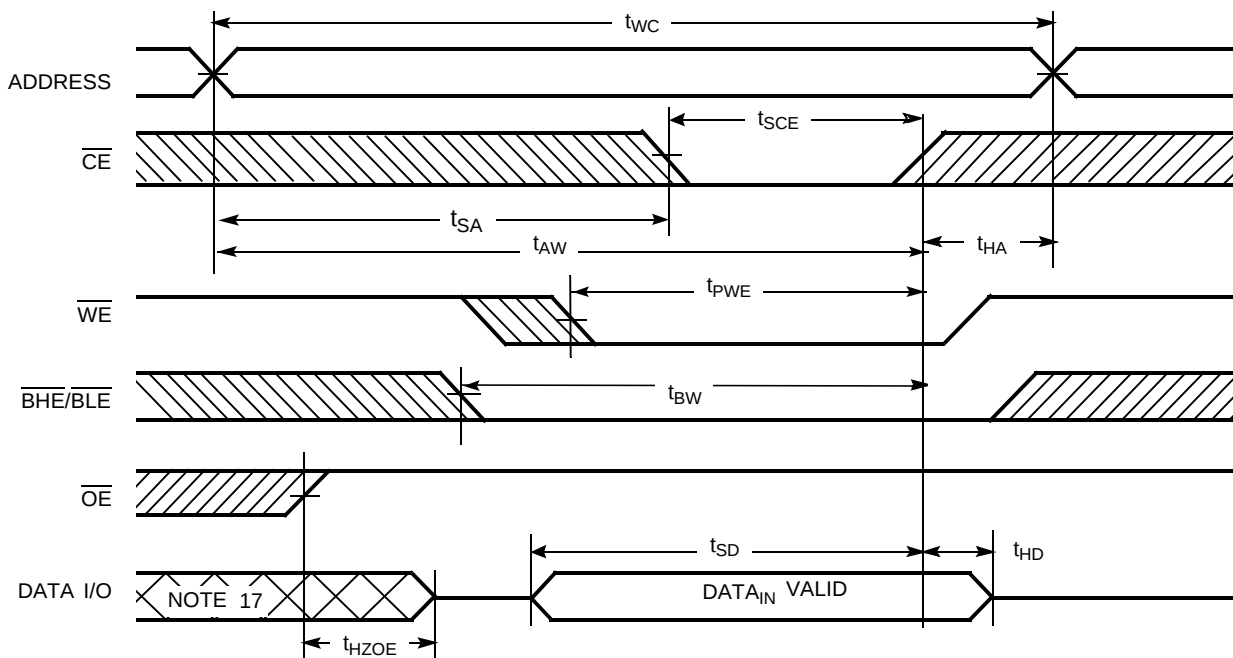
14. Address valid prior to or coincident with $\overline{\text{CE}}$, $\overline{\text{BHE}}$, $\overline{\text{BLE}}$ transition LOW.

Switching Waveforms

Write Cycle No. 1 ($\overline{\text{WE}}$ Controlled)^[11, 15, 16]



Write Cycle No. 2 ($\overline{\text{CE}}$ Controlled)^[11, 15, 16]

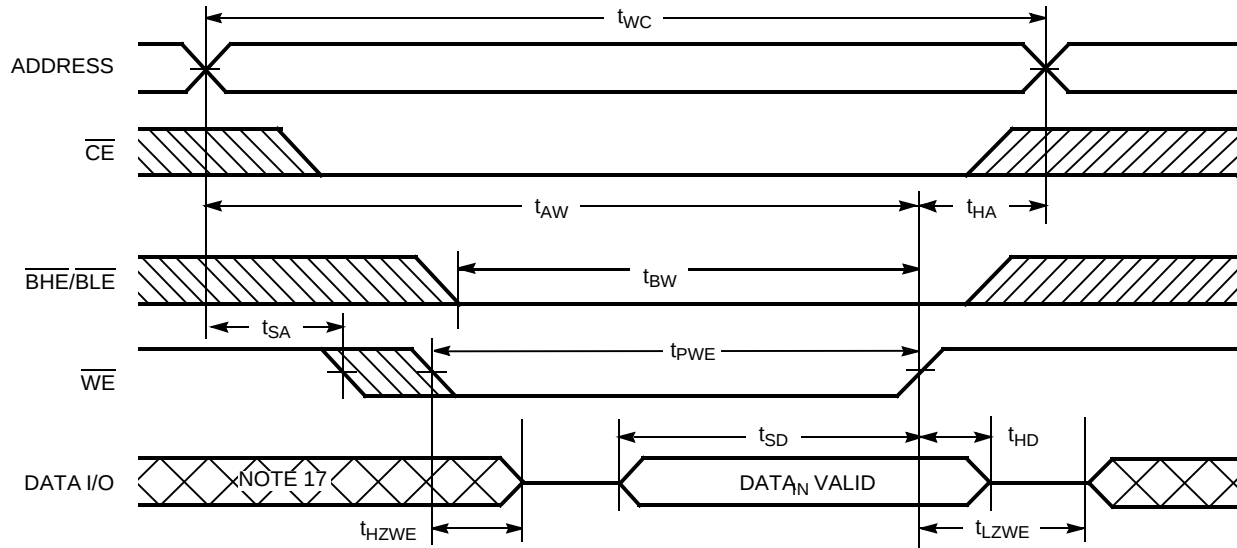


Notes:

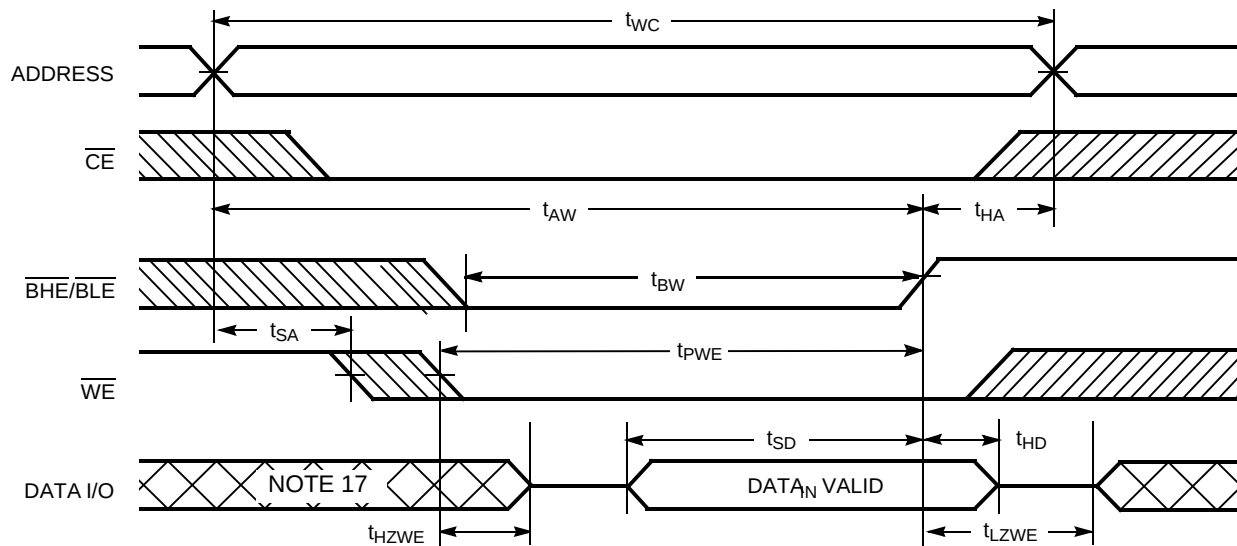
15. Data I/O is high-impedance if $\overline{\text{OE}} = V_{\text{IH}}$.
16. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ HIGH, the output remains in a high-impedance state.
17. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms

Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)^[16]



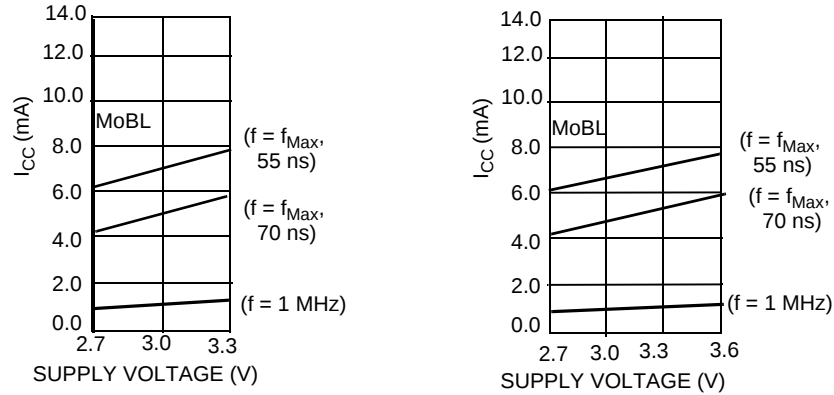
Write Cycle No. 4 ($\overline{\text{BHE/BLE}}$ Controlled, $\overline{\text{OE}}$ LOW)^[16]



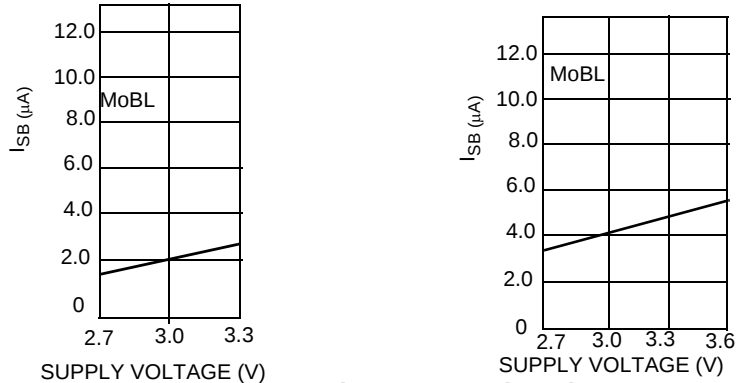
Typical DC and AC Parameters

(Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, $T_A = 25^\circ\text{C}$)

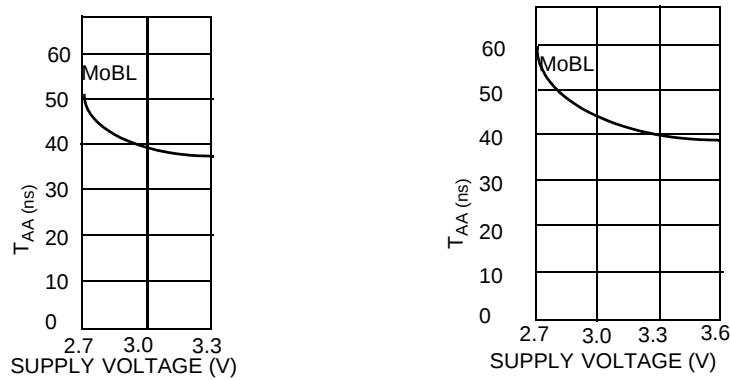
Operating Current vs. Supply Voltage



Standby Current vs. Supply Voltage



Access Time vs. Supply Voltage



Truth Table

$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	$\overline{\text{BHE}}$	$\overline{\text{BLE}}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	High-Z	Deselect/Power-down	Standby (I_{SB})
L	X	X	H	H	High-Z	Output Disabled	Active (I_{CC})
L	H	L	L	L	Data Out (I/O_0 – I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	High Z (I/O_8 – I/O_{15}); Data Out (I/O_0 – I/O_7)	Read	Active (I_{CC})
L	H	L	L	H	Data Out (I/O_8 – I/O_{15}); High Z (I/O_0 – I/O_7)	Read	Active (I_{CC})
L	L	X	L	L	Data In (I/O_0 – I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	High Z (I/O_8 – I/O_{15}); Data In (I/O_0 – I/O_7)	Write	Active (I_{CC})
L	L	X	L	H	Data in (I/O_8 – I/O_{15}); High Z (I/O_0 – I/O_7)	Write	Active (I_{CC})
L	H	H	L	L	High-Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	High-Z	Output Disabled	Active (I_{CC})
L	H	H	L	H	High-Z	Output Disabled	Active (I_{CC})

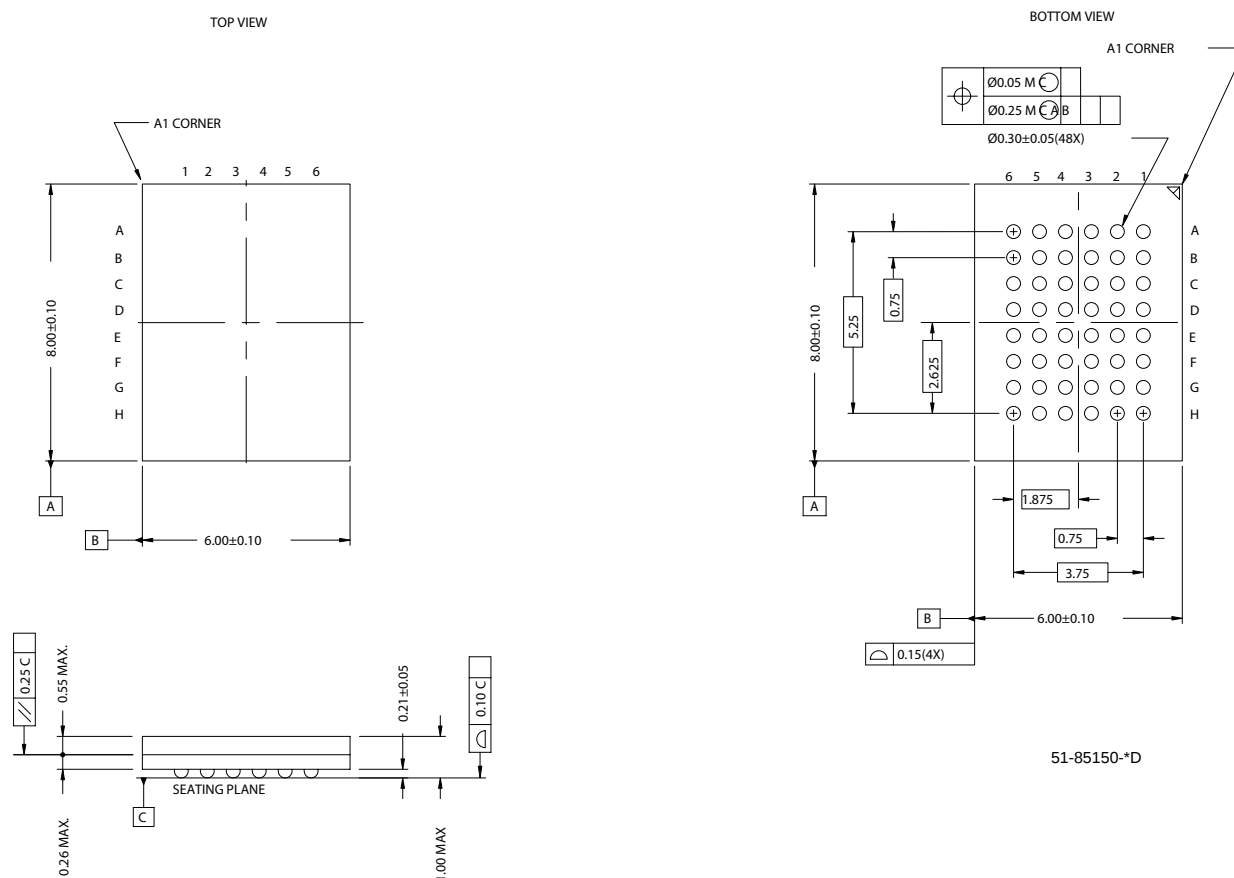
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY62136CV30LL-55BVI	51-85150	48-ball Fine Pitch BGA (6 x 8 x 1 mm)	Industrial
70	CY62136CV30LL-70BVXI		48-ball Fine Pitch BGA (6 x 8 x 1 mm) Pb-free	

Please contact your local Cypress sales representative for availability of these parts

Package Diagram

48-ball VFBGA (6 x 8 x 1 mm) (51-85150)



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Document History Page

Document Title: CY62136CV30 2-Mbit (128K x 16) Static RAM Document Number: 38-05199				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	112379	02/19/02	GAV	New Data Sheet (advance information)
*A	114023	04/25/02	JUI	Added BV package diagram Changed Advance Information to Preliminary
*B	117063	07/12/02	MGN	Changed Preliminary to Final
*C	118121	08/26/02	MGN	Added new part numbers: CY62136CV with wider voltage (2.7V – 3.6V); CY62136CV33 narrower voltage range (3.0V – 3.6V) For $T_{AA} = 55$ ns, improved t_{PWE} Min from 45 ns to 40 ns For $T_{AA} = 70$ ns, improved t_{PWE} Min from 50 ns to 45 ns For $T_{AA} = 70$ ns, improved t_{LZWE} Min from 5 ns to 10 ns
*D	118622	10/3/02	MGN	Improved Typ. I_{CC} spec. to 7 mA (for 55 ns) and 5.5 mA (for 70 ns) Improved Max I_{CC} spec. to 15 mA (for 55 ns) and 12 mA (for 70 ns) For $T_{AA} = 55$ ns, improved t_{LZWE} min. from 5 ns to 10 ns Changed upper spec. for Supply Voltage to Ground Potential to $V_{CC(max)} + 0.5V$ Changed upper spec. for DC Voltage Applied to Outputs in High-Z State and DC Input Voltage to $V_{CC} + 0.3V$
*E	486789	SEE ECN	VKN	Changed address of Cypress Semiconductor Corporation on Page# 1 from "3901 North First Street" to "198 Champion Court" Removed Part numbers: CY62136CV and CY62136CV33 Updated Ordering Information table