

# DATA SHEET

## **74ALVCH16823**

18-bit bus-interface D-type flip-flop  
with reset and enable (3-State)

Product specification

1998 Jul 29

IC24 Data Handbook

## 18-bit D-type flip-flop (3-State)

## 74ALVCH16823

## FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A.
- CMOS low power consumption
- Direct interface with TTL levels
- Current drive  $\pm 24$  mA at 3.0 V
- Multibyte™flow-through standard pin-out architecture
- Low inductance multiple  $V_{CC}$  and GND pins to minimize noise and ground bounce
- All data inputs have bus hold
- Output drive capability 50 $\Omega$  transmission lines @ 85°C

## DESCRIPTION

The 74ALVCH16823 is a 18-bit edge-triggered flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. Incorporates bushold data inputs which eliminate the need for external pull-up resistors to hold unused inputs. The 74ALVCH16823 consists of two sections of nine edge-triggered flip-flops. A clock (CP) input, an output-enable ( $\overline{OE}$ ) input, a Master reset ( $\overline{MR}$ ) input and a clock-enable ( $\overline{CE}$ ) input are provided for each total 9-bit section.

With the clock-enable ( $\overline{CE}$ ) input LOW, the D-type flip-flops will store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH CP transition. Taking  $\overline{CE}$  HIGH disables the clock buffer, thus latching the outputs. Taking the Master reset ( $\overline{MR}$ ) input LOW causes all the Q outputs to go LOW independently of the clock.

When  $\overline{OE}$  is LOW, the contents of the flip-flops are available at the outputs. When the  $\overline{OE}$  is HIGH, the outputs go to the high impedance OFF-state. Operation of the  $\overline{OE}$  input does not affect the state of flip-flops.

Active bus hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

## QUICK REFERENCE DATA

GND = 0V;  $T_{amb} = 25^{\circ}\text{C}$ ;  $t_r = t_f \leq 2.5\text{ns}$

| SYMBOL            | PARAMETER                               | CONDITIONS                                                               |                  | TYPICAL    | UNIT |
|-------------------|-----------------------------------------|--------------------------------------------------------------------------|------------------|------------|------|
| $t_{PHL}/t_{PLH}$ | Propagation delay<br>CP to Qn           | $V_{CC} = 2.5\text{V}$ , CL = 30pF<br>$V_{CC} = 3.3\text{V}$ , CL = 50pF |                  | 2.1<br>2.1 | ns   |
| $F_{max}$         | Maximum clock frequency                 | $V_{CC} = 2.5\text{V}$ , CL = 30pF<br>$V_{CC} = 3.3\text{V}$ , CL = 50pF |                  | 300<br>350 | MHz  |
| $C_I$             | Input capacitance                       |                                                                          |                  | 5.0        | pF   |
| $C_{PD}$          | Power dissipation capacitance per latch | $V_I = \text{GND to } V_{CC}^1$                                          | Outputs enabled  | 16         | pF   |
|                   |                                         |                                                                          | Outputs disabled | 10         |      |

## NOTES:

- $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  $C_L$  = output load capacity in pF;  
 $f_o$  = output frequency in MHz;  $V_{CC}$  = supply voltage in V;  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

## ORDERING INFORMATION

| PACKAGES                     | TEMPERATURE RANGE | OUTSIDE NORTH AMERICA | NORTH AMERICA | DWG NUMBER |
|------------------------------|-------------------|-----------------------|---------------|------------|
| 56-Pin Plastic SSOP Type II  | -40°C to +85°C    | 74ALVCH16823 DL       | ACH16823 DL   | SOT371-1   |
| 56-Pin Plastic TSSOP Type II | -40°C to +85°C    | 74ALVCH16823 DGG      | ACH16823 DGG  | SOT364-1   |

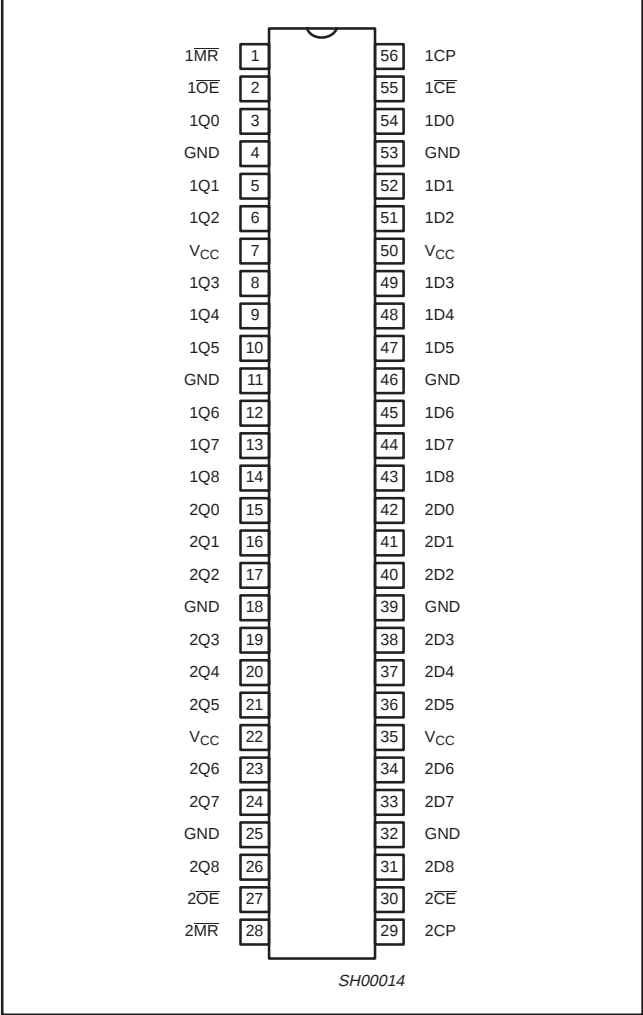
18-bit D-type flip-flop (3-State)

74ALVCH16823

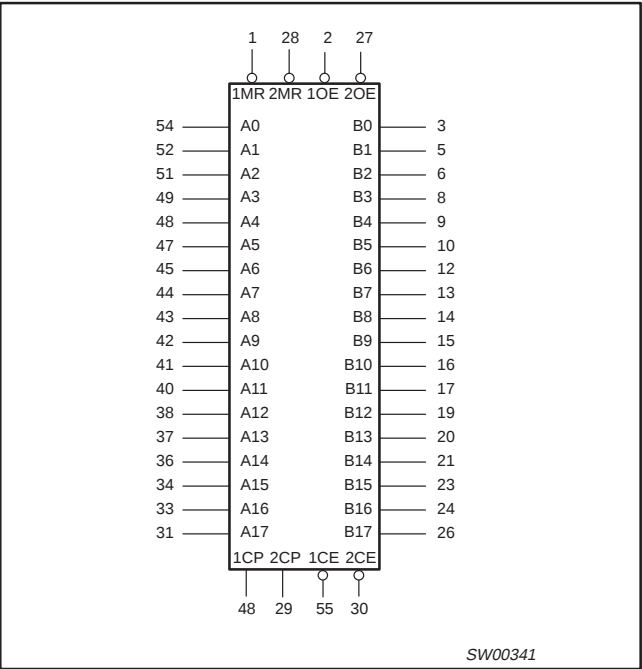
PIN DESCRIPTION

| PIN NUMBER                                                               | SYMBOL             | FUNCTION                               |
|--------------------------------------------------------------------------|--------------------|----------------------------------------|
| 2, 27                                                                    | 1OE, 2OE           | Output enable input (active-Low)       |
| 54, 52, 51, 49, 48, 47, 45, 44, 43<br>42, 41, 40, 38, 37, 36, 34, 33, 31 | 1D0-1D8<br>2D0-2D8 | Data inputs                            |
| 3, 5, 6, 8, 9, 10, 12, 13, 14<br>15, 16, 17, 19, 20, 21, 23, 24, 26      | 1Q0-1Q8<br>2Q0-2Q8 | Data outputs                           |
| 56, 29                                                                   | 1CP, 2CP           | Clock pulse input (active rising edge) |
| 55, 30                                                                   | 1CE, 2CE           | Clock enable input (active-Low)        |
| 1, 28                                                                    | 1MR, 2MR           | Master reset input (active-Low)        |
| 4, 11, 18, 25, 32, 39, 46, 53                                            | GND                | Ground (0V)                            |
| 7, 22, 35, 50                                                            | VCC                | Positive supply voltage                |

PIN CONFIGURATION



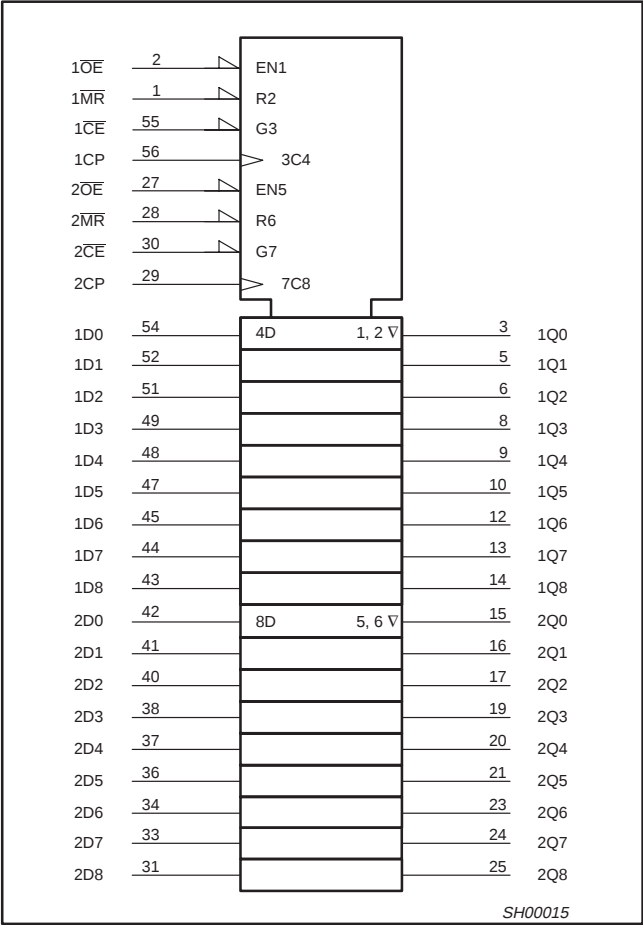
LOGIC SYMBOL



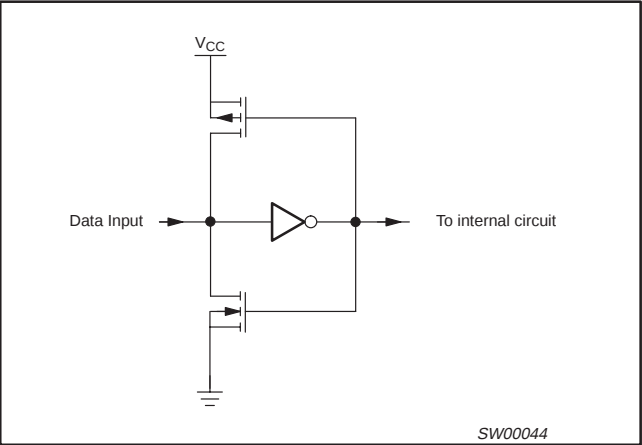
18-bit D-type flip-flop (3-State)

74ALVCH16823

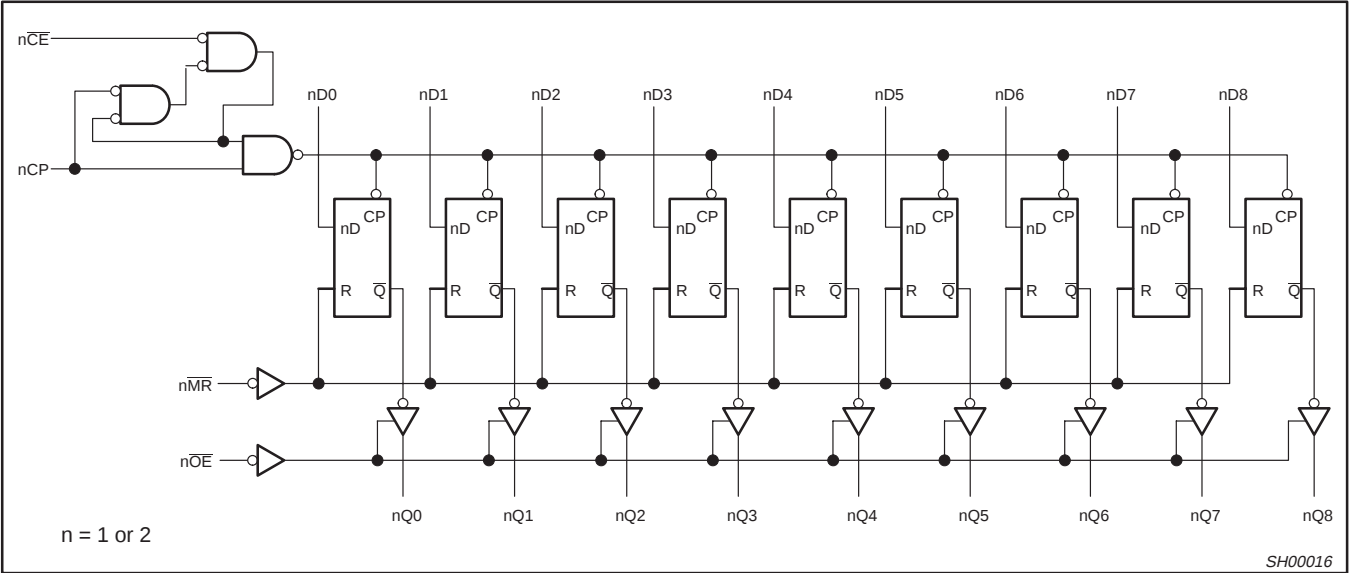
LOGIC SYMBOL (IEEE/IEC)



BUS HOLD CIRCUIT



LOGIC DIAGRAM



## 18-bit D-type flip-flop (3-State)

74ALVCH16823

## FUNCTION TABLE

| INPUTS |     |     |     |     | OUTPUT         | OPERATING MODES    |
|--------|-----|-----|-----|-----|----------------|--------------------|
| nOE    | nMR | nCE | nCP | nDx | nQx            |                    |
| L      | L   | X   | X   | X   | L              | Clear              |
| L      | H   | L   | ↑   | h   | H              | Load and read data |
| L      | H   | L   | ↑   | l   | L              |                    |
| L      | H   | L   | L   | X   | Q <sub>0</sub> | Hold               |
| L      | H   | H   | X   | X   | Q <sub>0</sub> |                    |
| H      | X   | X   | X   | X   | Z              | Disable outputs    |

H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the Low-to-High clock transition

L = LOW voltage level

l = LOW voltage level one set-up time prior to the Low-to-High clock transition

X = Don't care

Z = HIGH impedance "off" state

↑ = LOW to High clock transition

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL                          | PARAMETER                                                                     | CONDITIONS                    | LIMITS |                 | UNIT |
|---------------------------------|-------------------------------------------------------------------------------|-------------------------------|--------|-----------------|------|
|                                 |                                                                               |                               | MIN    | MAX             |      |
| V <sub>CC</sub>                 | DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load) |                               | 2.3    | 2.7             | V    |
|                                 | DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load) |                               | 3.0    | 3.6             |      |
| V <sub>CC</sub>                 | DC supply voltage (for low-voltage applications)                              |                               | 1.2    | 3.6             | V    |
| V <sub>I</sub>                  | DC Input voltage range                                                        | for data input pins           | 0      | V <sub>CC</sub> | V    |
|                                 |                                                                               | for control pins              | 0      | 5.5             | V    |
| V <sub>O</sub>                  | DC output voltage range                                                       |                               | 0      | V <sub>CC</sub> | V    |
| T <sub>amb</sub>                | Operating free-air temperature range                                          |                               | −40    | +85             | °C   |
| t <sub>r</sub> , t <sub>f</sub> | Input rise and fall times                                                     | V <sub>CC</sub> = 2.3 to 3.0V | 0      | 20              | ns/V |
|                                 |                                                                               | V <sub>CC</sub> = 3.0 to 3.6V | 0      | 10              |      |

## ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134). Voltages are referenced to GND (ground = 0V).

| SYMBOL                             | PARAMETER                                                                                             | CONDITIONS                                                                                                                     | RATING                        | UNIT |
|------------------------------------|-------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------|-------------------------------|------|
| V <sub>CC</sub>                    | DC supply voltage                                                                                     |                                                                                                                                | −0.5 to +4.6                  | V    |
| I <sub>IK</sub>                    | DC input diode current                                                                                | V <sub>I</sub> < 0                                                                                                             | −50                           | mA   |
| V <sub>I</sub>                     | DC input voltage                                                                                      | For control pins <sup>1</sup>                                                                                                  | −0.5 to +5.5                  | V    |
|                                    |                                                                                                       | For data inputs <sup>1</sup>                                                                                                   | −0.5 to V <sub>CC</sub> + 0.5 |      |
| I <sub>OK</sub>                    | DC output diode current                                                                               | V <sub>O</sub> > V <sub>CC</sub> or V <sub>O</sub> < 0                                                                         | ± 50                          | mA   |
| V <sub>O</sub>                     | DC output voltage                                                                                     | Note 1                                                                                                                         | −0.5 to V <sub>CC</sub> + 0.5 | V    |
| I <sub>O</sub>                     | DC output source or sink current                                                                      | V <sub>O</sub> = 0 to V <sub>CC</sub>                                                                                          | ± 50                          | mA   |
| I <sub>GND</sub> , I <sub>CC</sub> | DC V <sub>CC</sub> or GND current                                                                     |                                                                                                                                | ± 100                         | mA   |
| T <sub>stg</sub>                   | Storage temperature range                                                                             |                                                                                                                                | −65 to +150                   | °C   |
| P <sub>TOT</sub>                   | Power dissipation per package<br>—plastic medium-shrink (SSOP)<br>—plastic thin-medium-shrink (TSSOP) | For temperature range: −40 to +125 °C<br>above +55°C derate linearly with 11.3 mW/K<br>above +55°C derate linearly with 8 mW/K | 850<br>600                    | mW   |

## NOTE:

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 18-bit D-type flip-flop (3-State)

74ALVCH16823

## DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

| SYMBOL                             | PARAMETER                                                  | TEST CONDITIONS                                                                                                                 | LIMITS                |                       |                     | UNIT |
|------------------------------------|------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------|-----------------------|-----------------------|---------------------|------|
|                                    |                                                            |                                                                                                                                 | Temp = -40°C to +85°C |                       |                     |      |
|                                    |                                                            |                                                                                                                                 | MIN                   | TYP <sup>1</sup>      | MAX                 |      |
| V <sub>IH</sub>                    | HIGH level Input voltage                                   | V <sub>CC</sub> = 1.2V                                                                                                          | V <sub>CC</sub>       |                       |                     | V    |
|                                    |                                                            | V <sub>CC</sub> = 1.8V                                                                                                          | 0.7*V <sub>CC</sub>   | 0.9                   |                     |      |
|                                    |                                                            | V <sub>CC</sub> = 2.3 to 2.7V                                                                                                   | 1.7                   | 1.2                   |                     |      |
|                                    |                                                            | V <sub>CC</sub> = 2.7 to 3.6V                                                                                                   | 2.0                   | 1.5                   |                     |      |
| V <sub>IL</sub>                    | LOW level Input voltage                                    | V <sub>CC</sub> = 1.2V                                                                                                          |                       | –                     | GND                 | V    |
|                                    |                                                            | V <sub>CC</sub> = 1.8V                                                                                                          |                       | 0.9                   | 0.2*V <sub>CC</sub> |      |
|                                    |                                                            | V <sub>CC</sub> = 2.3 to 2.7V                                                                                                   |                       | 1.2                   | 0.7                 |      |
|                                    |                                                            | V <sub>CC</sub> = 2.7 to 3.6V                                                                                                   |                       | 1.5                   | 0.8                 |      |
| V <sub>OH</sub>                    | HIGH level output voltage                                  | V <sub>CC</sub> = 1.8 to 3.6V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = –100μA                    | V <sub>CC</sub> –0.2  | V <sub>CC</sub>       | –                   | V    |
|                                    |                                                            | V <sub>CC</sub> = 1.8V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = –6mA                             | V <sub>CC</sub> –0.4  | V <sub>CC</sub> –0.10 | –                   |      |
|                                    |                                                            | V <sub>CC</sub> = 2.3V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = –6mA                             | V <sub>CC</sub> –0.3  | V <sub>CC</sub> –0.08 | –                   |      |
|                                    |                                                            | V <sub>CC</sub> = 2.3V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = –12mA                            | V <sub>CC</sub> –0.5  | V <sub>CC</sub> –0.17 | –                   |      |
|                                    |                                                            | V <sub>CC</sub> = 2.3V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = –18mA                            | V <sub>CC</sub> –0.6  | V <sub>CC</sub> –0.26 | –                   |      |
|                                    |                                                            | V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = –12mA                            | V <sub>CC</sub> –0.5  | V <sub>CC</sub> –0.14 | –                   |      |
|                                    |                                                            | V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = –24mA                            | V <sub>CC</sub> –1.0  | V <sub>CC</sub> –0.28 | –                   |      |
| V <sub>OL</sub>                    | LOW level output voltage                                   | V <sub>CC</sub> = 1.8 to 3.6V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100μA                     |                       | GND                   | 0.20                | V    |
|                                    |                                                            | V <sub>CC</sub> = 1.8V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 6mA                              |                       | 0.09                  | 0.30                |      |
|                                    |                                                            | V <sub>CC</sub> = 2.3V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 6mA                              |                       | 0.07                  | 0.20                |      |
|                                    |                                                            | V <sub>CC</sub> = 2.3V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 12mA                             |                       | 0.15                  | 0.40                |      |
|                                    |                                                            | V <sub>CC</sub> = 2.3V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 18mA                             |                       | 0.23                  | 0.60                |      |
|                                    |                                                            | V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 12mA                             |                       | 0.14                  | 0.40                |      |
|                                    |                                                            | V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 24mA                             |                       | 0.27                  | 0.55                |      |
| I <sub>I</sub>                     | Input leakage current per control pin                      | V <sub>CC</sub> = 1.8 to 3.6V;<br>V <sub>I</sub> = 5.5V or GND                                                                  |                       | 0.1                   | 5                   | μA   |
|                                    | Input leakage current per data pin                         | V <sub>CC</sub> = 1.8 to 3.6V;<br>V <sub>I</sub> = V <sub>CC</sub> or GND                                                       |                       | 0.1                   | 5                   |      |
| I <sub>IHZ</sub> /I <sub>ILZ</sub> | Input current for common I/O pins                          | V <sub>CC</sub> = 1.8 to 2.7V;<br>V <sub>I</sub> = V <sub>CC</sub> or GND                                                       |                       | 0.1                   | 10                  | μA   |
|                                    |                                                            | V <sub>CC</sub> = 3.6V;<br>V <sub>I</sub> = V <sub>CC</sub> or GND                                                              |                       | 0.1                   | 15                  |      |
| I <sub>OZ</sub>                    | 3-State output OFF-state current                           | V <sub>CC</sub> = 1.8 to 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ;<br>V <sub>O</sub> = V <sub>CC</sub> or GND |                       | 0.1                   | 5                   | μA   |
|                                    |                                                            | V <sub>CC</sub> = 2.7 to 3.6V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ;<br>V <sub>O</sub> = V <sub>CC</sub> or GND |                       | 0.1                   | 10                  |      |
| ΔI <sub>CC</sub>                   | Additional quiescent supply current given per data I/O pin | V <sub>CC</sub> = 2.7V to 3.6V; V <sub>I</sub> = V <sub>CC</sub> – 0.6V; I <sub>O</sub> = 0                                     |                       | 150                   | 750                 | μA   |
| I <sub>BHL</sub>                   | Bus hold LOW sustaining current                            | V <sub>CC</sub> = 2.3V; V <sub>I</sub> = 0.7V <sup>2</sup>                                                                      | 45                    | –                     |                     | μA   |
|                                    |                                                            | V <sub>CC</sub> = 3.0V; V <sub>I</sub> = 0.8V <sup>2</sup>                                                                      | 75                    | 150                   |                     |      |
| I <sub>BHH</sub>                   | Bus hold HIGH sustaining current                           | V <sub>CC</sub> = 2.3V; V <sub>I</sub> = 1.7V <sup>2</sup>                                                                      | –45                   |                       |                     | μA   |
|                                    |                                                            | V <sub>CC</sub> = 3.0V; V <sub>I</sub> = 2.0V <sup>2</sup>                                                                      | –75                   | –175                  |                     |      |
| I <sub>BHLO</sub>                  | Bus hold LOW overdrive current                             | V <sub>CC</sub> = 2.7V <sup>2</sup>                                                                                             | 300                   |                       |                     | μA   |
|                                    |                                                            | V <sub>CC</sub> = 3.6V <sup>2</sup>                                                                                             | 450                   |                       |                     |      |
| I <sub>BHHO</sub>                  | Bus hold HIGH overdrive current                            | V <sub>CC</sub> = 2.7V <sup>2</sup>                                                                                             | –300                  |                       |                     | μA   |
|                                    |                                                            | V <sub>CC</sub> = 3.6V <sup>2</sup>                                                                                             | –450                  |                       |                     |      |

## NOTES:

1. All typical values are at  $T_{amb} = 25^\circ C$ .
2. Valid for data inputs of bus hold parts.

## 18-bit D-type flip-flop (3-State)

74ALVCH16823

**AC CHARACTERISTICS FOR  $V_{CC} = 2.3V$  TO  $2.7V$  RANGE AND  $V_{CC} < 2.3V$** GND = 0V;  $t_r = t_f \leq 2.0ns$ ;  $C_L = 30pF$ 

| SYMBOL            | PARAMETER                                                          | WAVEFORM | LIMITS                          |                     |     |                 |      |     |                  | UNIT |
|-------------------|--------------------------------------------------------------------|----------|---------------------------------|---------------------|-----|-----------------|------|-----|------------------|------|
|                   |                                                                    |          | $V_{CC} = 2.3 \text{ to } 2.7V$ |                     |     | $V_{CC} = 1.8V$ |      |     | $V_{CC} = 1.2V$  |      |
|                   |                                                                    |          | MIN                             | TYP <sup>1, 2</sup> | MAX | MIN             | TYP1 | MAX | TYP <sup>1</sup> |      |
| $t_{PLH}/t_{PHL}$ | Propagation delay<br>nCP to nQ <sub>n</sub>                        | 1, 5     | 1.0                             | 2.8                 | 4.9 | 1.5             | 4.5  | 7.5 | 10.6             | ns   |
| $t_{PLH}/t_{PHL}$ | Propagation delay<br>nMR to nQ <sub>n</sub>                        | 2, 5     | 1.0                             | 2.9                 | 5.0 | 1.5             | 4.6  | 7.4 | 9.9              | ns   |
| $t_{PZH}/t_{PZL}$ | 3-State output enable time<br>nOE <sub>n</sub> to nQ <sub>n</sub>  | 4, 5     | 1.0                             | 2.8                 | 5.3 | 1.5             | 4.4  | 7.7 | 10.4             | ns   |
| $t_{PHZ}/t_{PLZ}$ | 3-State output disable time<br>nOE <sub>n</sub> to nQ <sub>n</sub> | 4, 5     | 1.0                             | 2.2                 | 4.1 | 1.5             | 3.3  | 5.5 | 6.7              | ns   |
| $t_w$             | nCP pulse width                                                    | 1, 5     | 3.0                             | 1.6                 |     | 4.0             | 2.0  |     |                  | ns   |
|                   | nMR pulse width, LOW                                               | 3, 5     | 3.0                             | 0.4                 |     | 4.0             | 0.8  |     |                  |      |
| $t_{SU}$          | Set up time nD <sub>n</sub> to nCP                                 | 3, 5     | 1.2                             | 0.2                 |     | 1.5             | 0.2  |     |                  | ns   |
|                   | Set up time nCE to nCP                                             |          | 1.8                             | -0.2                |     | 2.0             | -0.2 |     |                  |      |
| $t_h$             | Hold time nD <sub>n</sub> to nCP                                   | 3, 5     | 0.8                             | -0.1                |     | 0.6             | -0.2 |     |                  | ns   |
|                   | Hold time nCE to nCP                                               |          | 0.3                             | 0.2                 |     | 0.3             | 0.2  |     |                  |      |
| $t_{rec}$         | Recovery time nMR to nCP                                           | 2, 5     | 1.0                             | 0.3                 |     | 0.8             | 0.2  |     |                  | ns   |
| $F_{max}$         | Maximum clock pulse frequency                                      | 1, 5     | 150                             | 300                 |     | 125             | 250  |     |                  | MHz  |

**NOTE:**

1. All typical values are measured at  $T_{amb} = 25^\circ C$ .
2. Typical value is measured at  $V_{CC} = 2.5V$ .

**AC CHARACTERISTICS FOR  $V_{CC} = 3.0V$  TO  $3.6V$  RANGE AND  $V_{CC} = 2.7V$** GND = 0V;  $t_r = t_f \leq 2.5ns$ ;  $C_L = 50pF$ 

| SYMBOL                             | PARAMETER                                                          | WAVEFORM | LIMITS                       |                     |     |                        |                  |     | UNIT |
|------------------------------------|--------------------------------------------------------------------|----------|------------------------------|---------------------|-----|------------------------|------------------|-----|------|
|                                    |                                                                    |          | V <sub>CC</sub> = 3.0 ± 0.3V |                     |     | V <sub>CC</sub> = 2.7V |                  |     |      |
|                                    |                                                                    |          | MIN                          | TYP <sup>1, 2</sup> | MAX | MIN                    | TYP <sup>1</sup> | MAX |      |
| t <sub>PLH</sub> /t <sub>PHL</sub> | Propagation delay<br>nCP to nQ <sub>n</sub>                        | 1, 5     | 1.0                          | 2.5                 | 3.7 | 1.0                    | 2.7              | 4.3 | ns   |
| t <sub>PLH</sub> /t <sub>PHL</sub> | Propagation delay<br>nMR to nQ <sub>n</sub>                        | 2, 5     | 1.0                          | 2.6                 | 4.0 | 1.0                    | 3.1              | 4.6 | ns   |
| t <sub>PZH</sub> /t <sub>PZL</sub> | 3-State output enable time<br>nOE <sub>n</sub> to nQ <sub>n</sub>  | 4, 5     | 1.0                          | 2.5                 | 4.3 | 1.0                    | 3.1              | 5.2 | ns   |
| t <sub>PHZ</sub> /t <sub>PLZ</sub> | 3-State output disable time<br>nOE <sub>n</sub> to nQ <sub>n</sub> | 4, 5     | 1.0                          | 2.8                 | 3.9 | 1.0                    | 3.1              | 4.3 | ns   |
| t <sub>w</sub>                     | nCP pulse width HIGH or LOW                                        | 1, 5     | 2.5                          | 1.4                 |     | 3.0                    | 1.6              |     | ns   |
|                                    | nMR pulse width HIGH or LOW                                        | 3, 5     | 2.5                          | 0.3                 |     | 3.0                    | 0.6              |     |      |
| t <sub>su</sub>                    | Set up time nD <sub>n</sub> to nCP                                 | 3, 5     | 1.2                          | 0.2                 |     | 1.5                    | 0.4              |     | ns   |
|                                    | Set up time nCE to nCP                                             |          | 1.5                          | −0.1                |     | 1.9                    | −0.1             |     |      |
| t <sub>h</sub>                     | Hold time nD <sub>n</sub> to nCP                                   | 3, 5     | 0.8                          | 0.0                 |     | 0.6                    | −0.2             |     | ns   |
|                                    | Hold time nCE to nCP                                               |          | 0.5                          | 0.1                 |     | 0.4                    | 0.1              |     |      |
| t <sub>rec</sub>                   | Recovery time nMR to nCP                                           | 2, 5     | 1.0                          | 0.2                 |     | 0.8                    | 0.1              |     | ns   |
| F <sub>max</sub>                   | Maximum clock pulse frequency                                      | 1, 5     | 200                          | 350                 |     | 150                    | 300              |     | MHz  |

**NOTES:**

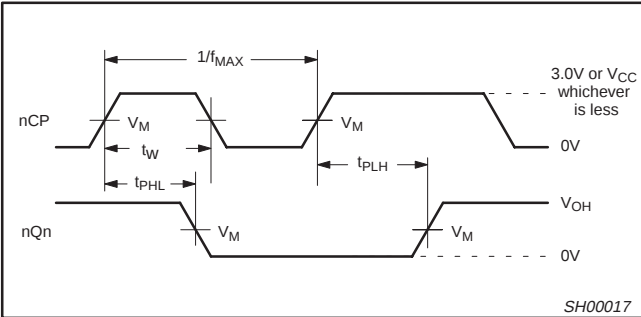
1. All typical values are measured at  $T_{amb} = 25^\circ C$ .
2. Typical value is measured at  $V_{CC} = 3.3V$ .

18-bit D-type flip-flop (3-State)

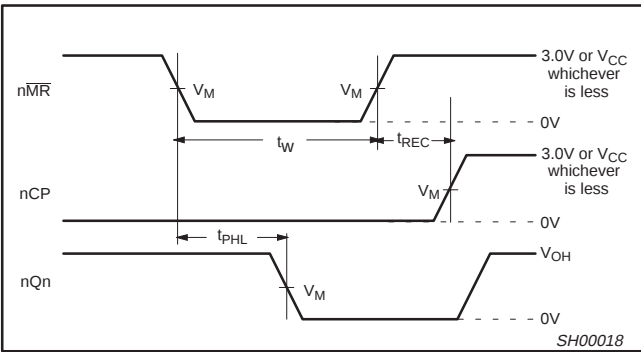
74ALVCH16823

**AC WAVEFORMS FOR  $V_{CC} = 2.3V$  TO  $2.7V$  AND  $V_{CC} < 2.3V$  RANGE**  
 $V_M = 0.5 V_{CC}$   
 $V_X = V_{OL} + 0.15V$   
 $V_Y = V_{OH} - 0.15V$   
 $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.  
 $V_I = V_{CC}$

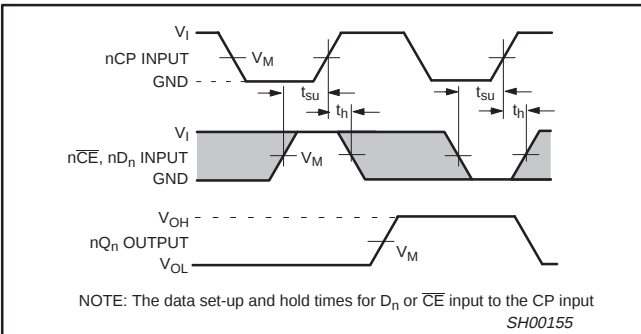
**AC WAVEFORMS FOR  $V_{CC} = 3.0V$  TO  $3.6V$  AND  $V_{CC} = 2.7V$  RANGE**  
 $V_M = 1.5 V$   
 $V_X = V_{OL} + 0.3V$   
 $V_Y = V_{OH} - 0.3V$   
 $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.  
 $V_I = 2.7V$



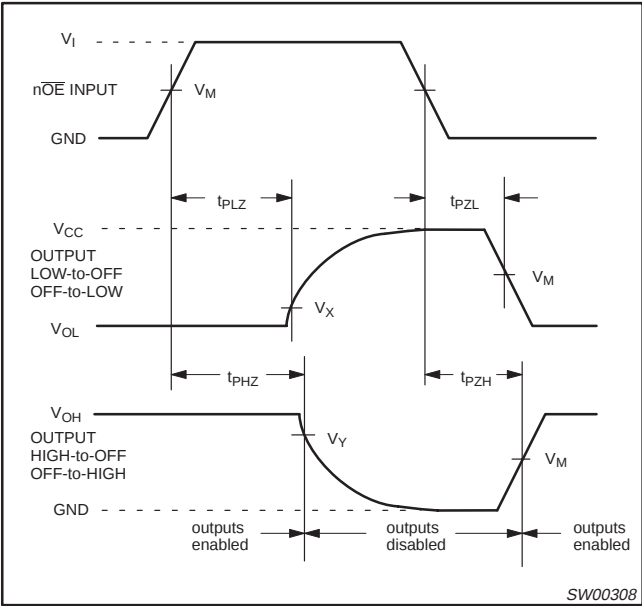
Waveform 1. Clock (nCP) to Output (nQn) Propagation Delays, Clock Pulse Width, and Maximum Clock Pulse Frequency



Waveform 2. Master Reset (MR) Pulse Width, MR to Output propagation Delay and MR to Clock Recovery Time

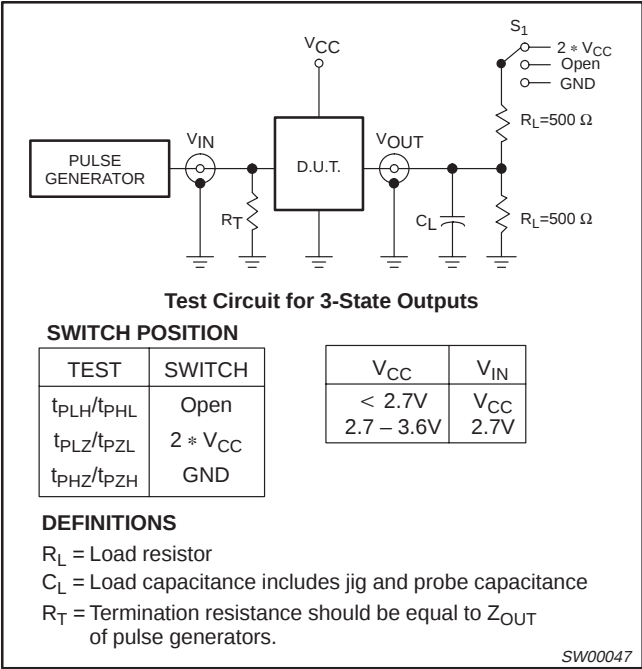


Waveform 3. Data Setup and Hold Times for the  $D_n$  or  $\overline{CE}$  input to the CP input



Waveform 4. 3-State Enable and Disable Times

TEST CIRCUIT



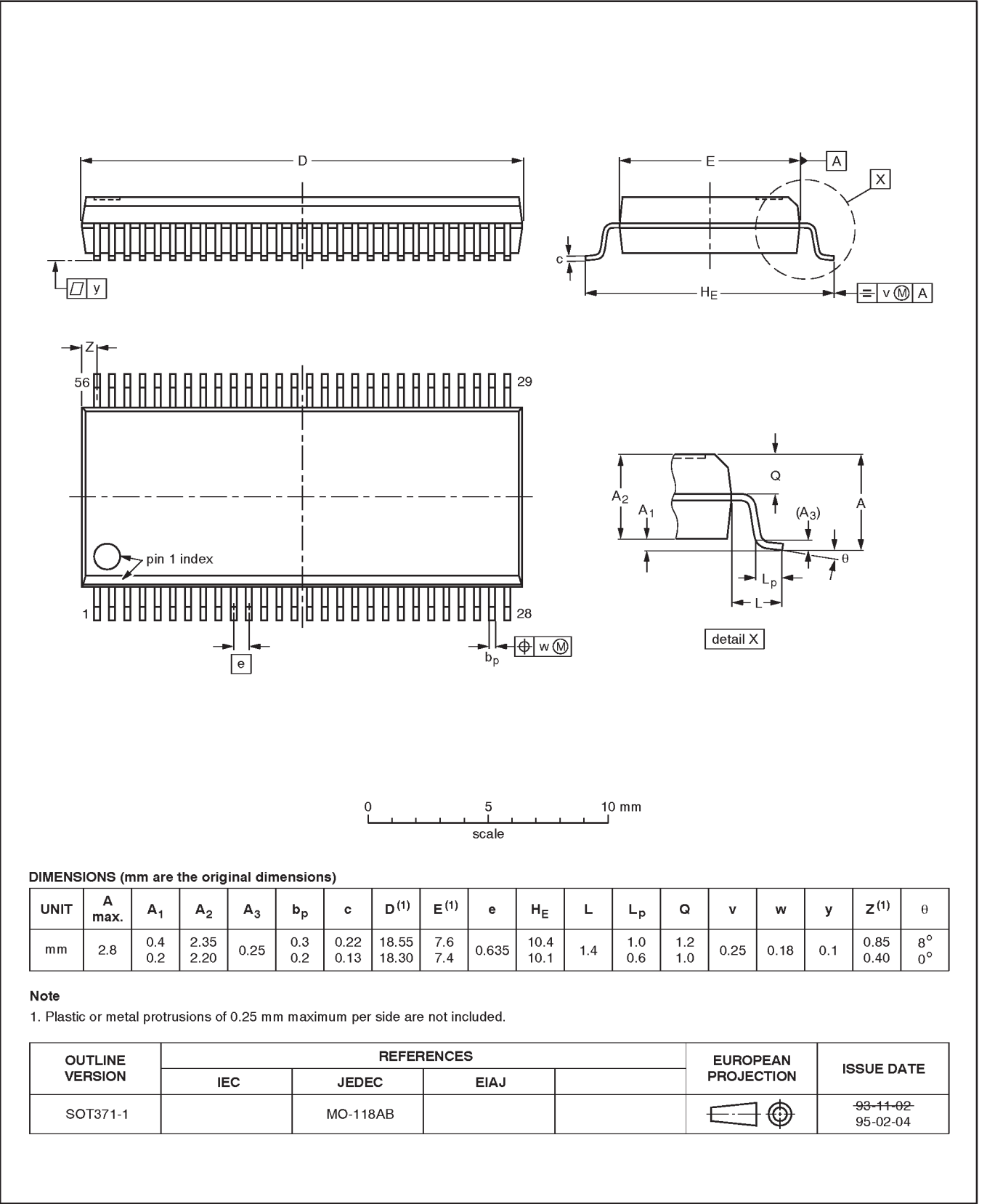
Waveform 5. Load circuitry for switching times

18-bit bus-interface D-type flip-flop  
with reset and enable (3-State)

74ALVCH16823

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1

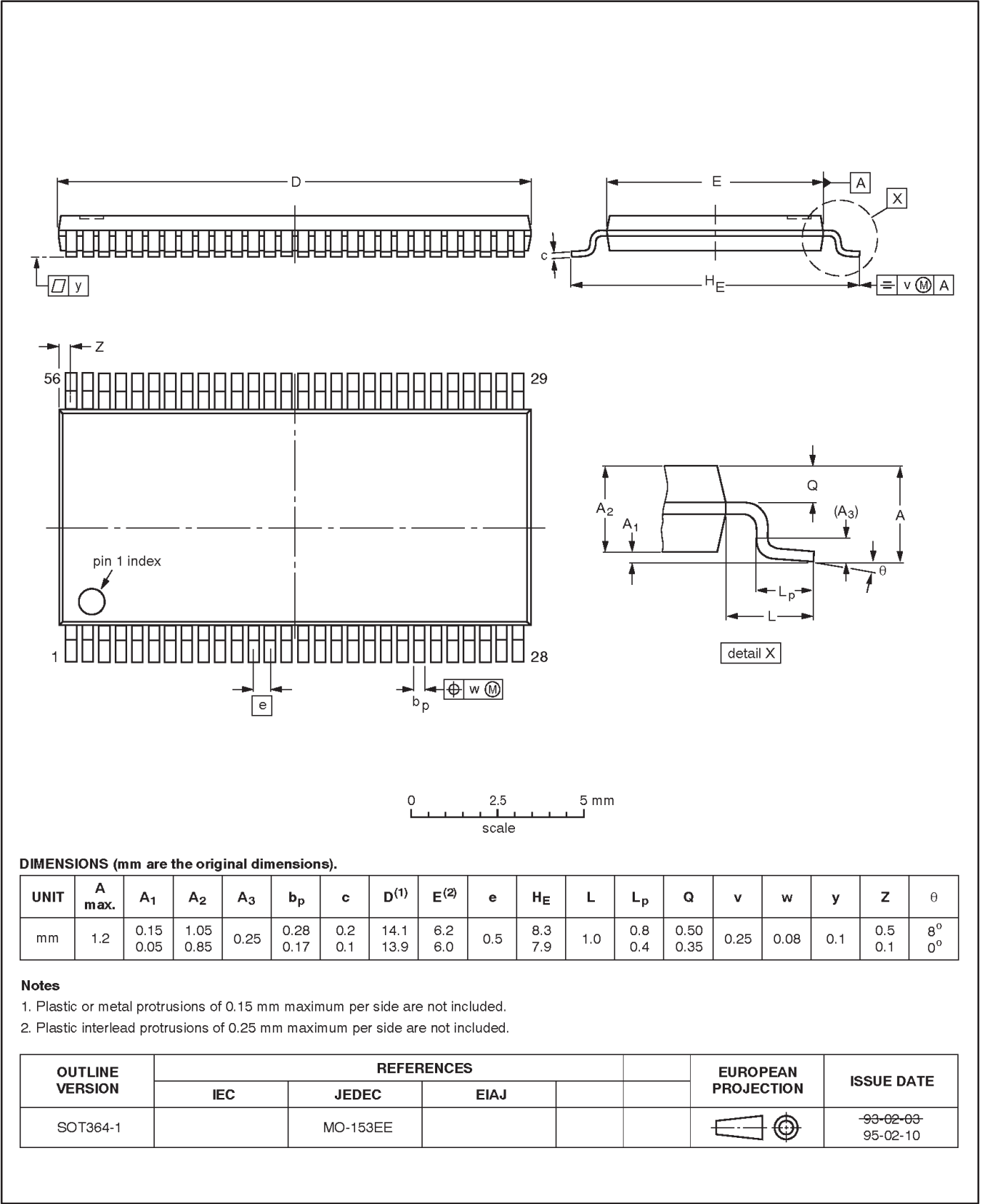


18-bit bus-interface D-type flip-flop  
with reset and enable (3-State)

74ALVCH16823

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm

SOT364-1



---

18-bit bus-interface D-type flip-flop  
with reset and enable (3-State)

---

74ALVCH16823

---

## NOTES

# 18-bit bus-interface D-type flip-flop with reset and enable (3-State)

74ALVCH16823

## Data sheet status

| Data sheet status         | Product status | Definition [1]                                                                                                                                                                                                                                             |
|---------------------------|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Objective specification   | Development    | This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.                                                                                                          |
| Preliminary specification | Qualification  | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
| Product specification     | Production     | This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.                                                       |

[1] Please consult the most recently issued datasheet before initiating or completing a design.

## Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Application information** — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

## Disclaimers

**Life support** — These products are not designed for use in life support appliances, devices or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

**Right to make changes** — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

Philips Semiconductors  
811 East Arques Avenue  
P.O. Box 3409  
Sunnyvale, California 94088-3409  
Telephone 800-234-7381

© Copyright Philips Electronics North America Corporation 1998  
All rights reserved. Printed in U.S.A.

print code

Date of release: 05-96

Document order number:

9397-750-04554

*Let's make things better.*