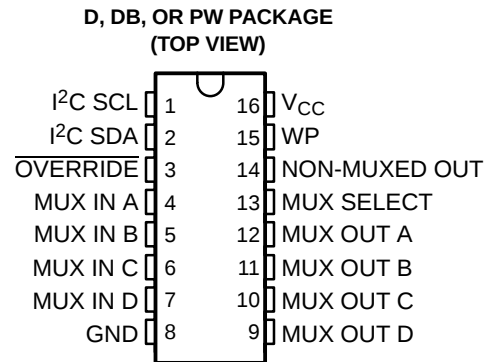


FEATURES

- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Useful for Jumperless Configuration of PC Motherboard**
- **Inputs Accept Voltages to 5.5 V**
- **MUX OUT Signals are 2.5-V Outputs**
- **NON-MUXED OUT Signal is a 3.3-V Output**
- **Minimum of 1000 Write Cycles**
- **Minimum of 10 Years Data Retention**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**



DESCRIPTION/ORDERING INFORMATION

This 4-bit 1-of-2 multiplexer with I²C input interface is designed for 3-V to 3.6-V V_{CC} operation.

The PCA8550 is designed to multiplex four bits of data from parallel inputs or from I²C input data stored in a nonvolatile register. An additional bit of register output also is provided, which is latched to prevent changes in the output value during the write cycle. The factory default for the contents of the register is all low. These stored values can be read from, or written to, using the I²C bus. The ability to control writing to the register is provided by the write protect (WP) input. The override ($\overline{\text{OVERRIDE}}$) input forces all the register outputs to a low.

This device provides a fast-mode (400 kbit/s) or standard-mode (100 kbit/s) I²C serial interface for data input and output. The implementation is as a slave. The device address is specified in the I²C interface definition table. Both of the I²C Schmitt-trigger inputs (SCL and SDA) provide integrated pullup resistors and are 5-V tolerant.

The PCA8550 requires a monotonic power-supply ramp at start-up in the region of 1.1 V to 2.5 V. The nonvolatile registers and I²C state machine initialize to their default states after this V_{CC} level is passed.

The PCA8550 is characterized for operation from 0°C to 70°C.

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	SOIC – D	Tube of 40	PCA8550D	PCA8550
		Reel of 2500	PCA8550DR	
	SSOP – DB	Reel of 2000	PCA8550DBR	
	TSSOP – PW	Reel of 2000	PCA8550PWR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PCA8550

NONVOLATILE 5-BIT REGISTER WITH I²C INTERFACE

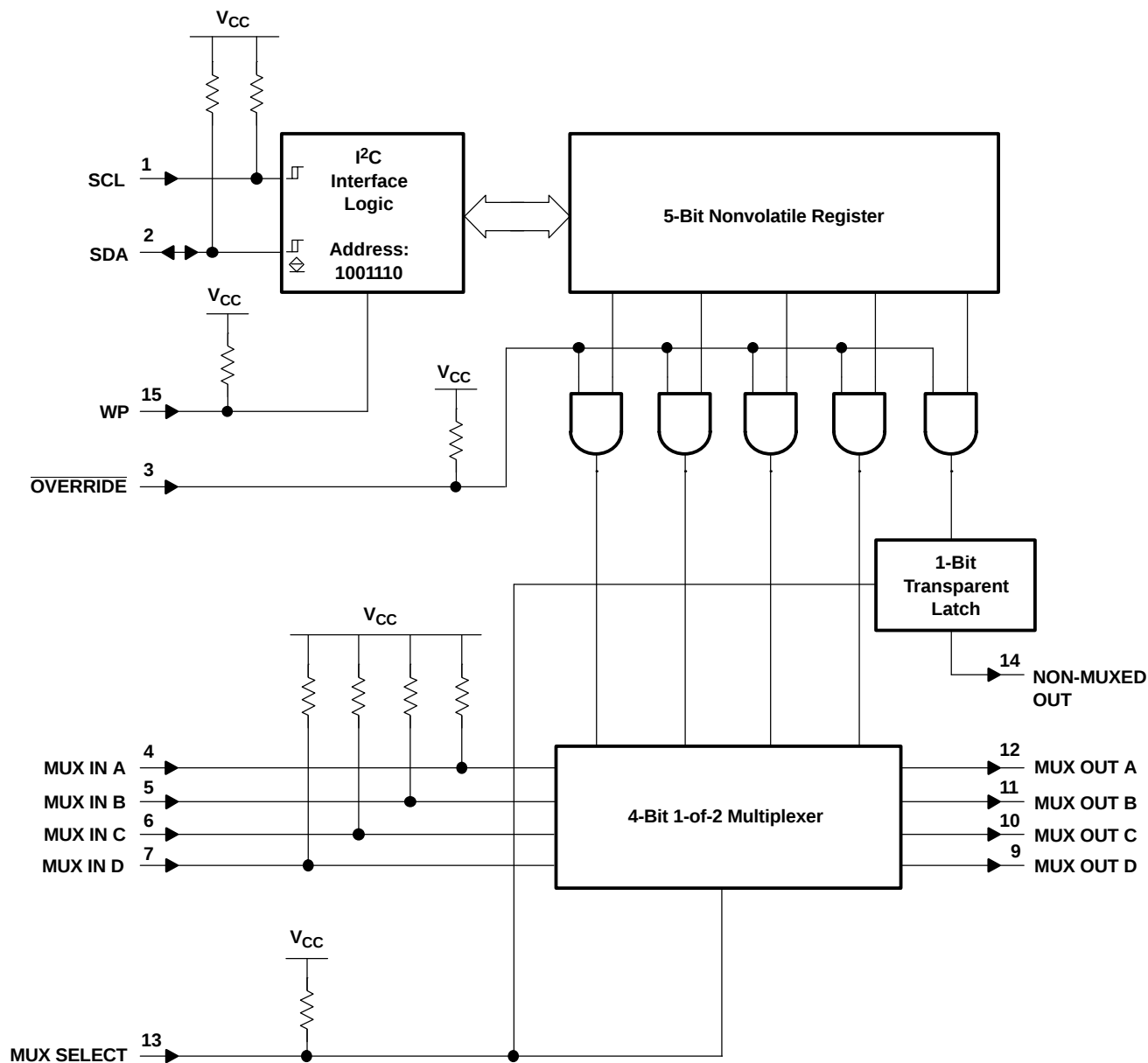
SCPS050C—MARCH 1999—REVISED MAY 2005

FUNCTION TABLE

INPUTS		OUTPUTS	
MUX SELECT	OVERRIDE	MUX OUT	NON-MUXED OUT
L	L	L	L
L	H	Nonvolatile register	Nonvolatile register
H	X	MUX IN	Latched NON-MUXED OUT ⁽¹⁾

(1) The latched NON-MUXED OUT state is the value present on the NON-MUXED OUT output at the time the MUX SELECT input transitions from the low to the high state.

LOGIC DIAGRAM (POSITIVE LOGIC)



I²C Interface

I²C communication with this device is initiated by a master sending a start condition, a high-to-low transition on the serial data (SDA) input/output while the serial clock (SCL) input is high. After the start condition, the device address byte is sent, MSB first, including the data-direction bit (R/W). This device does not respond to the general call address. After receiving the valid address byte, this device responds with an acknowledge, a low on the SDA input/output during the high of the acknowledge-related clock pulse.

The data byte follows the address acknowledge. If the R/W bit is high, the data from this device are the values read from the nonvolatile register. If the R/W bit is low, the data are from the master, to be written into the register. A valid data byte is one in which the three high-order bits are low. The first valid data byte that is received is written into the register, following the stop condition. If an invalid data byte is received, it is acknowledged, but is not written into the register. The data byte is followed by an acknowledge sent from this device. If other data bytes are sent from the master, following the acknowledge, they are ignored by this device.

A stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master. If the WP input is low during the falling edge of the first valid data byte acknowledge on the SCL input and the R/W bit is low, the stop condition causes the I²C interface logic to write the data byte value into the nonvolatile register. Data are written only if complete bytes are received and acknowledged. Writing to the register takes time (t_{wr}), during which the device does not respond to its slave address. If the WP input is high, the I²C interface logic does not write to the register.

I²C Interface Definition Table

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Address	H	L	L	H	H	H	L	R/W
Data	L	L	L	NON-MUXED OUT	MUX OUT D	MUX OUT C	MUX OUT B	MUX OUT A

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	−0.5	6.5	V
V _I	Input voltage range ⁽²⁾	−0.5	6.5	V
V _O	Output voltage range	SDA ⁽²⁾	−0.5	6.5
		MUX OUT outputs ⁽²⁾	−0.5	2.9
		NON-MUXED OUT output ⁽²⁾⁽³⁾	−0.5	V _{CC} + 0.5
I _{IK}	Input clamp current	V _I < 0	−50	mA
I _{OK}	Output clamp current	V _O < 0 or V _O > V _{CC} ⁽³⁾	−50, +10	mA
I _{IOK}	Input/output clamp current	V _O < 0	−50	mA
I _O	Continuous output current	V _O = 0 to V _{CC} ⁽³⁾	±15	mA
	Continuous current through V _{CC} or GND		±30	mA
θ _{JA}	Package thermal impedance ⁽⁴⁾	D package	113	°C/W
		DB package	131	
		PW package	149	
T _{stg}	Storage temperature range	−65	85	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51.

PCA8550

NONVOLATILE 5-BIT REGISTER WITH I²C INTERFACE

SCPS050C—MARCH 1999—REVISED MAY 2005



Recommended Operating Conditions

			MIN	MAX	UNIT
V _{CC}	Supply voltage		3	3.6	V
V _{IH}	High-level input voltage	SCL, SDA	2.7	4	V
		OVERIDE, MUX IN, MUX SELECT, WP	2	4	
V _{IL}	Low-level input voltage	SCL, SDA	−0.5	0.9	V
		OVERIDE, MUX IN, MUX SELECT, WP	−0.5	0.8	
I _{OH}	High-level output current	MUX OUT, NON-MUXED OUT		−2	mA
I _{OL}	Low-level output current	SDA		6	mA
		MUX OUT, NON-MUXED OUT		2	
Δt/Δv	Input transition rise or fall rate	OVERIDE, MUX IN, MUX SELECT, WP		10	ns/V
T _A	Operating free-air temperature		0	70	°C

Electrical Characteristics

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V _{IK}	Input diode clamp voltage	I _I = −18 mA	−1.5		V
V _{hys} ⁽¹⁾	SCL, SDA		0.19		V
V _{OH}	MUX OUT	I _{OH} = −100 μA	2	2.625	V
		I _{OH} = −1 mA	1.7	2.625	
	NON-MUXED OUT	I _{OH} = −100 μA	2.4	3.6	
		I _{OH} = −2 mA	2	3.6	
V _{OL}	MUX OUT	I _{OL} = 100 μA	−0.3	0.4	V
		I _{OL} = 2 mA	−0.3	0.7	
	NON-MUXED OUT	I _{OL} = 100 μA	−0.5	0.4	
		I _{OL} = 2 mA	−0.5	0.7	
	SDA	I _{OL} = 3 mA		0.4	
		I _{OL} = 6 mA		0.6	
I _{IH}	SCL, SDA	V _{IH} = 2.4 V	−1.5	−12	μA
	OVERIDE, MUX SELECT, WP		−20	−100	
	MUX IN		−0.166	−0.75	mA
I _{IL}	SCL, SDA	V _{IL} = 0.4 V	−7	−32	μA
	OVERIDE, MUX SELECT, WP		−86	−267	
	MUX IN		−0.72	−2	mA
I _{CC}	During read or write cycle	V _I = 0 to V _{CC} , I _O = 0, V _{CC} = 3.3 V		10	mA
	Not during read or write cycle	V _I = V _{CC} , I _O = 0		500	μA
C _i		V _I = V _{CC} or GND		10	pF

(1) V_{hys} is the hysteresis of Schmitt-trigger inputs.

Nonvolatile Storage Specifications

PARAMETER	SPECIFICATIONS
Write time (t _{wr})	10 ms, typical
Memory-cell data retention	10 years, minimum
Maximum number of memory-cell write cycles	1000 cycles, minimum

I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
		MIN	MAX	
f_{SCL}	I ² C clock frequency	10	400	kHz
t_{SCH}	I ² C clock high time	600		ns
t_{SCL}	I ² C clock low time	1.3		μs
t_{SP}	I ² C spike time	0	50	ns
t_{SDS}	I ² C serial data setup time	100		ns
t_{SDH}	I ² C serial data hold time	0	900	ns
t_{ICR}	I ² C input rise time	20	300	ns
t_{ICF}	I ² C input fall time	20	300	ns
t_{OCF}	I ² C output fall time (10-pF to 400-pF bus)	$20 + 0.1 C_b^{(1)}$	250	ns
t_{BUF}	I ² C bus free time between stop and start	1.3		μs
t_{STS}	I ² C start or repeated start condition setup	600		ns
t_{STH}	I ² C start or repeated start condition hold	600		ns
t_{SPS}	I ² C stop condition setup	600		ns
$C_b^{(1)}$	I ² C bus capacitive load		400	pF

(1) C_b = capacitance of one bus line in pF

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 2](#))

PARAMETER		FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
				MIN	MAX	
t_{MPD}	Mux input to output propagation delay	MUX IN	MUX OUT	20		ns
t_{SOV}	MUX SELECT to output valid	MUX SELECT	Output valid	22		ns
t_{OVN}	$\overline{\text{OVERRIDE}}$ to NON-MUXED OUT output delay	$\overline{\text{OVERRIDE}}$	NON-MUXED OUT	15		ns
t_{OVM}	$\overline{\text{OVERRIDE}}$ to MUX OUT output delay	$\overline{\text{OVERRIDE}}$	MUX OUT	25		ns
t_{SU}	Setup time	WP	Falling edge of first valid data byte acknowledge on the SCL input	30		ns
t_H	Hold time	WP	Falling edge of first valid data byte acknowledge on the SCL input	120		ns
t_r	Output rise time			1	3	ns/V
t_f	Output fall time			1	3	ns/V

PARAMETER MEASUREMENT INFORMATION

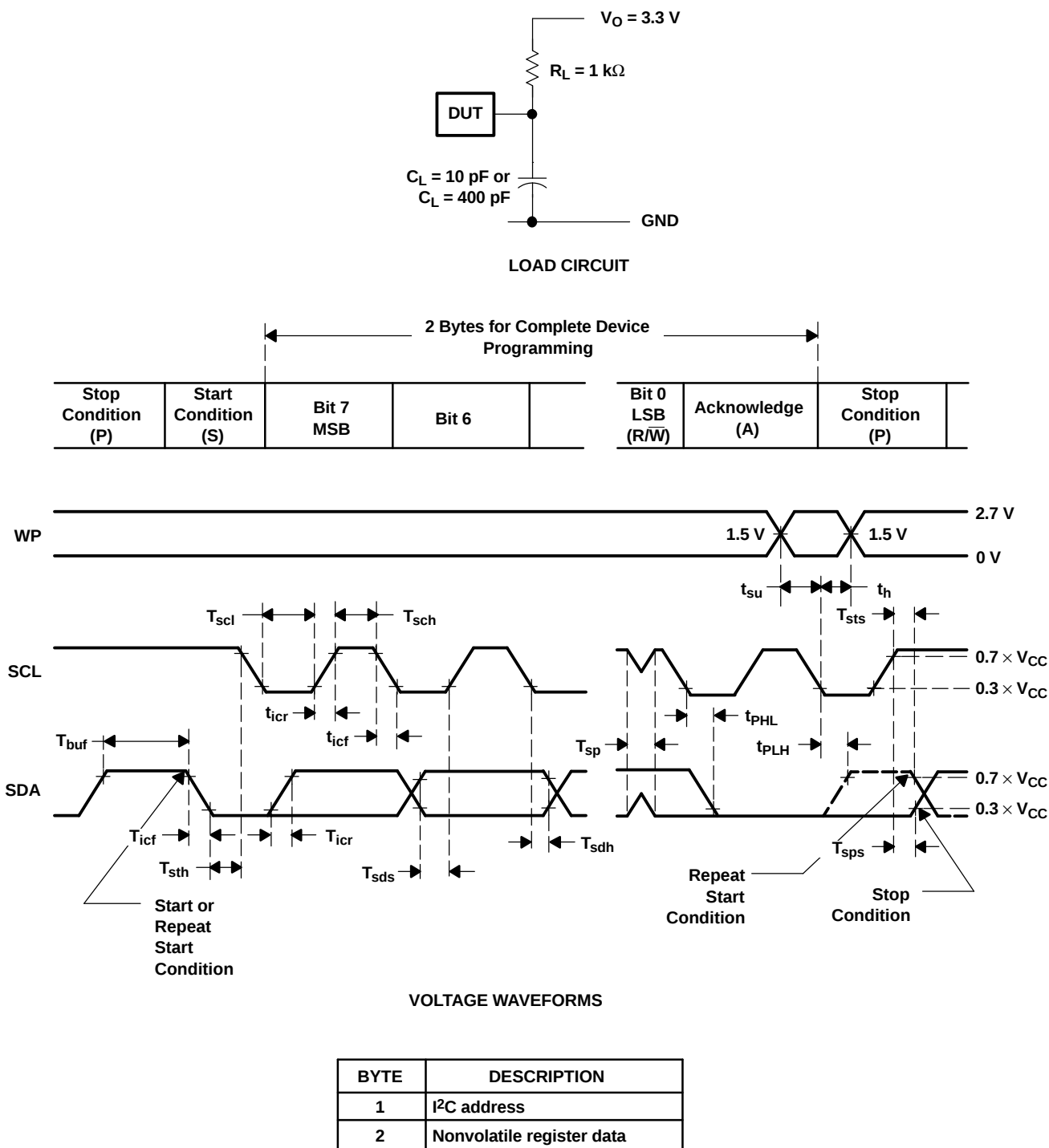
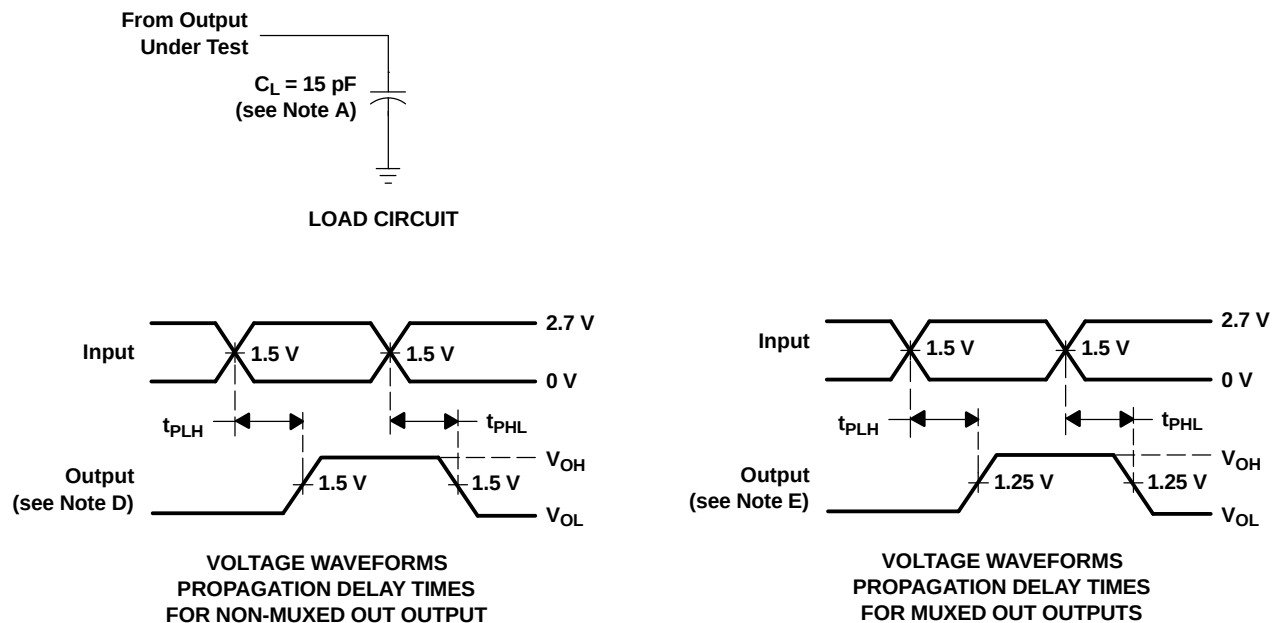


Figure 1. I²C Interface Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 C. The outputs are measured one at a time, with one transition per measurement.
 D. t_{PLH} and t_{PHL} are the same as t_{SOV} and t_{OVN} .
 E. t_{PLH} and t_{PHL} are the same as t_{mpd} , t_{SOV} , and t_{ovm} .

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
PCA8550D	ACTIVE	SOIC	D	16		TBD	Call TI	Call TI
PCA8550DBR	ACTIVE	SSOP	DB	16		TBD	Call TI	Call TI
PCA8550DBRE4	ACTIVE	SSOP	DB	16		TBD	Call TI	Call TI
PCA8550DE4	ACTIVE	SOIC	D	16		TBD	Call TI	Call TI
PCA8550DR	ACTIVE	SOIC	D	16		TBD	Call TI	Call TI
PCA8550DRE4	ACTIVE	SOIC	D	16		TBD	Call TI	Call TI
PCA8550PWR	PREVIEW	TSSOP	PW	16	2000	TBD	Call TI	Call TI
PCA8550PWRE4	ACTIVE	TSSOP	PW	16		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

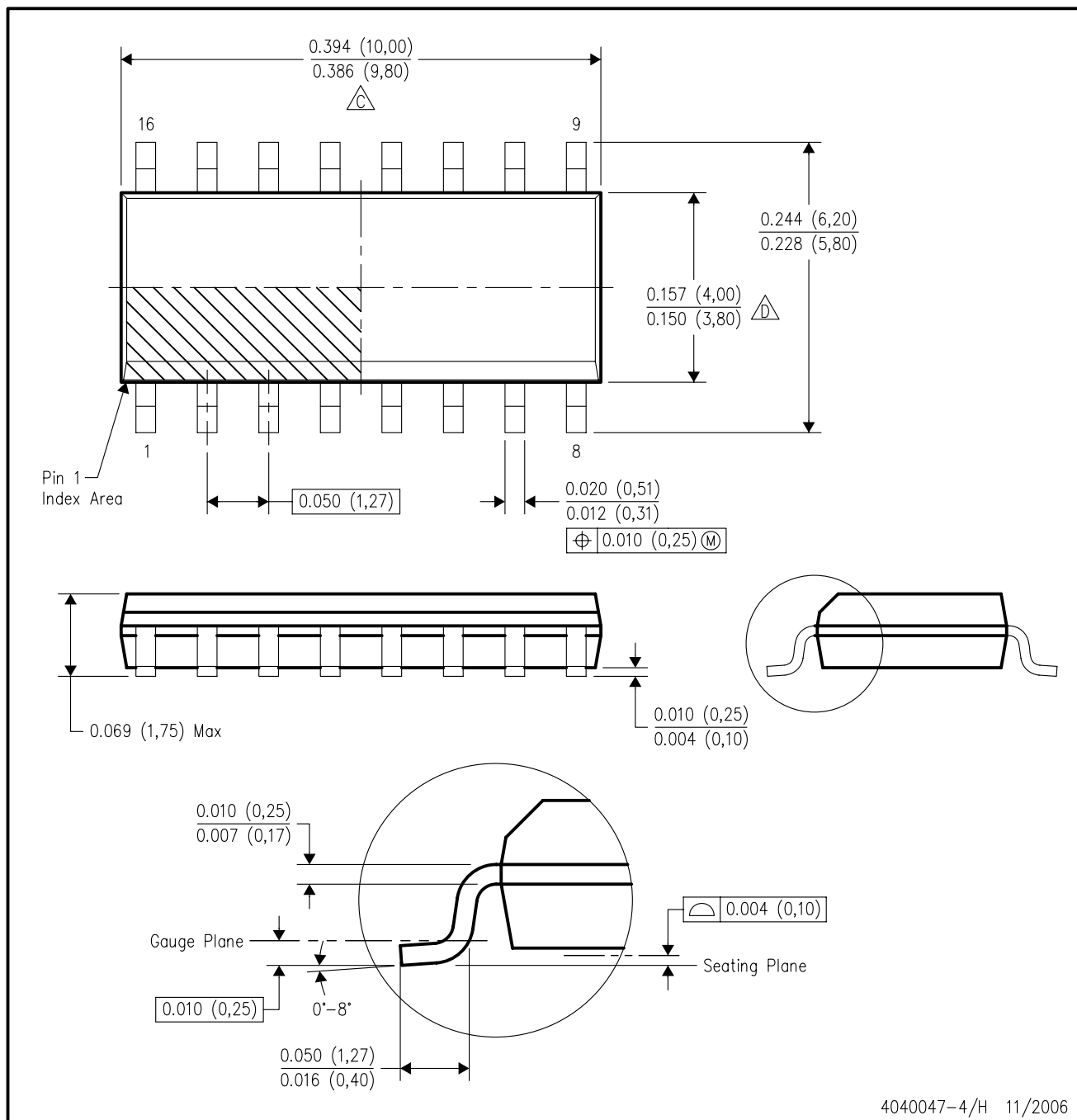
14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE

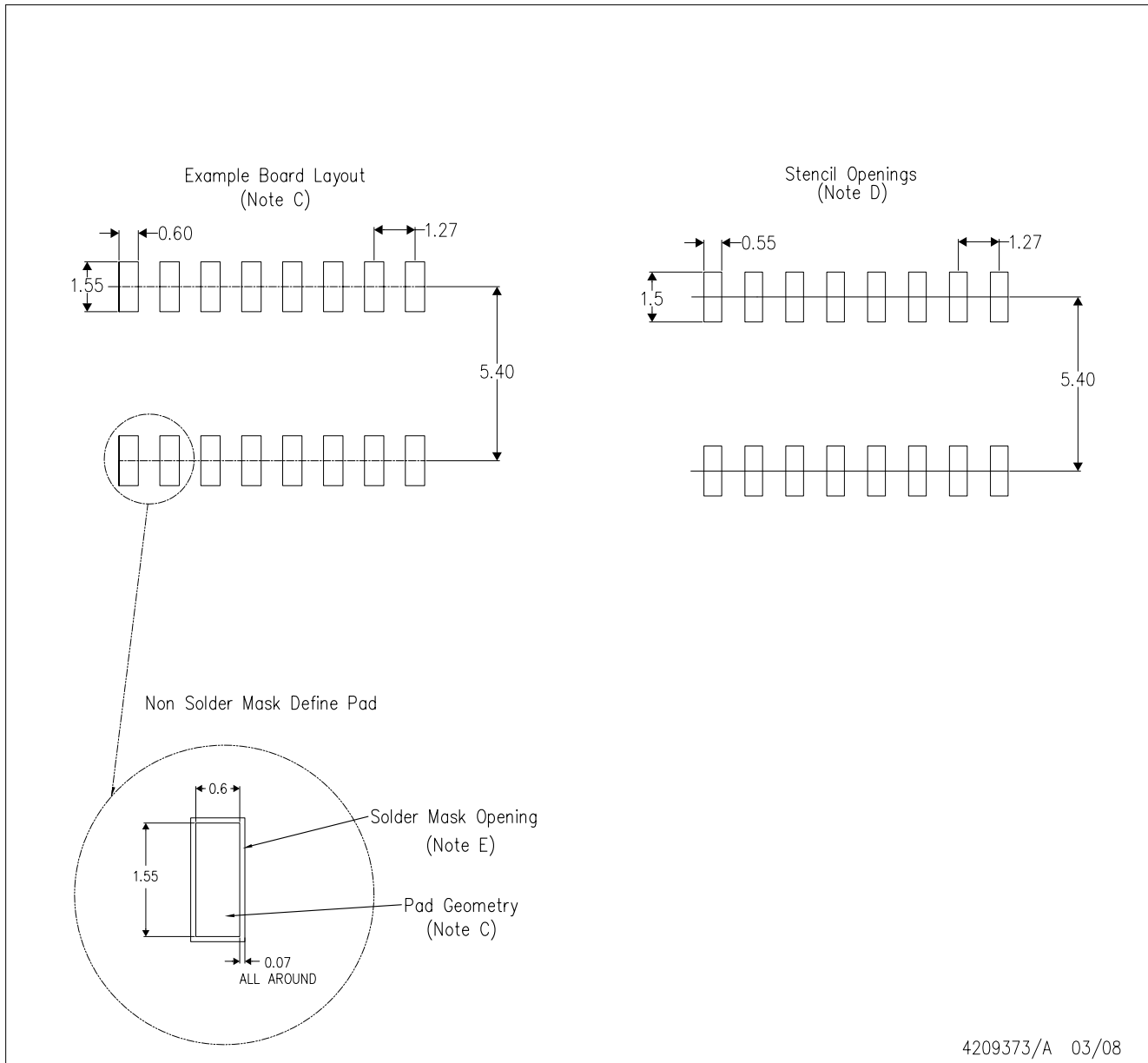


4040047-4/H 11/2006

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AC.

D(R-PDSO-G16)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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