

To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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EOL announced Product

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MOS FIELD EFFECT TRANSISTOR

2SK3659

SWITCHING

N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK3659 is N-channel MOS FET device that features a low on-state resistance and excellent switching characteristics, designed for low voltage high current applications such as DC/DC converter with synchronous rectifier.

ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3659	Isolated TO-220

FEATURES

- 4.5V drive available.
- Low on-state resistance,
 $R_{DS(on)1} = 5.7 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 40 \text{ A)}$
- Low gate charge,
 $Q_G = 32 \text{ nC TYP. (} V_{DD} = 16 \text{ V, } V_{GS} = 10 \text{ V, } I_D = 65 \text{ A)}$
- Built-in gate protection diode.
- Avalanche capability ratings.
- Isolated TO-220 package.

ABSOLUTE MAXIMUM RATING ($T_A = 25^\circ\text{C}$)

Drain to source voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	20	V
Gate to source voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 20	V
Drain current (DC) ($T_C = 25^\circ\text{C}$)	$I_{D(DC)}$	± 65	A
Drain current (pulse) ^{Note1}	$I_{D(pulse)}$	± 260	A
Total power dissipation ($T_A = 25^\circ\text{C}$)	P_{T1}	2.0	W
Total power dissipation ($T_C = 25^\circ\text{C}$)	P_{T2}	25	W
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$
Single Avalanche Current ^{Note2}	I_{AS}	35	A
Single Avalanche Energy ^{Note2}	E_{AS}	122	mJ

Note 1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

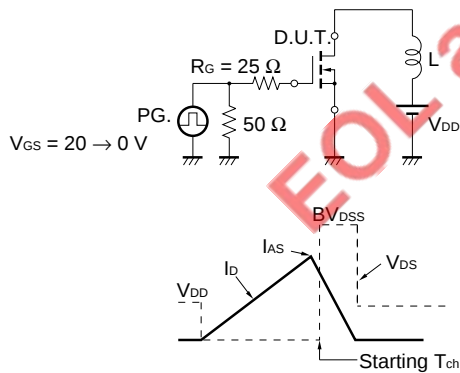
2. Starting $T_{ch} = 25^\circ\text{C}$, $V_{DD} = 10 \text{ V}$, $R_G = 25 \Omega$, $V_{GS} = 20 \rightarrow 0 \text{ V}$

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 Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

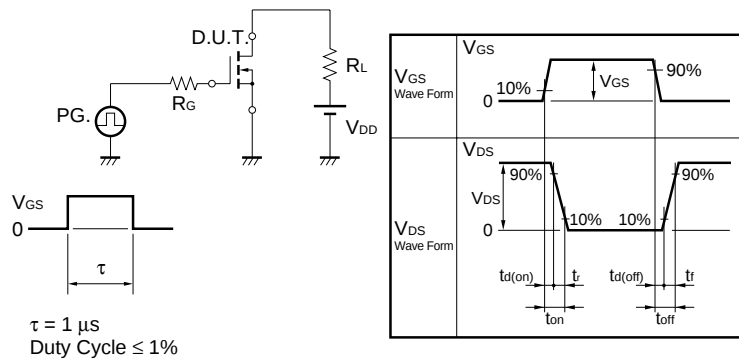
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristics	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V			10	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μA
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5		2.5	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 40 A	15			S
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = 10 V, I _D = 40 A		4.6	5.7	mΩ
	R _{DS(on)2}	V _{GS} = 4.5 V, I _D = 40 A		7.1	9.9	mΩ
Input Capacitance	C _{iss}	V _{DS} = 10 V		1700		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		700		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		250		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 10 V, I _D = 40 A		16		ns
Rise Time	t _r	V _{GS} = 10 V		14		ns
Turn-off Delay Time	t _{d(off)}	R _G = 10 Ω		50		ns
Fall Time	t _f			12		ns
Total Gate Charge	Q _G	V _{DD} = 16 V		32		nC
Gate to Source Charge	Q _{GS}	V _{GS} = 10 V		6.0		nC
Gate to Drain Charge	Q _{GD}	I _D = 65 A		8.3		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 65 A, V _{GS} = 0 V		1.0		V
Reverse Recovery Time	t _{rr}	I _F = 65 A, V _{GS} = 0 V		45		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		34		nC

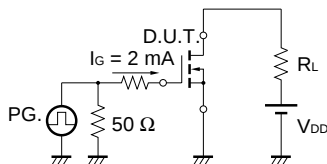
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

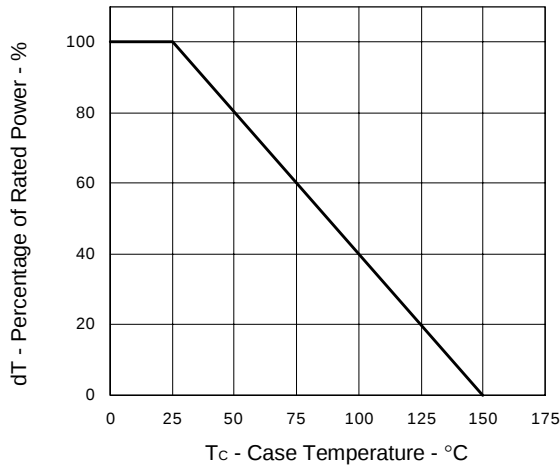


TEST CIRCUIT 3 GATE CHARGE

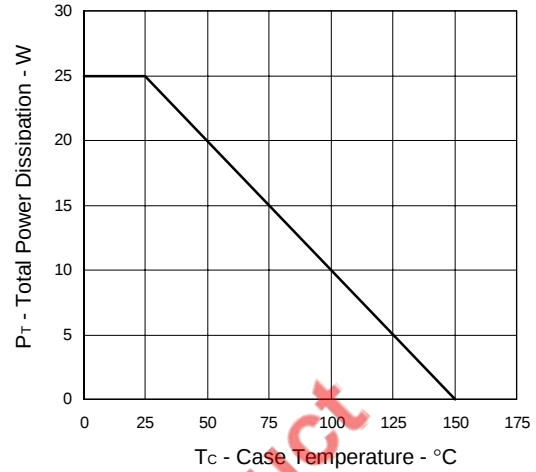


TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)

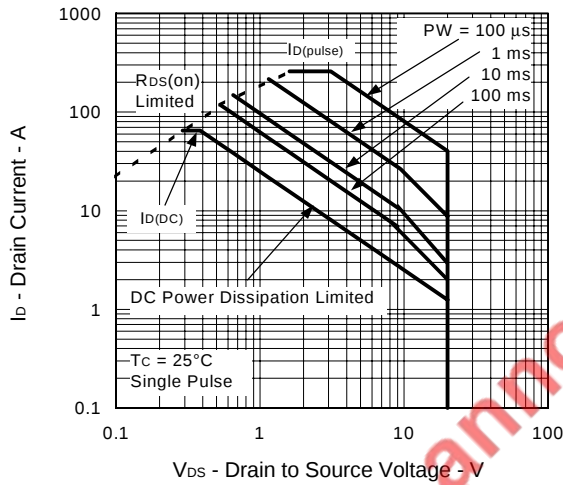
DERATING FACTOR OF FORWARD BIAS
SAFE OPERATING AREA



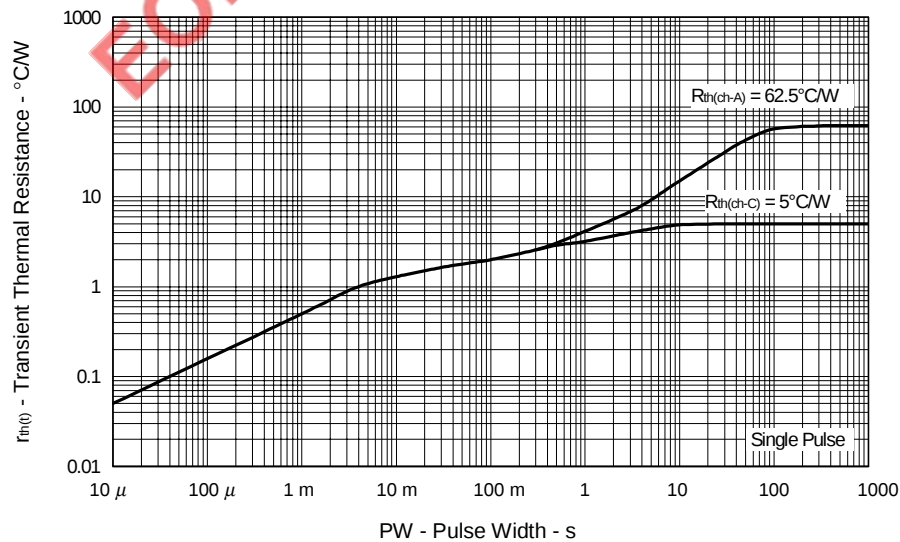
TOTAL POWER DISSIPATION vs.
CASE TEMPERATURE



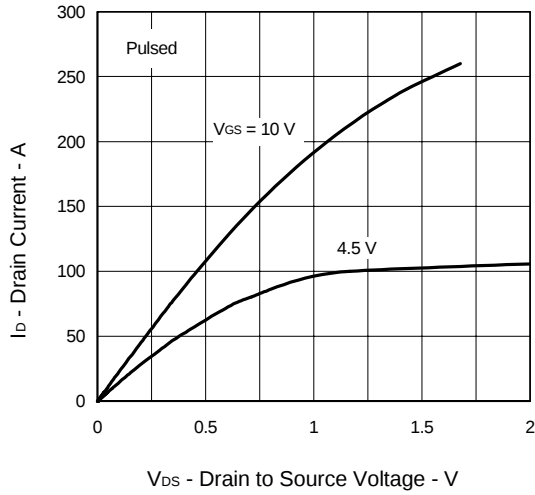
FORWARD BIAS SAFE OPERATING AREA



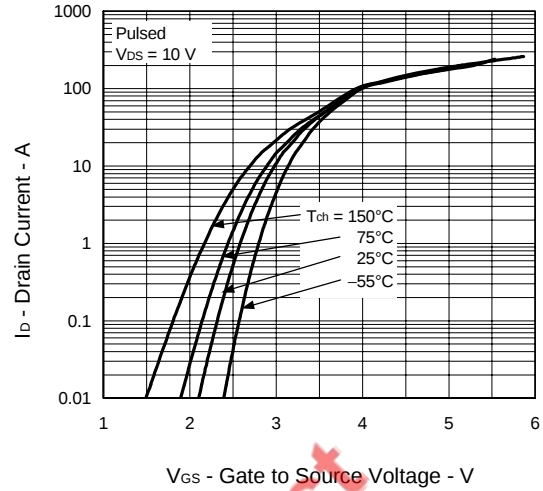
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



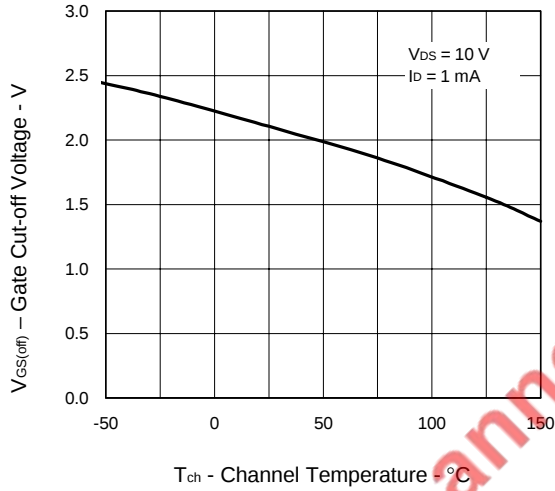
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



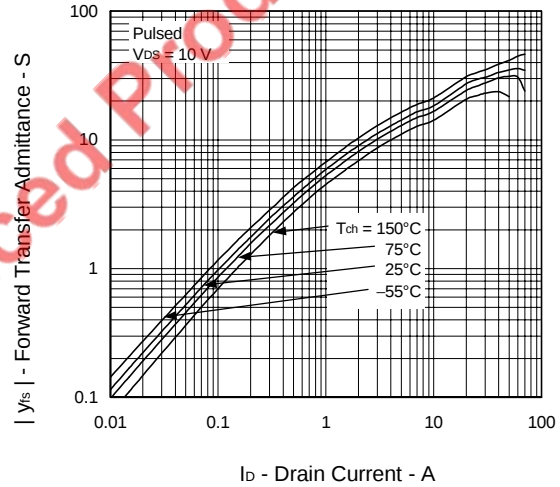
FORWARD TRANSFER CHARACTERISTICS



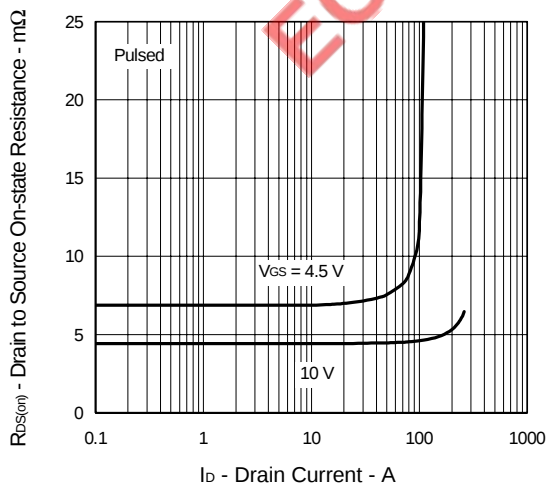
GATE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



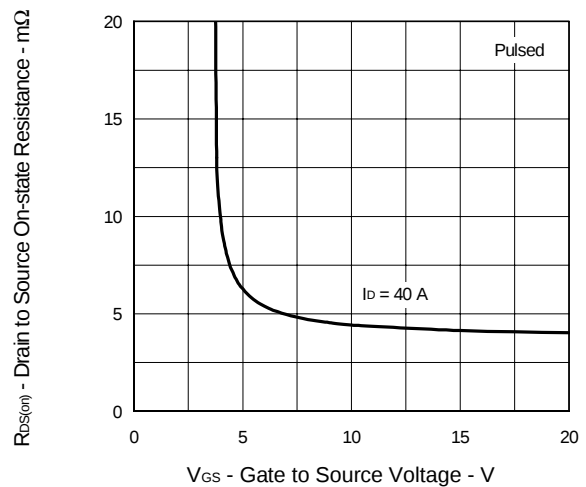
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



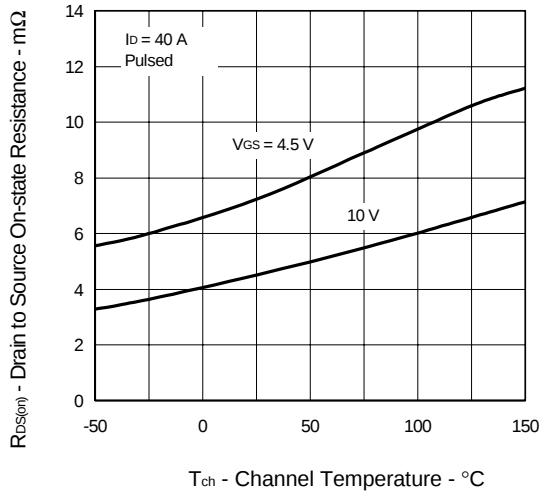
DRAIN TO SOURCE ON-STATE
RESISTANCE vs. DRAIN CURRENT



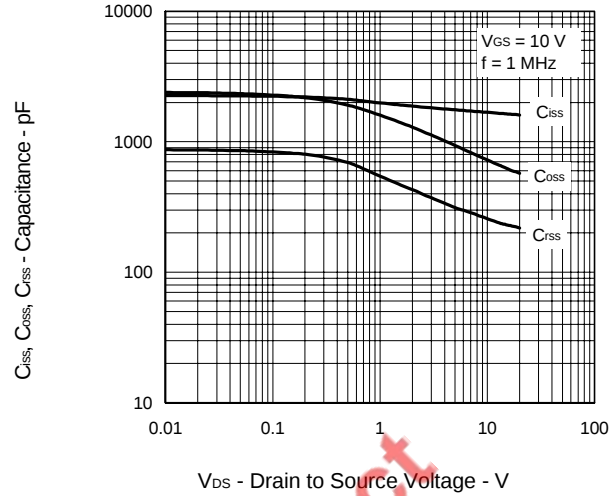
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



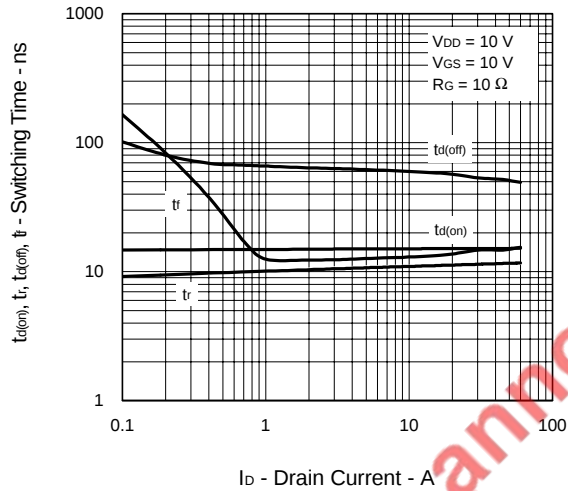
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



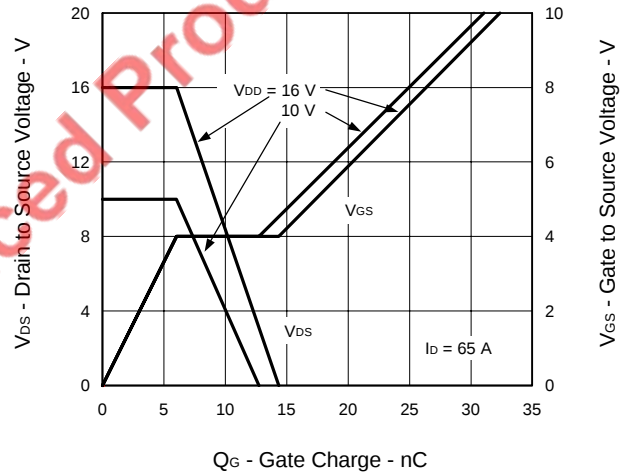
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



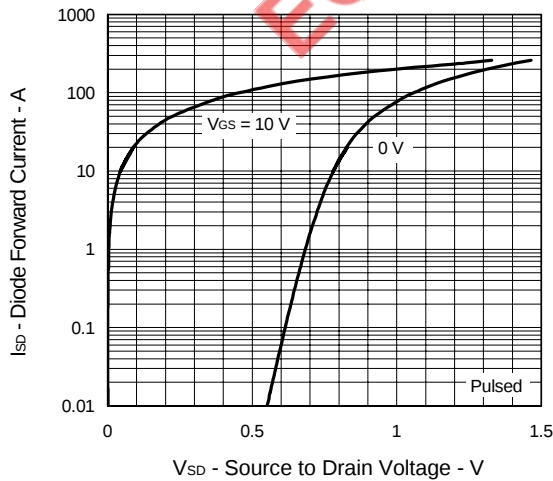
SWITCHING CHARACTERISTICS



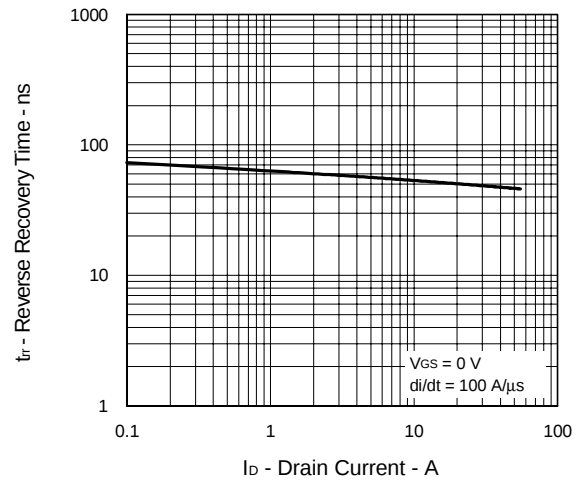
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



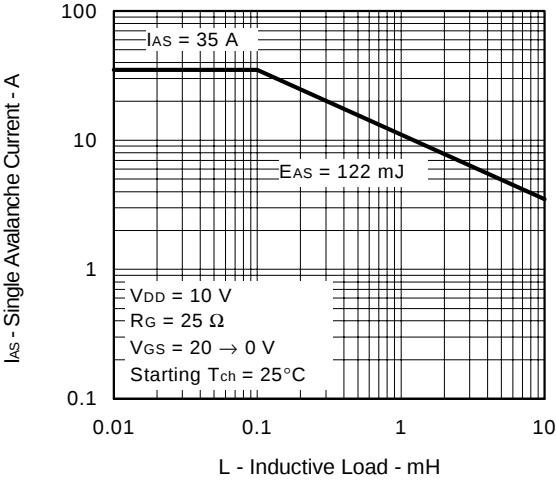
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



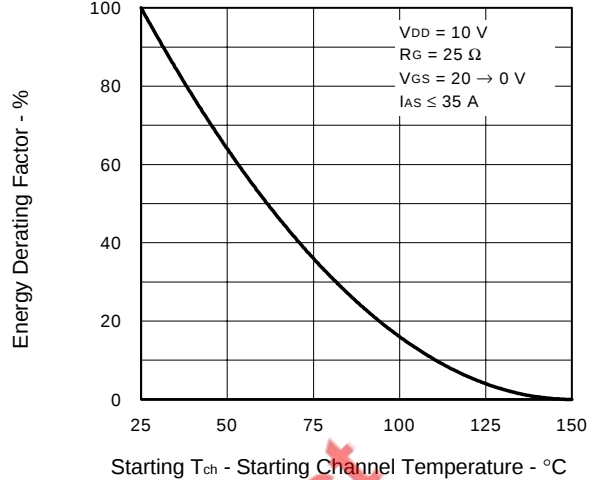
REVERSE RECOVERY TIME vs. DRAIN CURRENT



SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD



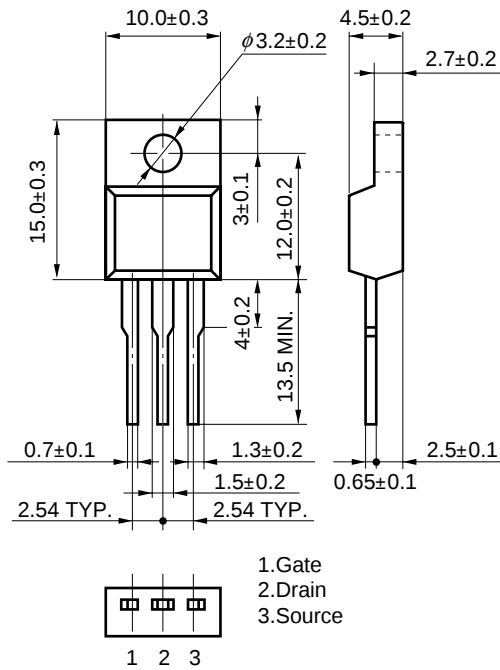
SINGLE AVALANCHE ENERGY
DERATING FACTOR



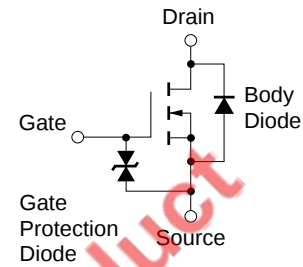
EOL announced Product

PACKAGE DRAWING (Unit: mm)

Isolated TO-220 (MP-45F)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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