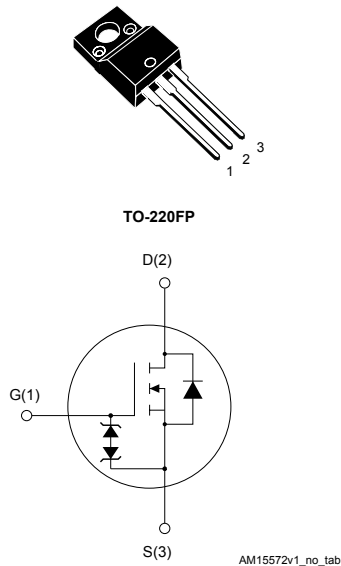


## N-channel 900 V, 1.90 $\Omega$ typ., 4 A MDmesh K5 Power MOSFET in a TO-220FP package



### Features

Order code	$V_{DS}$	$R_{DS(on)}$ max.	$I_D$
STF4N90K5	900 V	2.10 $\Omega$	4 A

- Ultra-low gate charge
- Very low FoM (figure of merit)
- Zener-protected
- 100% avalanche tested

### Applications

- Switching applications

### Description

This very high voltage N-channel Power MOSFET is designed using MDmesh K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

#### Product status link

[STF4N90K5](#)

#### Product summary

<b>Order code</b>	STF4N90K5
<b>Marking</b>	4N90K5
<b>Package</b>	TO-220FP
<b>Packing</b>	Tube

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	4	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	2.5	
$I_{DM}^{(1)}$	Drain current (pulsed)	16	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	20	W
$V_{iso}$	Insulation withstand voltage (RMS) from all three leads to external heat sink ( $t = 1\text{ s}$ ; $T_C = 25\text{ }^\circ\text{C}$ )	2.5	kV
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
$dv/dt^{(3)}$	MOSFET $dv/dt$ ruggedness	50	V/ns
$T_{stg}$	Storage temperature range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating junction temperature range		$^\circ\text{C}$

1. Pulse width is limited by safe operating area.
2.  $I_{SD} \leq 4\text{ A}$ ,  $di/dt = 100\text{ A}/\mu\text{s}$ ,  $V_{DS}(\text{peak}) < V_{(BR)DSS}$ ,  $V_{DD} = 450\text{ V}$ .
3.  $V_{DD} \leq 720\text{ V}$

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Thermal resistance, junction-to-case	6.25	$^\circ\text{C}/\text{W}$
$R_{thJA}$	Thermal resistance, junction-to-ambient	62.5	$^\circ\text{C}/\text{W}$

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or non-repetitive (pulse width limited by $T_J$ max.)	1	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	160	mJ

## 2 Electrical characteristics

$T_C = 25\text{ °C}$  unless otherwise specified.

**Table 4. Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	900	-	-	V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 900\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 900\text{ V}$ , $T_C = 125\text{ °C}^{(1)}$	-	-	50	
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$	-	-	$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 1.5\text{ A}$	-	1.90	2.10	$\Omega$

1. Specified by design, not tested in production.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	173	-	pF
$C_{oss}$	Output capacitance		-	17.9	-	pF
$C_{rss}$	Reverse transfer capacitance		-	1	-	pF
$C_{o(tr)}^{(1)}$	Time-related equivalent capacitance	$V_{DS} = 0\text{ to }720\text{ V}$ , $V_{GS} = 0\text{ V}$	-	29	-	pF
$C_{o(er)}^{(2)}$	Energy-related equivalent capacitance		-	11	-	pF
$R_g$	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	15.5	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 720\text{ V}$ , $I_D = 3\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$ (see the Figure 14. Test circuit for gate charge behavior)	-	5.3	-	nC
$Q_{gs}$	Gate-source charge		-	1.45	-	nC
$Q_{gd}$	Gate-drain charge		-	2.8	-	nC

1.  $C_{o(tr)}$  is a constant capacitance value that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 V to the stated value.

2.  $C_{o(er)}$  is a constant capacitance value that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 V to the stated value.

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 450\text{ V}$ , $I_D = 1.5\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$	-	10.5	-	ns
$t_r$	Rise time		-	11.8	-	ns
$t_{d(off)}$	Turn-off delay time	(see the Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	26.4	-	ns
$t_f$	Fall time		-	25.5	-	ns

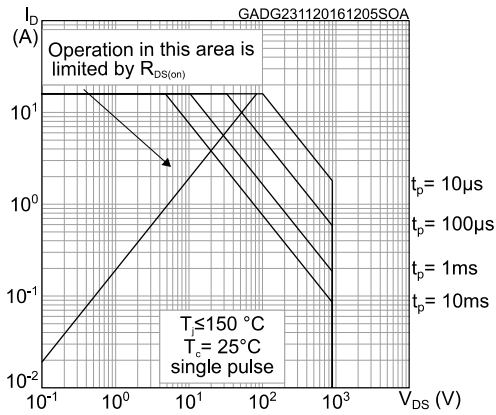
**Table 7. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-	-	4	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-	-	16	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 3\text{ A}$	-	-	1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 3\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,	-	289	-	ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60\text{ V}$	-	1.56	-	$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see the Figure 15. Test circuit for inductive load switching and diode recovery times)	-	10.8	-	A
$t_{rr}$	Reverse recovery time	$I_{SD} = 3\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,	-	494	-	ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$	-	2.45	-	$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see the Figure 15. Test circuit for inductive load switching and diode recovery times)	-	9.9	-	A

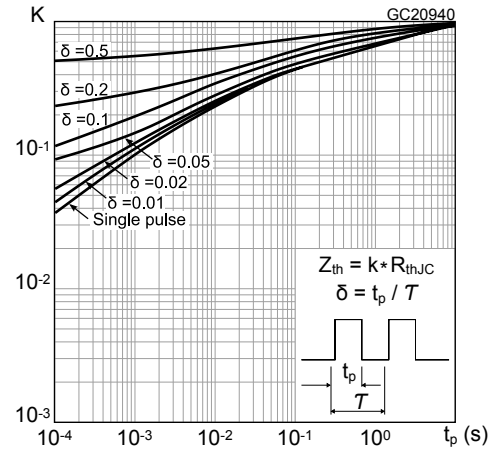
1. Pulse width is limited by safe operating area.
2. Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

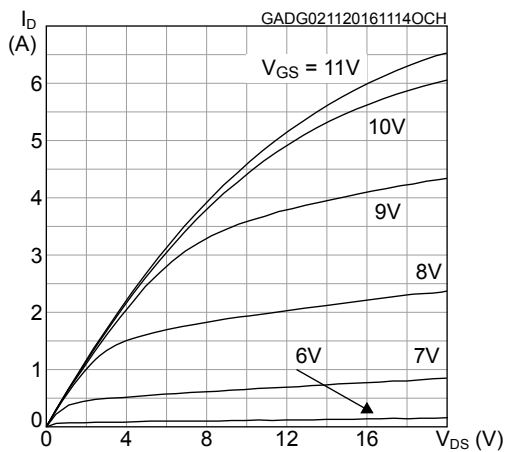
**Figure 1. Safe operating area**



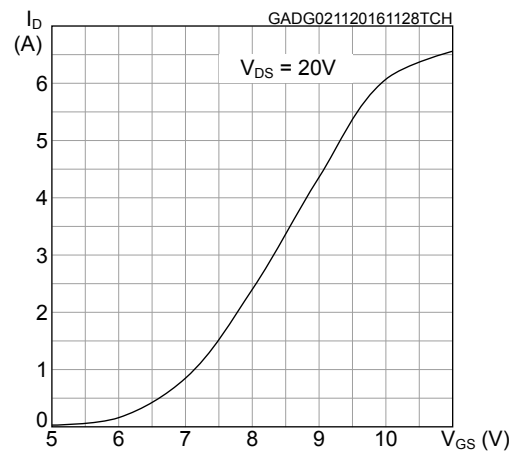
**Figure 2. Normalized transient thermal impedance**



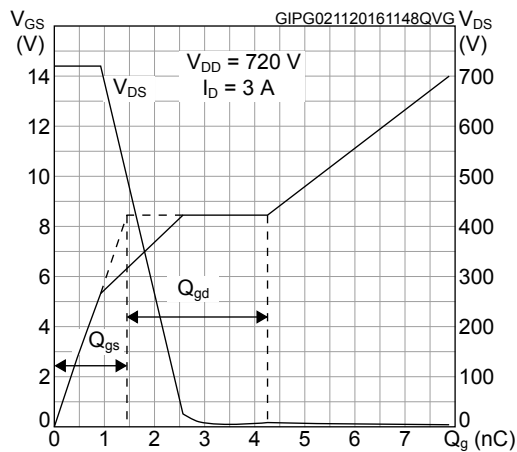
**Figure 3. Typical output characteristics**



**Figure 4. Typical transfer characteristics**



**Figure 5. Typical gate charge characteristics**



**Figure 6. Typical drain-source on-resistance**

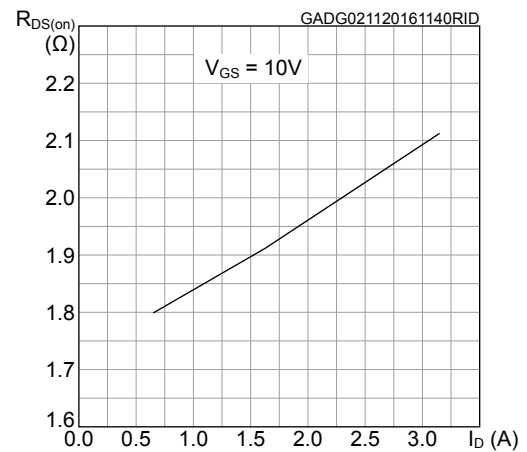


Figure 7. Typical capacitance characteristics

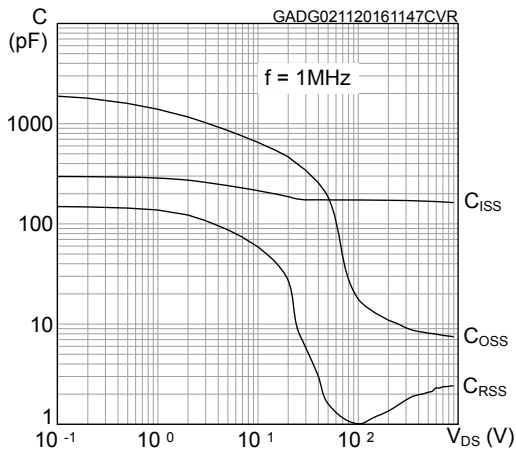


Figure 8. Normalized gate threshold vs temperature

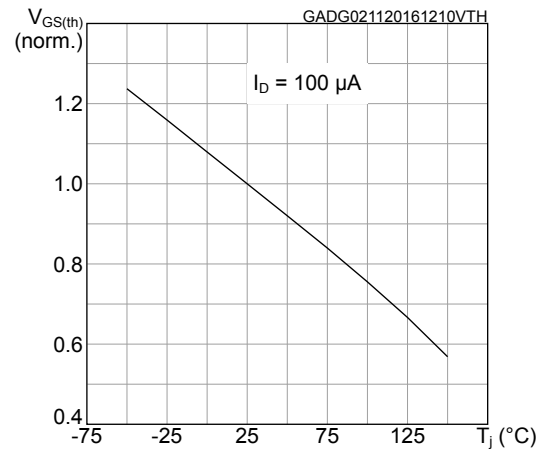


Figure 9. Normalized on-resistance vs temperature

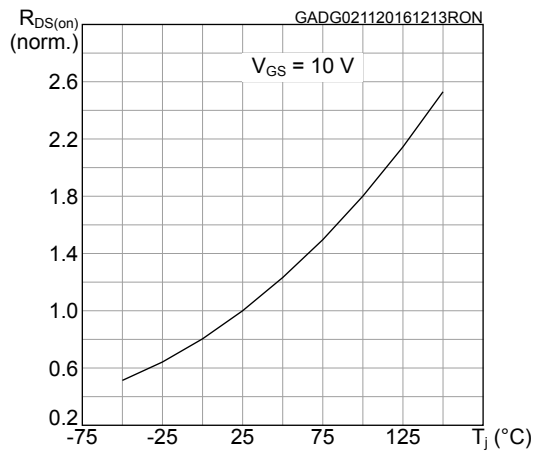


Figure 10. Normalized breakdown voltage vs temperature

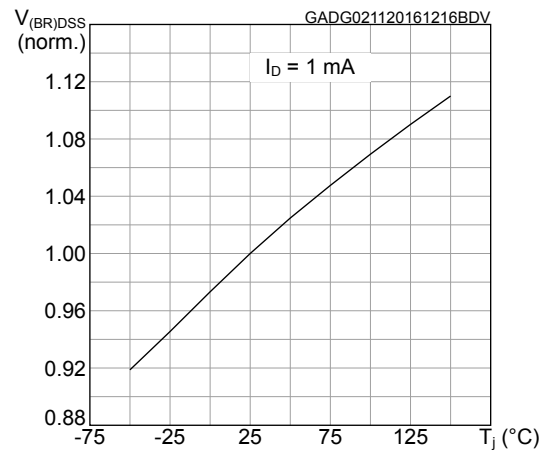


Figure 11. Maximum avalanche energy vs temperature

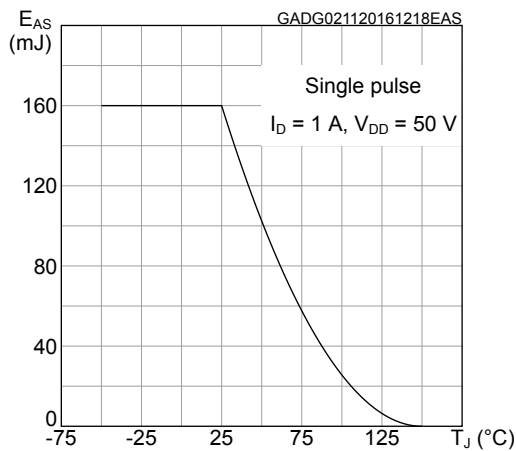
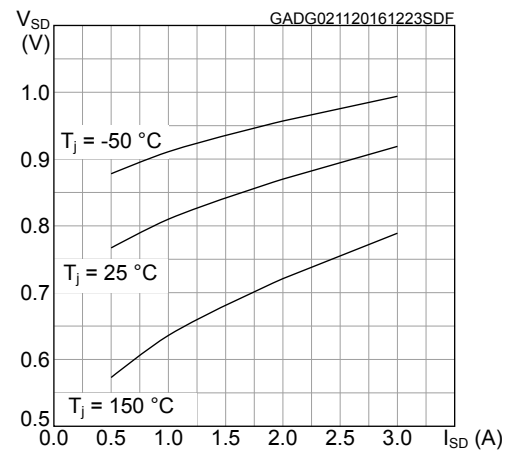
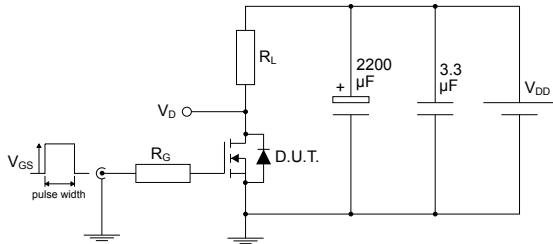


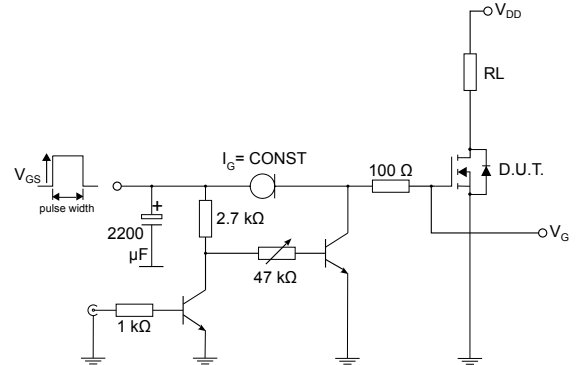
Figure 12. Typical reverse diode forward characteristics



### 3 Test circuits

**Figure 13. Test circuit for resistive load switching times**


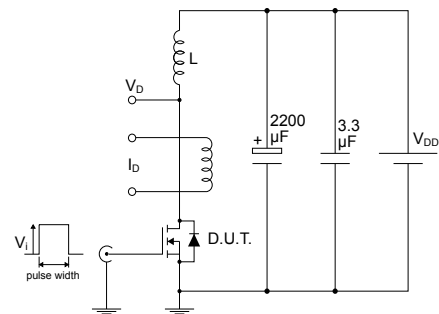
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**Figure 14. Test circuit for gate charge behavior**


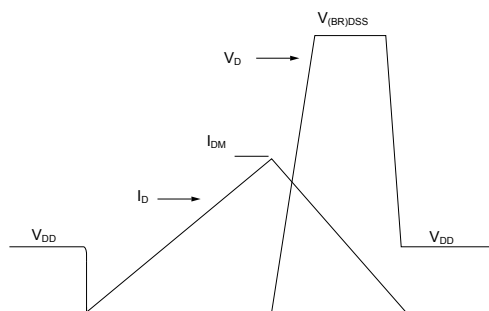
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**Figure 15. Test circuit for inductive load switching and diode recovery times**

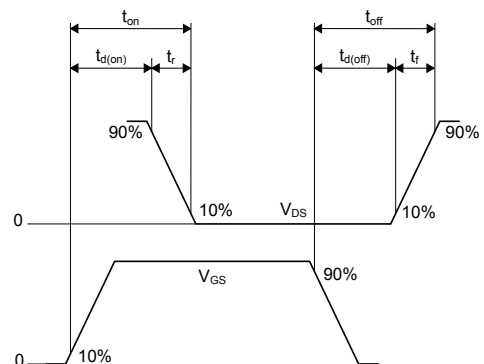

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**Figure 16. Unclamped inductive load test circuit**


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**Figure 17. Unclamped inductive waveform**


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**Figure 18. Switching time waveform**


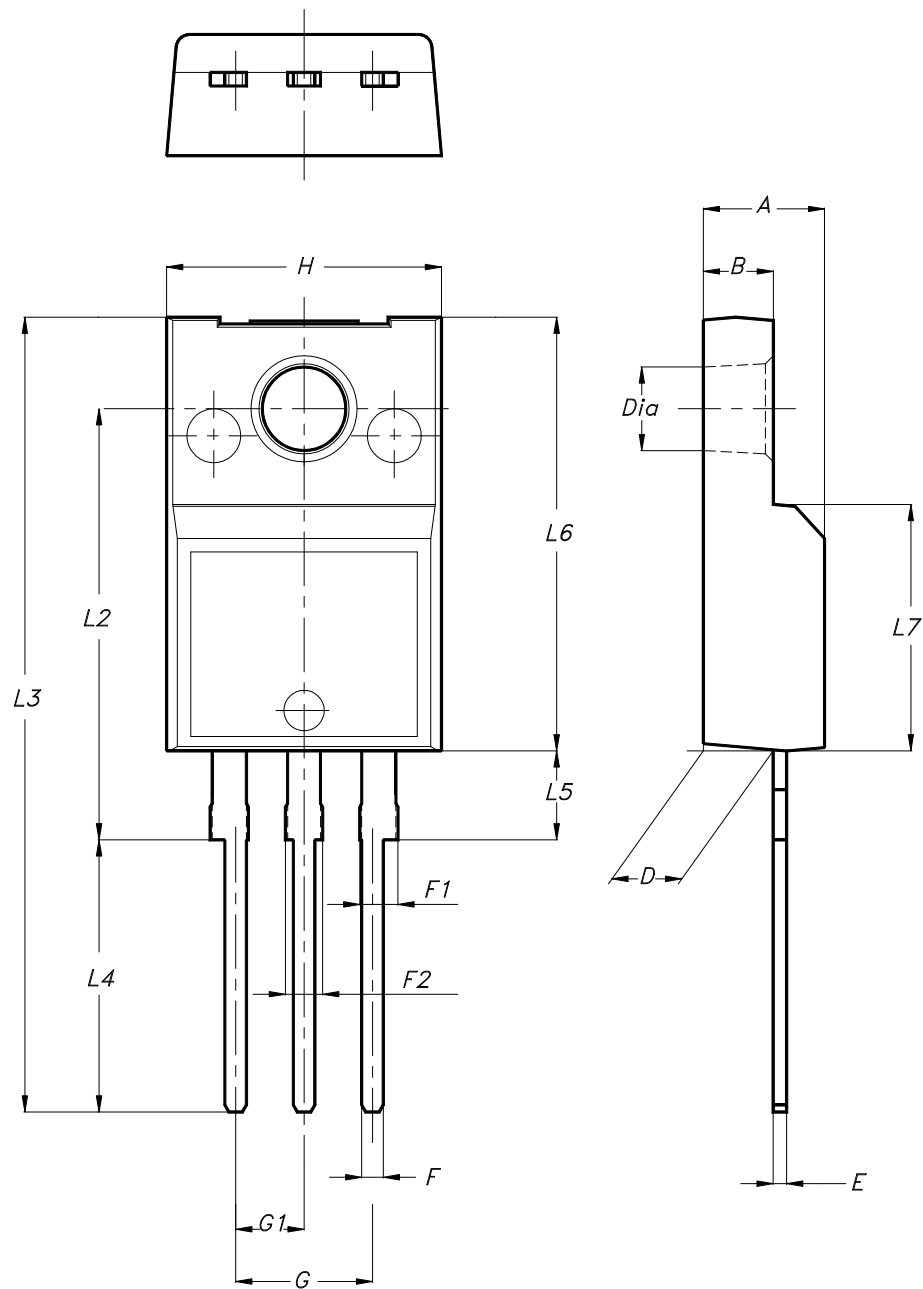
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## 4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 TO-220FP type B package information

Figure 19. TO-220FP type B package outline



7012510\_B\_rev.14

**Table 8. TO-220FP type B package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.20
G1	2.40		2.70
H	10.00		10.40
L2		16.00	
L3	28.60		30.60
L4	9.80		10.60
L5	2.90		3.60
L6	15.90		16.40
L7	9.00		9.30
Dia	3.00		3.20

## Revision history

**Table 9. Document revision history**

Date	Revision	Changes
02-Nov-2016	1	First release.
23-Nov-2016	2	Updated <i>Figure 2: "Safe operating area"</i> . Minor text changes.
27-Mar-2026	3	Updated <a href="#">Section 4.1: TO-220FP type B package information</a> . Minor text changes.

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