

FDC6322C

Dual N & P Channel , Digital FET

General Description

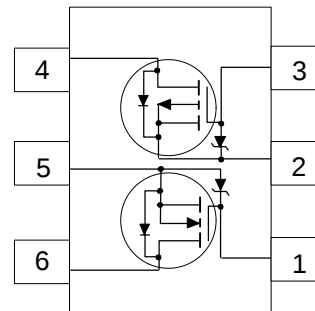
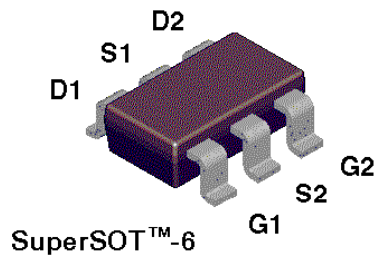
These dual N & P Channel logic level enhancement mode field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. The device is an improved design especially for low voltage applications as a replacement for bipolar digital transistors in load switching applications. Since bias resistors are not required, this dual digital FET can replace several digital transistors with difference bias resistors.

Features

- N-Ch 25 V, 0.22 A, $R_{DS(ON)} = 5 \Omega$ @ $V_{GS} = 2.7$ V.
- P-Ch 25 V, -0.46 A, $R_{DS(ON)} = 1.5 \Omega$ @ $V_{GS} = -2.7$ V.
- Very low level gate drive requirements allowing direct operation in 3 V circuits. $V_{GS(th)} < 1.5$ V.
- Gate-Source Zener for ESD ruggedness. >6kV Human Body Model
- Replace NPN & PNP digital transistors.



Mark: .322



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless other wise noted

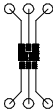
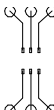
Symbol	Parameter	N-Channel	P-Channel	Units
V _{DSS} , V _{CC}	Drain-Source Voltage, Power Supply Voltage	25	-25	V
V _{GSS} , V _{IN}	Gate-Source Voltage,	8	-8	V
I _D , I _O	Drain/Output Current - Continuous	0.22	-0.46	A
	- Pulsed	0.5	-1	
P _D	Maximum Power Dissipation (Note 1a)	0.9		W
	(Note 1b)	0.7		
T _J , T _{STG}	Operating and Storage Tempature Ranger	-55 to 150		°C
ESD	Electrostatic Discharge Rating MIL-STD-883D Human Body Model (100pf / 1500 Ohm)	6		kV

THERMAL CHARACTERISTICS

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	140	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	60	$^\circ\text{C/W}$

DMOS Electrical Characteristics ($T_A = 25\text{ }^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	N-Ch	25			V
		V _{GS} = 0 V, I _D = -250 μA	P-Ch	-25			
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	I _D = 250 μA, Referenced to 25 °C	N-Ch		25		mV / °C
		I _D = -250 μA, Referenced to 25 °C	P-Ch		-22		
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 20 V, V _{GS} = 0 V, T _J = 55°C	N-Ch			1	μA
						10	
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -20 V, V _{GS} = 0 V, T _J = 55°C	P-Ch			-1	μA
						-10	
I _{GSS}	Gate - Body Leakage Current	V _{GS} = 8 V, V _{DS} = 0 V	N-Ch			100	nA
		V _{GS} = -8 V, V _{DS} = 0 V	P-Ch			-100	nA
ON CHARACTERISTICS (Note 2)							
ΔV _{GS(th)} /ΔT _J	Gate Threshold Voltage Temp. Coefficient	I _D = 250 μA, Referenced to 25 °C	N-Ch		-2.1		mV / °C
		I _D = -250 μA, Referenced to 25 °C	P-Ch		2.1		
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	0.65	0.85	1.5	V
		V _{DS} = V _{GS} , I _D = -250 μA	P-Ch	-0.65	-0.86	-1.5	
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 2.7 V, I _D = 0.2 A, T _J =125°C	N-Ch		3.8	5	Ω
					6.3	9	
					3.1	4	
		V _{GS} = -2.7 V, I _D = -0.25 A, T _J =125°C	P-Ch		1.22	1.5	
					1.65	2.4	
					0.87	1.1	
I _{D(on)}	On-State Drain Current	V _{GS} = 2.7 V, V _{DS} = 5 V	N-Ch	0.2			A
		V _{GS} = -2.7 V, V _{DS} = -5 V	P-Ch	-0.5			
g _{FS}	Forward Transconductance	V _{DS} = 5 V, I _D = 0.4 A	N-Ch		0.2		S
		V _{DS} = -5 V, I _D = -0.5 A	P-Ch		0.8		
DYNAMIC CHARACTERISTICS							
C _{iss}	Input Capacitance	N-Channel V _{DS} = 10 V, V _{GS} = 0 V, f = 1.0 MHz	N-Ch		9.5		pF
C _{oss}	Output Capacitance		P-Ch		62		
			N-Ch		6		
C _{rss}	Reverse Transfer Capacitance		P-Ch		35		
		N-Ch		1.3			
		f = 1.0 MHz	P-Ch		9.5		

SWITCHING CHARACTERISTICS (Note 2)							
Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
$t_{D(on)}$	Turn - On Delay Time	N-Channel $V_{DD} = 6\text{ V}$, $I_D = 0.5\text{ A}$,	N-Ch		5	10	nS
			P-Ch		7	14	
t_r	Turn - On Rise Time	$V_{GS} = 4.5\text{ V}$, $R_{GEN} = 50\ \Omega$	N-Ch		4.5	10	nS
			P-Ch		8	16	
$t_{D(off)}$	Turn - Off Delay Time	P-Channel $V_{DD} = -6\text{ V}$, $I_D = -0.5\text{ A}$,	N-Ch		4	8	nS
			P-Ch		55	90	
t_f	Turn - Off Fall Time	$V_{Gen} = -4.5\text{ V}$, $R_{GEN} = 50\ \Omega$	N-Ch		3.2	7	nS
			P-Ch		35	55	
Q_g	Total Gate Charge	N-Channel $V_{DS} = 5\text{ V}$, $I_D = 0.2\text{ A}$,	N-Ch		0.49	0.7	nC
			P-Ch		1	1.5	
Q_{gs}	Gate-Source Charge	$V_{GS} = 4.5\text{ V}$	N-Ch		0.22		nC
		P- Channel	P-Ch		0.32		
Q_{gd}	Gate-Drain Charge	$V_{DS} = -5\text{ V}$, $I_D = -0.25\text{ A}$,	N-Ch		0.07		nC
		$V_{GS} = -4.5\text{ V}$	P-Ch		0.25		
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
I_S	Maximum Continuous Drain-Source Diode Forward Current		N-Ch			0.5	A
			P-Ch			-0.5	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 0.5\text{ A}$ (Note 2)	N-Ch		0.97	1.3	V
		$V_{GS} = 0\text{ V}$, $I_S = -0.5\text{ A}$ (Note 2)	P-Ch		-0.88	-1.2	
Notes:							
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 in still air.							
 a. 140°C/W on a 0.125 in^2 pad of 2oz copper.  b. 180°C/W on a 0.005 in^2 of pad of 2oz copper.							
Scale 1 : 1 on letter size paper							
2. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2.0\%$.							

Typical Electrical Characteristics: N-Channel

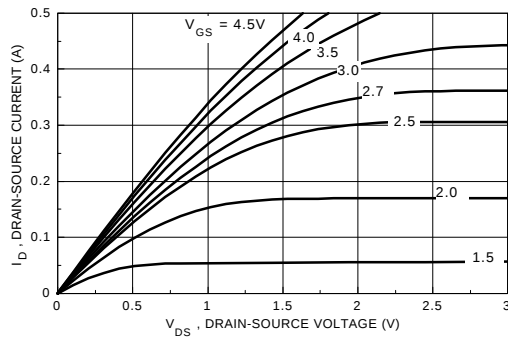


Figure 1. On-Region Characteristics.

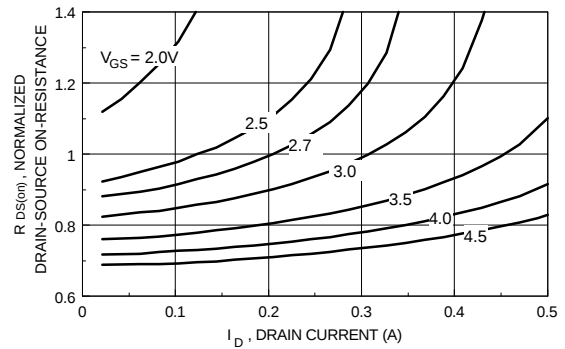


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

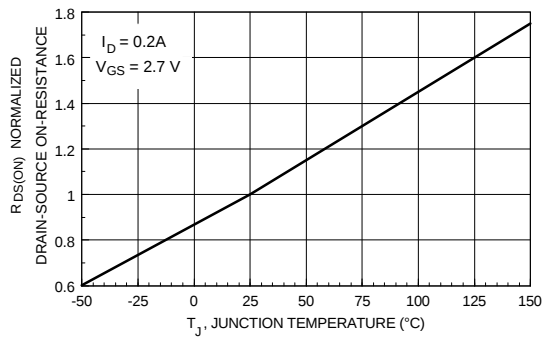


Figure 3. On-Resistance Variation with Temperature.

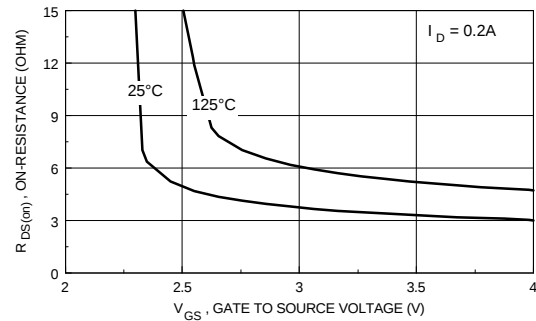


Figure 4. On Resistance Variation with Gate-To- Source Voltage.

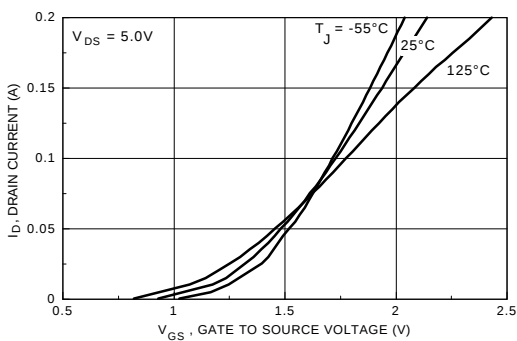


Figure 5. Transfer Characteristics.

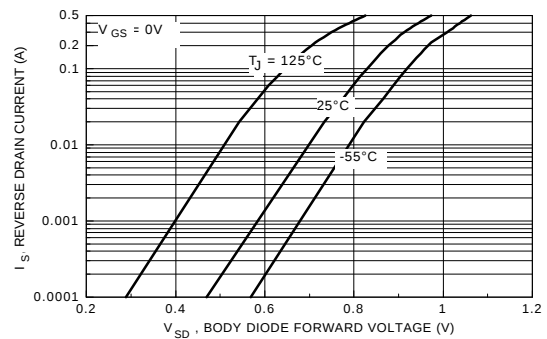


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Electrical Characteristics: N-Channel (continued)

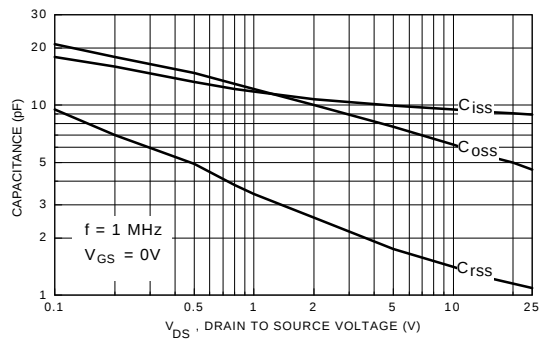


Figure 7. Capacitance Characteristics.

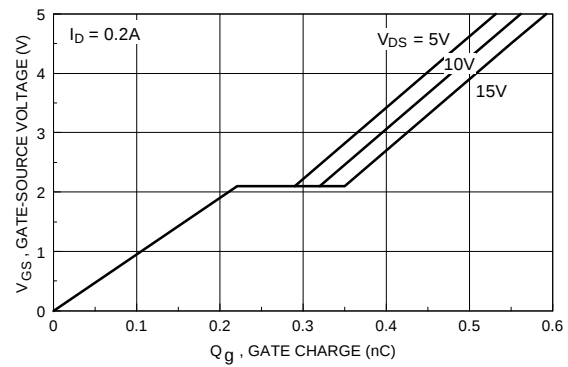


Figure 8. Gate Charge Characteristics.

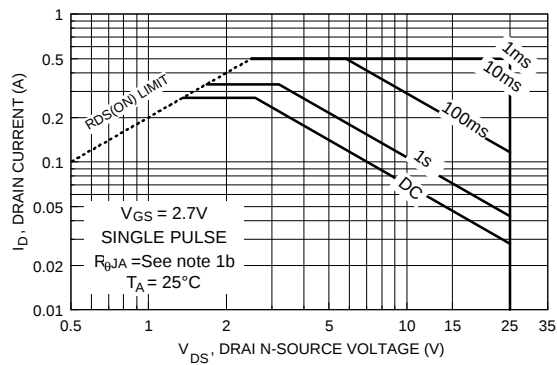


Figure 9. Maximum Safe Operating Area.

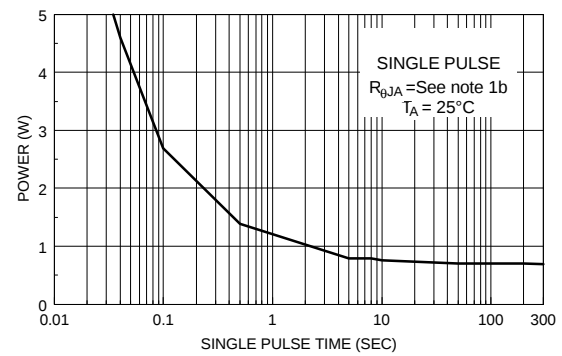


Figure 10. Single Pulse Maximum Power Dissipation.

Typical Electrical Characteristics: P-Channel

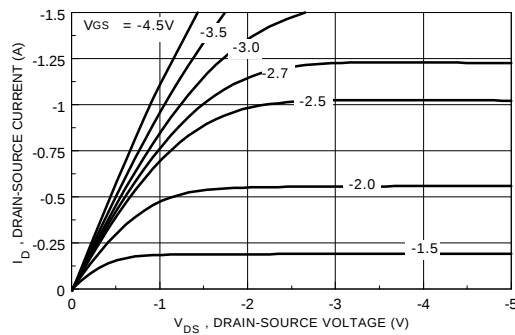


Figure 11. On-Region Characteristics.

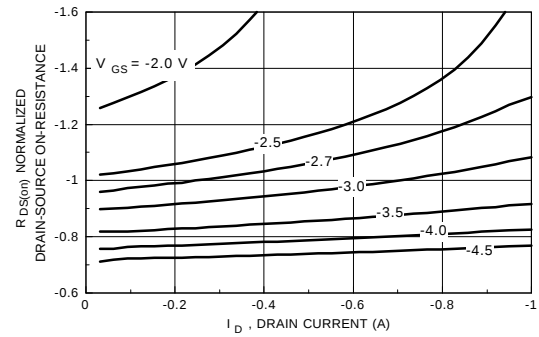


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

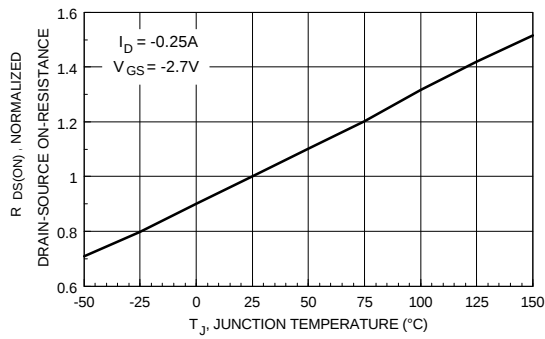


Figure 13. On-Resistance Variation with Temperature.

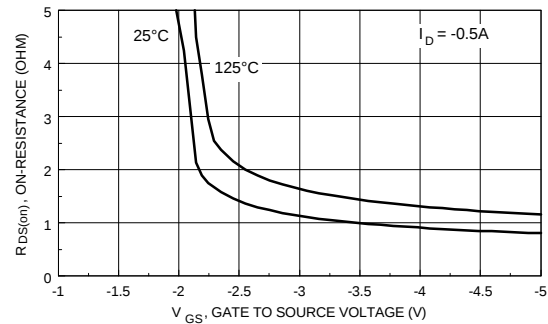


Figure 14. On Resistance Variation with V_{GS} .

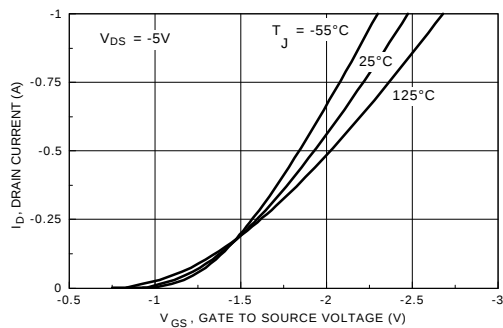


Figure 15. Transfer Characteristics.

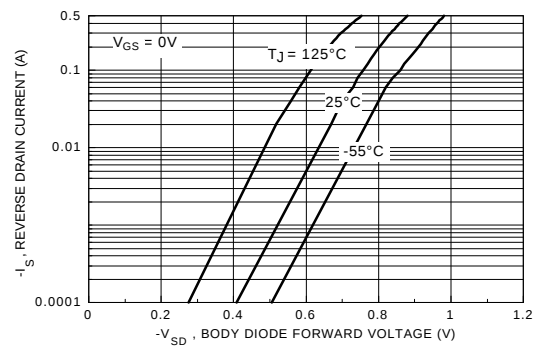


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Electrical Characteristics: P-Channel (continued)

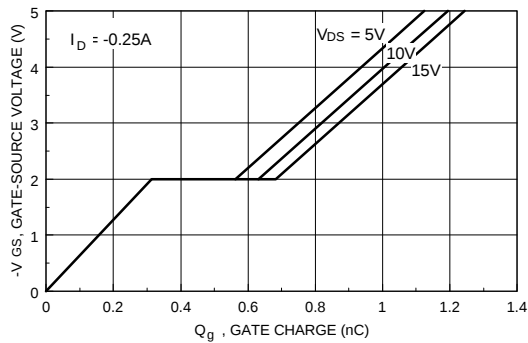


Figure 17. Gate Charge Characteristics.

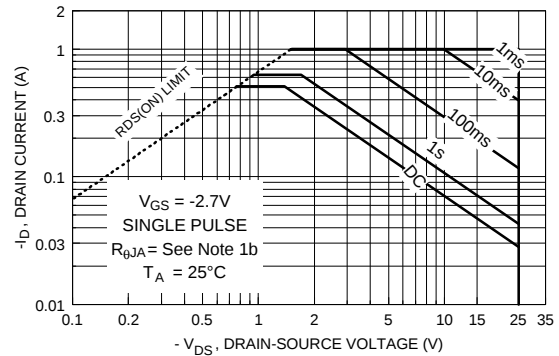


Figure 18. Maximum Safe Operating Area.

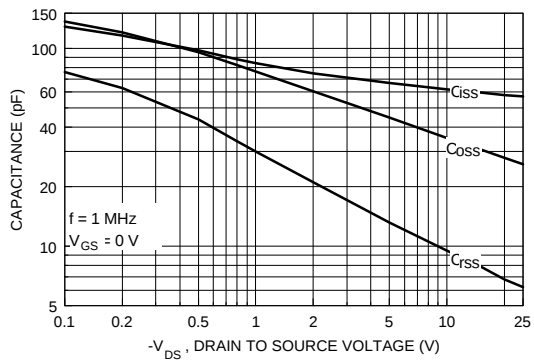


Figure 19. Capacitance Characteristics.

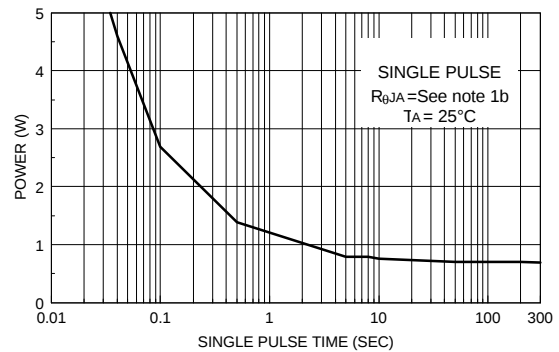


Figure 20. Single Pulse Maximum Power Dissipation.

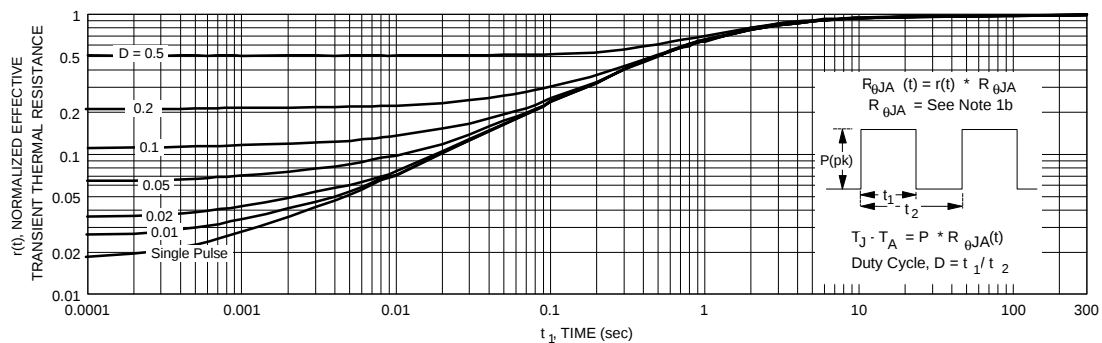


Figure 21. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1b. Transient thermal response will change depending on the circuit board design.

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACE ^{Ex} TM	FAST [®]	OPTOLOGIC TM	SMART START TM	VCX TM
Bottomless TM	FAST ^r TM	OPTOPLANAR TM	STAR*POWER TM	
CoolFET TM	FRFET TM	PACMAN TM	Stealth TM	
CROSSVOLT TM	GlobalOptoisolator TM	POP TM	SuperSOT TM -3	
DenseTrench TM	GTO TM	Power247 TM	SuperSOT TM -6	
DOME TM	HiSeC TM	PowerTrench [®]	SuperSOT TM -8	
EcoSPARK TM	ISOPLANAR TM	QFET TM	SyncFET TM	
E ² CMOS TM	LittleFET TM	QS TM	TinyLogic TM	
EnSigna TM	MicroFET TM	QT Optoelectronics TM	TruTranslation TM	
FACT TM	MicroPak TM	Quiet Series TM	UHC TM	
FACT Quiet Series TM	MICROWIRE TM	SILENT SWITCHER [®]	UltraFET [®]	

STAR*POWER is used under license

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.