



FDMA905P

Single P-Channel PowerTrench® MOSFET

-12 V, -10 A, 16 mΩ

Features

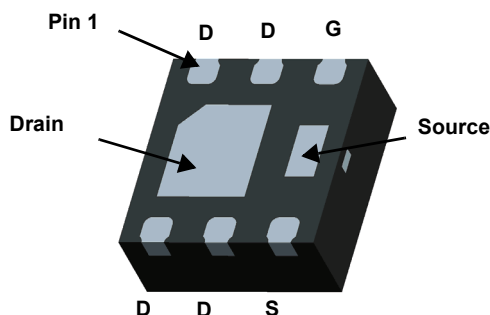
- Max $r_{DS(on)}$ = 16 mΩ at $V_{GS} = -4.5$ V, $I_D = -10$ A
- Max $r_{DS(on)}$ = 21 mΩ at $V_{GS} = -2.5$ V, $I_D = -8.9$ A
- Max $r_{DS(on)}$ = 82 mΩ at $V_{GS} = -1.8$ V, $I_D = -4.5$ A
- Low profile - 0.8 mm maximum - in the new package MicroFET 2X2 mm
- Free from halogenated compounds and antimony oxides
- RoHS Compliant



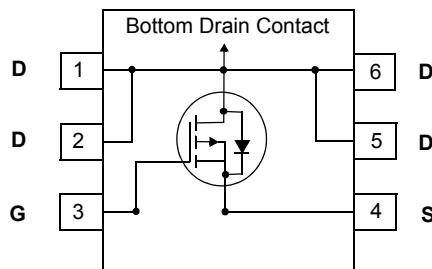
General Description

This device is designed specifically for battery charge or load switching in cellular handset and other ultraportable applications. It features a MOSFET with low on-state resistance.

The MicroFET 2X2 package offers exceptional thermal performance for its physical size and is well suited to linear mode applications.



MicroFET 2X2 (Bottom View)



MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	-12	V
V_{GS}	Gate to Source Voltage	± 8	V
I_D	Drain Current -Continuous (Note 1a)	-10	A
	-Pulsed	-40	
P_D	Power Dissipation (Note 1a)	2.4	W
	Power Dissipation (Note 1b)	0.9	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	6.9	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	52	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	145	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
A95	FDMA905P	MicroFET 2X2	7 "	8 mm	3000 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = -250\ \mu\text{A}$, $V_{GS} = 0\text{ V}$	-12			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$, referenced to 25°C		-4.3		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -9.6\text{ V}$, $V_{GS} = 0\text{ V}$			-1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 8\text{ V}$, $V_{DS} = 0\text{ V}$			± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = -250\ \mu\text{A}$	-0.4	-0.7	-1.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$, referenced to 25°C		2.6		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -4.5\text{ V}$, $I_D = -10\text{ A}$		14	16	m Ω
		$V_{GS} = -2.5\text{ V}$, $I_D = -8.9\text{ A}$		17	21	
		$V_{GS} = -1.8\text{ V}$, $I_D = -4.5\text{ A}$		21	82	
		$V_{GS} = -4.5\text{ V}$, $I_D = -10\text{ A}$, $T_J = 125^\circ\text{C}$		16	21	
g_{FS}	Forward Transconductance	$V_{DD} = -5\text{ V}$, $I_D = -10\text{ A}$		50		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = -6\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$		2559	3405	pF
C_{oss}	Output Capacitance			490	735	pF
C_{rss}	Reverse Transfer Capacitance			437	655	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -6\text{ V}$, $I_D = -10\text{ A}$, $V_{GS} = -4.5\text{ V}$, $R_{GEN} = 6\ \Omega$		11	20	ns
t_r	Rise Time			11	20	ns
$t_{d(off)}$	Turn-Off Delay Time			120	192	ns
t_f	Fall Time			59	94	ns
Q_g	Total Gate Charge	$V_{DD} = -6\text{ V}$, $I_D = -10\text{ A}$, $V_{GS} = -4.5\text{ V}$		21	29	nC
Q_{gs}	Gate to Source Charge			3.5		nC
Q_{gd}	Gate to Drain "Miller" Charge			4.2		nC

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = -2\text{ A}$ (Note 2)		-0.6	-1.2	V
		$V_{GS} = 0\text{ V}$, $I_S = -10\text{ A}$ (Note 2)		-0.8	-1.2	
t_{rr}	Reverse Recovery Time	$I_F = -10\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		21	34	ns
Q_{rr}	Reverse Recovery Charge			6.1	12	nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 52 $^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper.



b. 145 $^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0 %.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

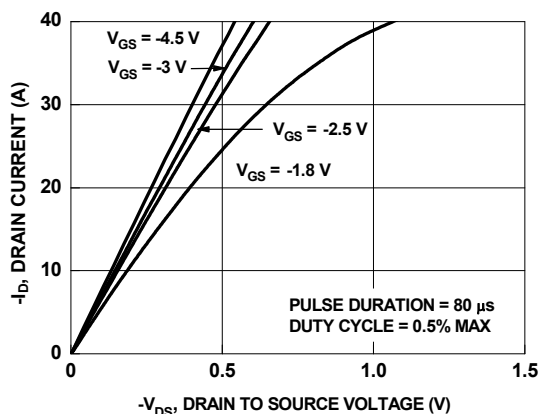


Figure 1. On-Region Characteristics

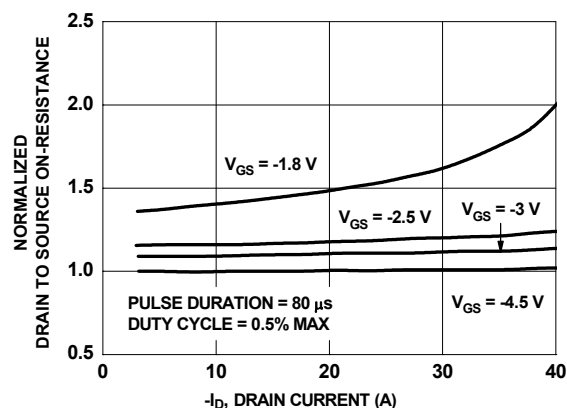


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

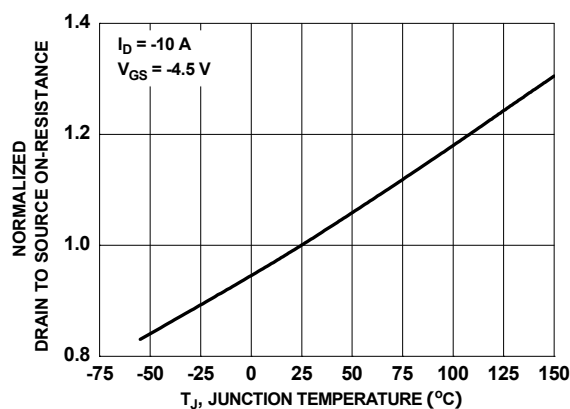


Figure 3. Normalized On-Resistance vs Junction Temperature

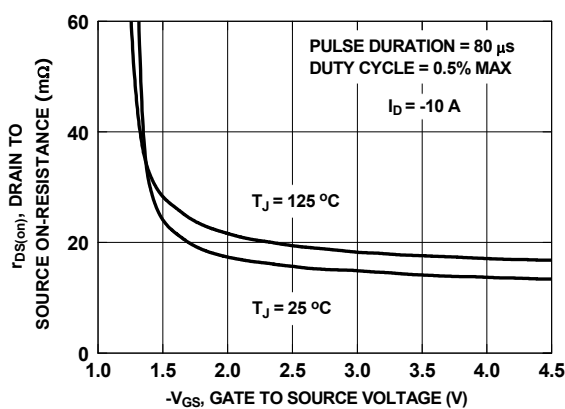


Figure 4. On-Resistance vs Gate to Source Voltage

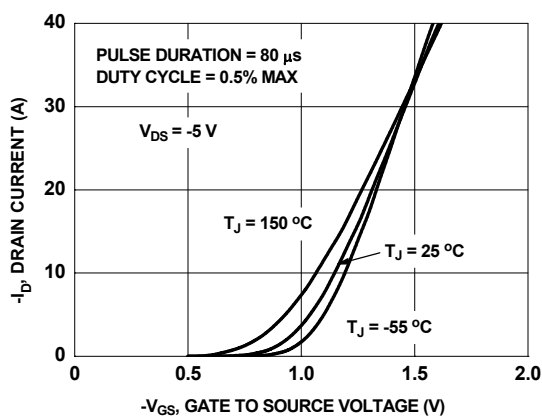


Figure 5. Transfer Characteristics

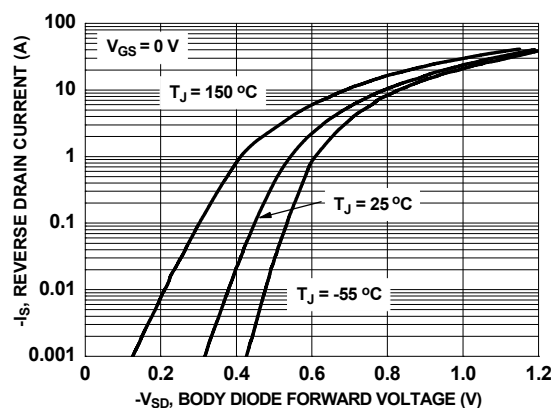


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

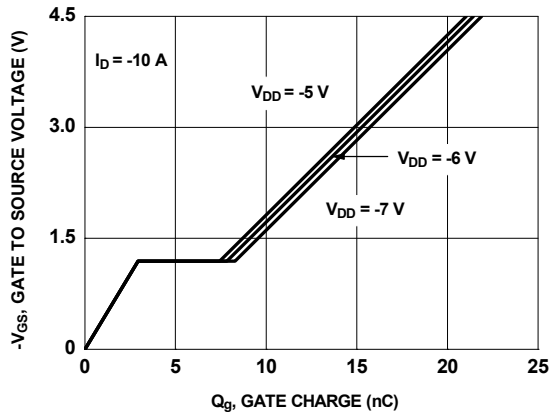


Figure 7. Gate Charge Characteristics

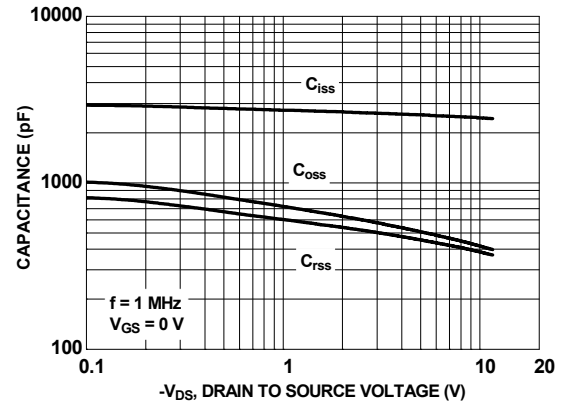


Figure 8. Capacitance vs Drain to Source Voltage

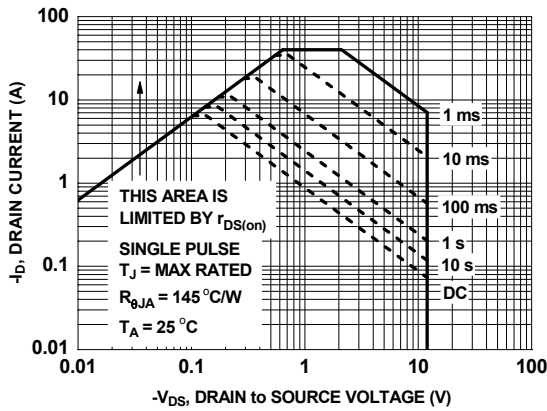


Figure 9. Forward Bias Safe Operating Area

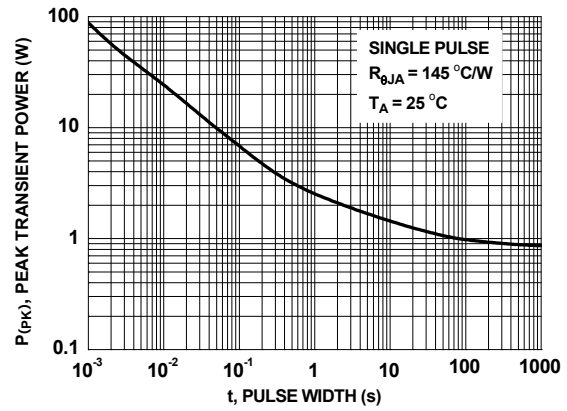


Figure 10. Single Pulse Maximum Power Dissipation

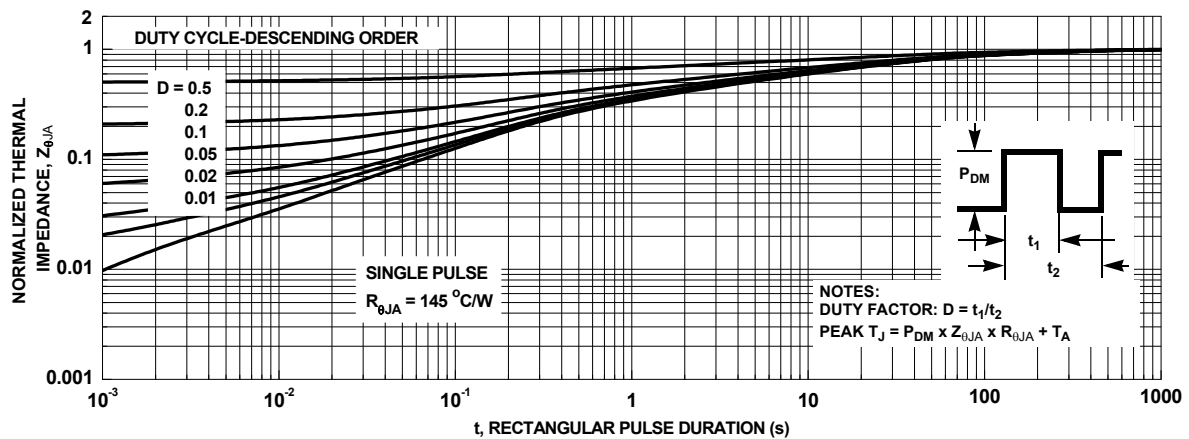
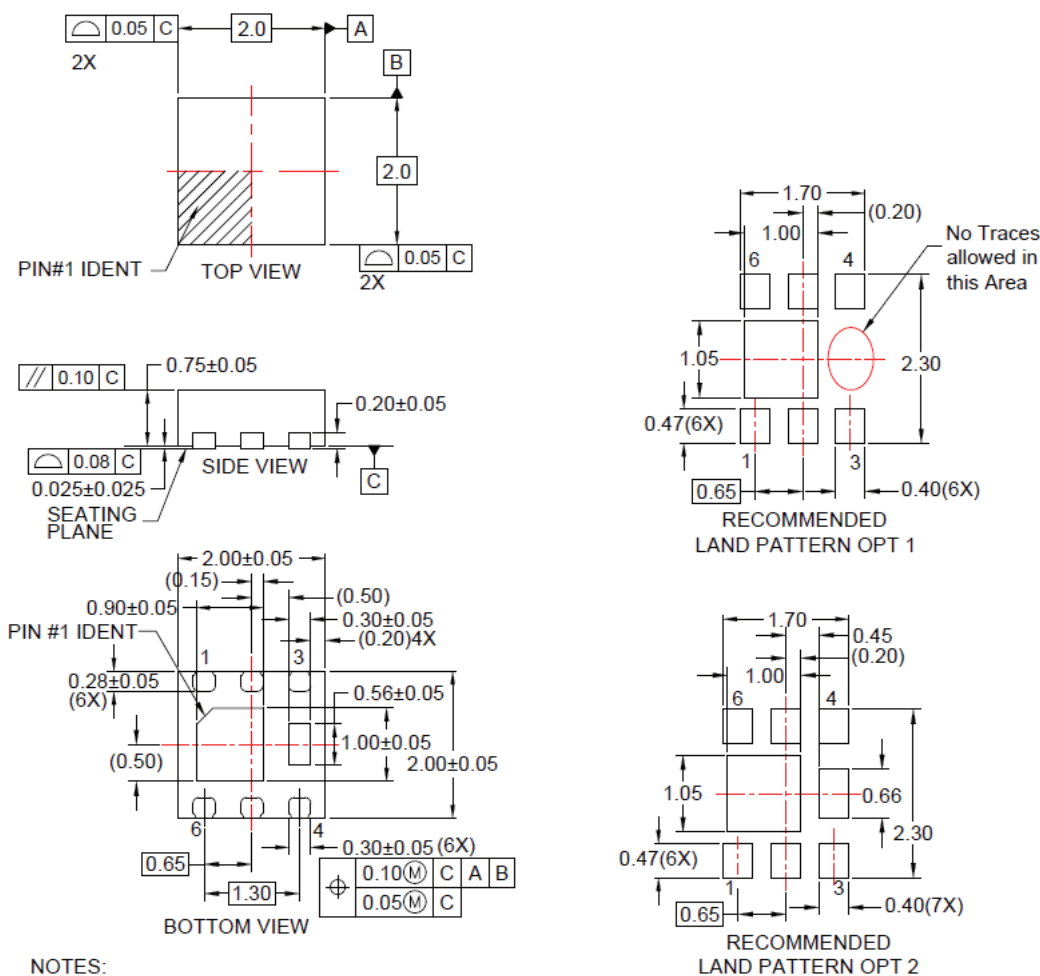


Figure 11. Junction-to-Ambient Transient Thermal Response Curve

Dimensional Outline and Pad Layout



NOTES:

- PACKAGE DOES NOT FULLY CONFORM TO JEDEC MO-229 REGISTRATION
- DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
- DRAWING FILENAME: MKT-MLP06Rev4.



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