



CY7C171A CY7C172A

4K x 4 Static RAM with Separate I/O

Features

- Automatic power-down when deselected
- CMOS for optimum speed/power
- High speed
— $t_{AA} = 15 \text{ ns}$
- Transparent write (CY7C171A)
- Low active power
— 375 mW
- Low standby power
— 93 mW
- TTL-compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge

Functional Description

The CY7C171A and CY7C172A are high-performance CMOS static RAMs organized as 4096 by 4 bits with separate I/O. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by 77% when deselected.

Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four input/output pins (I_0 through I_3) is

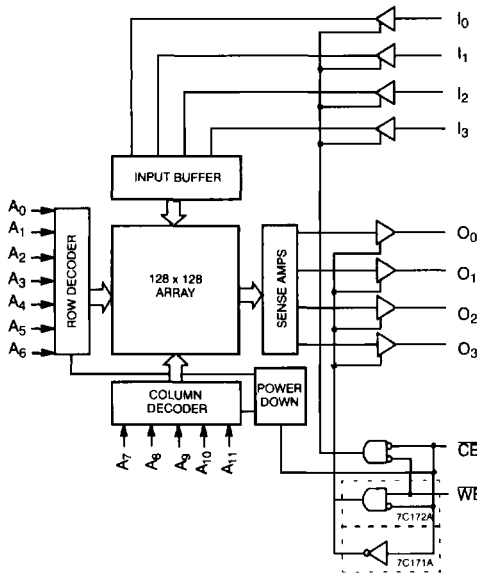
written into the memory location specified on the address pins (A_0 through A_{11}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data output pins.

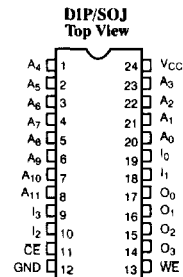
The output pins remain in a high-impedance state when write enable ($\overline{WE}$) is LOW (7C172A only), or chip enable is HIGH.

A die coat is used to insure alpha immunity.

Logic Block Diagram



Pin Configurations



Selection Guide

	7C171A-15 7C172A-15	7C171A-20 7C172A-20	7C171A-25 7C172A-25	7C171A-35 7C172A-35	7C171A-45 7C172A-45
Maximum Access Time (ns)	15	20	25	35	45
Maximum Operating Current (mA)	Commercial 115	80	70	70	70
	Military	90	80	70	70



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State	-0.5V to +7.0V
DC Input Voltage	-3.0V to +7.0V
Output Current into Outputs (LOW)	20 mA

Static Discharge Voltage	>2001V (per MIL-STD-883, Method 3015)
Latch-Up Current	>200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Military ^[1]	-55°C to +125°C	5V ± 10%

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Electrical Characteristics Over the Operating Range^[2]

Parameter	Description	Test Conditions	7C171A-15 7C172A-15		7C171A-20 7C172A-20		7C171A-25 7C172A-25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage		-3.0	0.8	-3.0	0.8	-3.0	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-10	+10	-10	+10	-10	+10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-10	+10	-10	+10	-10	+10	μA
I _{OS}	Output Short Circuit Current ^[3]	V _{CC} = Max., V _{OUT} = GND		-350		-350		-350	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA	Com'l	115		80		70	mA
			Mil			90		80	mA
I _{SB1}	Automatic $\overline{\text{CE}}$ Power-Down Current	Max. V _{CC} , $\overline{\text{CE}} \geq V_{IH}$, Min. Duty Cycle = 100%	Com'l	40		40		20	mA
			Mil			40		20	mA
I _{SB2}	Automatic $\overline{\text{CE}}$ Power-Down Current	Max. V _{CC} , $\overline{\text{CE}} \geq V_{IH} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V	Com'l	20		20		20	mA
			Mil			20		20	mA

Note:

1. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range^[2] (continued)

Parameter	Description	Test Conditions	7C171A-35 7C172A-35		7C171A-45 7C172A-45		Unit
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage		-3.0	0.8	-3.0	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-10	+10	-10	+10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-10	+10	-10	+10	μA
I _{OS}	Output Short Circuit Current ^[3]	V _{CC} = Max., V _{OUT} = GND		-350		-350	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA	Com'l	70			mA
			Mil	70		70	mA
I _{SB1}	Automatic $\overline{CE}$ Power-Down Current	Max. V _{CC} , $\overline{CE} \geq V_{IH}$, Min. Duty Cycle = 100%	Com'l	20			mA
			Mil	20		20	mA
I _{SB2}	Automatic $\overline{CE}$ Power-Down Current	Max. V _{CC} , $\overline{CE} \geq V_{IH} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V	Com'l	20			mA
			Mil	20		20	mA

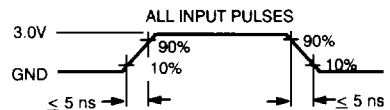
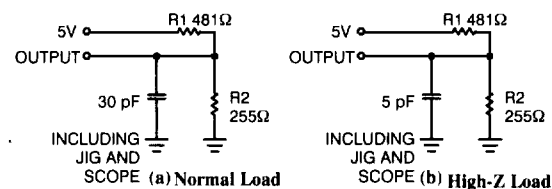
Capacitance^[4]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		10	pF

Notes:

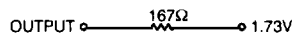
- See the last page of this specification for Group A subgroup testing information.
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters

AC Test Loads and Waveforms



C171A-4

Equivalent to: THÉVENIN EQUIVALENT



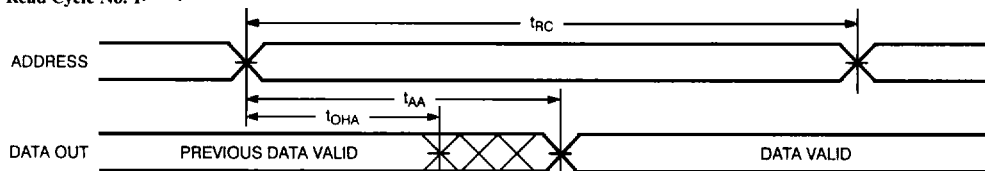
C171A-3

Switching Characteristics Over the Operating Range^[2,5]

Parameter	Description	7C171A–15 7C172A–15		7C171A–20 7C172A–20		7C171A–25 7C172A–25		7C171A–35 7C172A–35		7C171A–45 7C172A–45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t _{RC}	Read Cycle Time	15		20		25		35		45		ns
t _{AA}	Address to Data Valid		15		20		25		35		45	ns
t _{OHA}	Output Hold from Address Change	5		5		5		5		5		ns
t _{ACE}	CE LOW to Data Valid		15		20		25		35		45	ns
t _{LZCE}	CE LOW to LOW Z ^[6]	5		5		5		5		5		ns
t _{HZCE}	CE HIGH to HIGH Z ^[6, 7]		8		8		10		15		15	ns
t _{PU}	CE LOW to Power Up	0		0		0		0		0		ns
t _{PD}	CE HIGH to Power Down		15		20		20		20		25	ns
t _{RCS}	Read Command Set-Up	0		0		0		0		0		ns
t _{RCH}	Read Command Hold	0		0		0		0		0		ns
WRITE CYCLE ^[8]												
t _{WC}	Write Cycle Time	15		20		20		25		40		ns
t _{SCE}	CE LOW to Write End	12		15		20		25		30		ns
t _{AW}	Address Set-Up to Write End	12		15		20		25		30		ns
t _{HA}	Address Hold from Write End	0		0		0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t _{PWE}	WE Pulse Width	12		15		15		20		20		ns
t _{SD}	Data Set-Up to Write End	10		10		10		15		15		ns
t _{HD}	Data Hold from Write End	0		0		0		0		0		ns
t _{LZWE}	WE HIGH to Low Z ^[6] (7C172A)	5		5		5		5		5		ns
t _{HZWE}	WE LOW to High Z ^[6, 7] (7C172A)		7		7		7		10		15	ns
t _{AWE}	WE LOW to Data Valid (7C171A)		15		20		25		30		35	ns
t _{ADV}	Data Valid to Output Valid (7C171A)		15		20		25		30		35	ns

Notes:

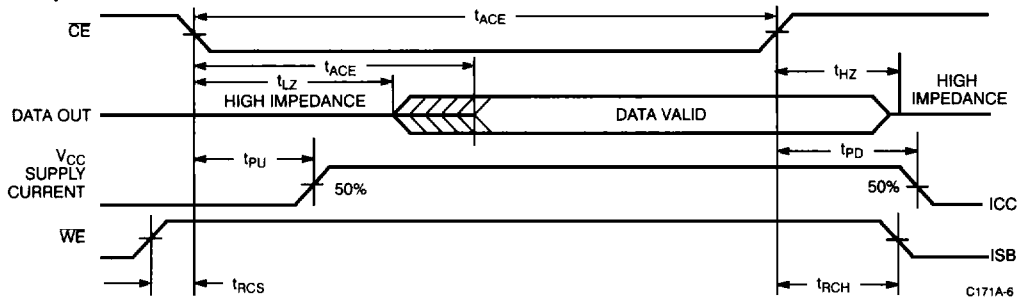
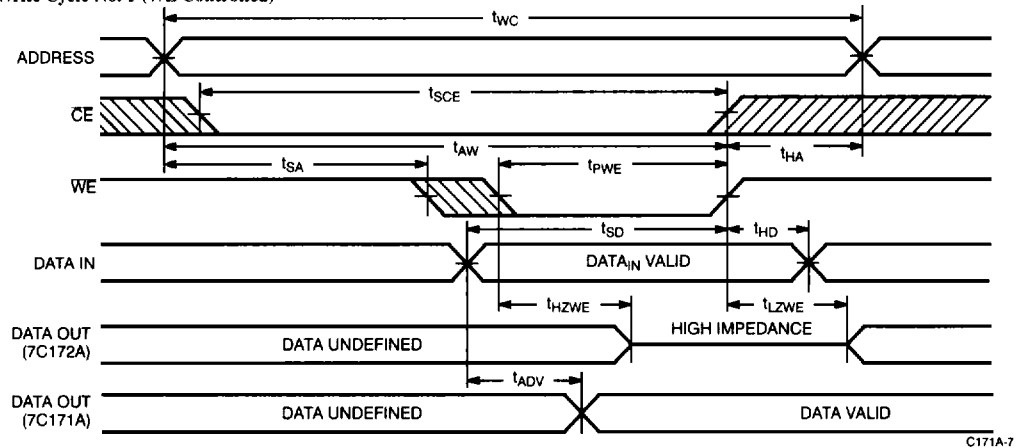
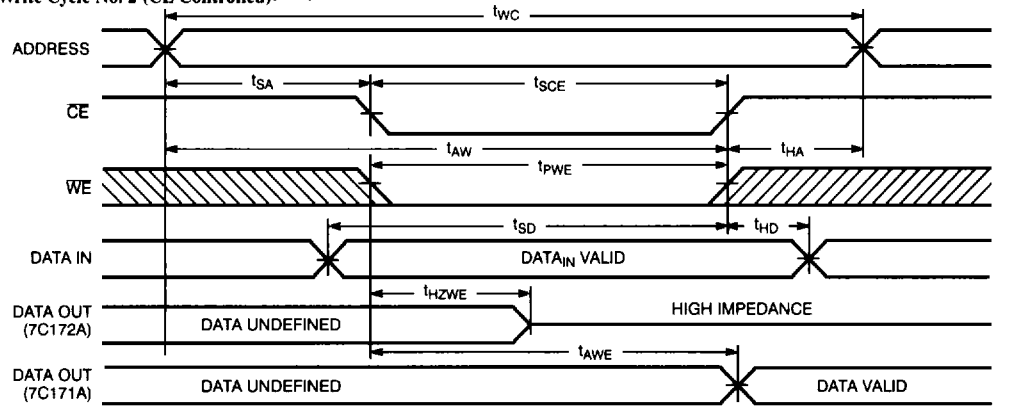
- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for any given device.
- t_{HZCE} and t_{HZWE} are tested with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady state voltage.
- The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- $\overline{WE}$ is HIGH for read cycle.
- Device is continuously selected, $\overline{CE} = V_{IL}$.
- Address valid prior to or coincident with $\overline{CE}$ transition LOW.
- If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state (7C172A).

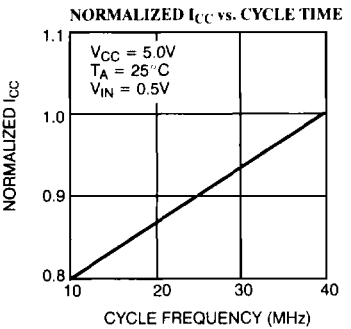
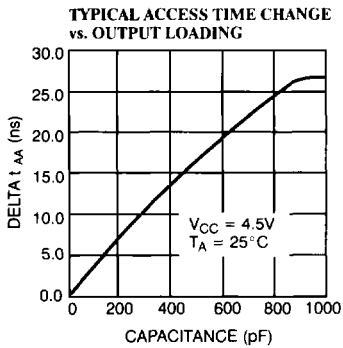
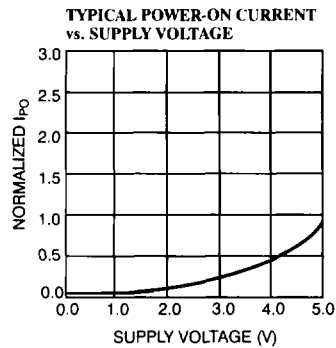
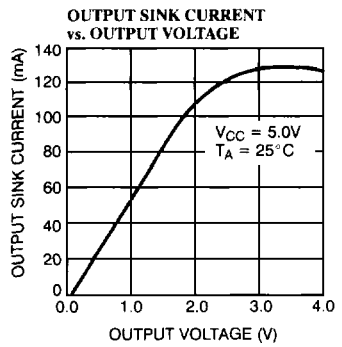
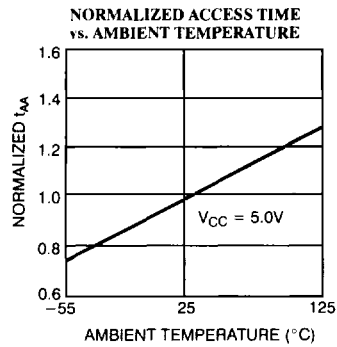
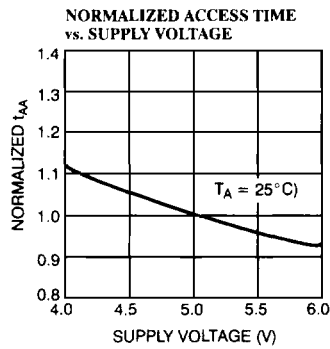
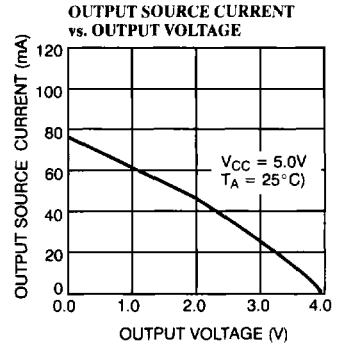
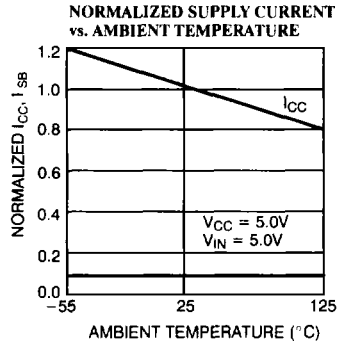
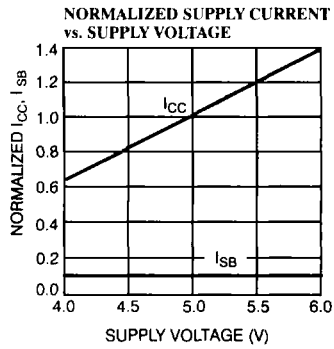
Switching Waveforms
Read Cycle No. 1^[9, 10]


C171A-5



Switching Waveforms (continued)

Read Cycle No. 2^[9, 11]Write Cycle No. 1 ($\overline{WE}$ Controlled)^[8]Write Cycle No. 2 ($\overline{CE}$ Controlled)^[8, 12]

Typical DC and AC Characteristics




Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C171A-15PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
20	CY7C171A-20PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
25	CY7C171A-25PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
35	CY7C171A-35PC	P13	24-Lead (300-Mil) Molded DIP	Commercial

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C172A-15PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C172A-15VC	V13	24-Lead Molded SOJ	
20	CY7C172A-20PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C172A-20VC	V13	24-Lead Molded SOJ	
	CY7C172A-20DMB	D14	24-Lead (300-Mil) CerDIP	Military
25	CY7C172A-25PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C172A-25VC	V13	24-Lead Molded SOJ	
	CY7C172A-25DMB	D14	24-Lead (300-Mil) CerDIP	Military
35	CY7C172A-35PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C172A-35DMB	D14	24-Lead (300-Mil) CerDIP	Military
45	CY7C172A-45DMB	D14	24-Lead (300-Mil) CerDIP	Military



MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL} Max.	1, 2, 3
I _{IX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{OS}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB1}	1, 2, 3
I _{SB1}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t _{RC}	7, 8, 9, 10, 11
t _{AA}	7, 8, 9, 10, 11
t _{OHA}	7, 8, 9, 10, 11
t _{ACE}	7, 8, 9, 10, 11
t _{RCS}	7, 8, 9, 10, 11
t _{RCH}	7, 8, 9, 10, 11
WRITE CYCLE	
t _{WC}	7, 8, 9, 10, 11
t _{SCE}	7, 8, 9, 10, 11
t _{AW}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{SA}	7, 8, 9, 10, 11
t _{PWE}	7, 8, 9, 10, 11
t _{SD}	7, 8, 9, 10, 11
t _{HD}	7, 8, 9, 10, 11
t _{AWE} ^[13]	7, 8, 9, 10, 11
t _{ADV} ^[13]	7, 8, 9, 10, 11

Note:

13. 7C171A only.

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