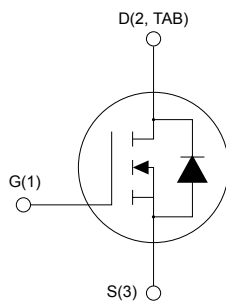
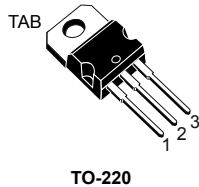


## N-channel 650 V, 308 mΩ typ., 11 A MDmesh M5 Power MOSFET in a TO-220 package



AM01475v1\_TAB



### Features

Order code	$V_{DS}$	$R_{DS(on)}$ max.	$I_D$
STP15N65M5	650 V	340 mΩ	11 A

- Higher  $V_{DSS}$  rating
- Higher  $dv/dt$  capability
- Excellent switching performance
- Extremely low  $R_{DS(on)}$
- 100% avalanche tested

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET based on the MDmesh M5 innovative vertical process technology combined with the well-known PowerMESH horizontal layout. The resulting product offers extremely low on-resistance, making it particularly suitable for applications requiring high power and superior efficiency.

#### Product status link

[STP15N65M5](#)

#### Product summary

Order code	STP15N65M5
Marking	15N65M5
Package	TO-220
Packing	Tube

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	650	V
$V_{GS}$	Gate-source voltage	±25	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ °C}$	11	A
	Drain current (continuous) at $T_C = 100\text{ °C}$	6.9	
$I_{DM}^{(1)}$	Drain current (pulsed)	44	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ °C}$	85	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$T_{stg}$	Storage temperature range	-55 to 150	°C
$T_J$	Operating junction temperature range		

1. Pulse width is limited by safe operating area.
2.  $I_{SD} \leq 11\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ;  $V_{DS}(\text{peak}) < V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$ .

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Thermal resistance, junction-to-case	1.47	°C/W
$R_{thJA}$	Thermal resistance, junction-to-ambient	62.5	

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_J$ max.)	2.5	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ °C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	160	mJ

## 2 Electrical characteristics

$T_C = 25\text{ °C}$  unless otherwise specified.

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	650	-	-	V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 650\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 650\text{ V}$ , $T_C = 125\text{ °C}^{(1)}$	-	-	100	
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 25\text{ V}$	-	-	$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 5.5\text{ A}$	-	308	340	m $\Omega$

1. Specified by design, not tested in production.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	816	-	pF
$C_{oss}$	Output capacitance		-	23	-	pF
$C_{rss}$	Reverse transfer capacitance		-	2.6	-	pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{DS} = 0\text{ to }520\text{ V}$ , $V_{GS} = 0\text{ V}$	-	70	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related		-	21	-	pF
$R_g$	Intrinsic gate resistance	$f = 1\text{ MHz}$ , $I_D = 0\text{ A}$	-	5	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 520\text{ V}$ , $I_D = 5.5\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$ (see the Figure 15. Test circuit for gate charge behavior)	-	22	-	nC
$Q_{gs}$	Gate-source charge		-	5.5	-	nC
$Q_{gd}$	Gate-drain charge		-	11	-	nC

- $C_{o(tr)}$  is an equivalent capacitance that provides the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 V to the stated value.
- $C_{o(er)}$  is an equivalent capacitance that provides the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 V to the stated value.

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(v)}$	Voltage delay time	$V_{DD} = 400\text{ V}$ , $I_D = 7\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see the Figure 16. Test circuit for inductive load switching and diode recovery times and Figure 19. Switching time waveform)	-	30	-	ns
$t_{r(v)}$	Voltage rise time		-	8	-	ns
$t_{f(i)}$	Current fall time		-	11	-	ns
$t_{c(off)}$	Crossing time		-	12.5	-	ns

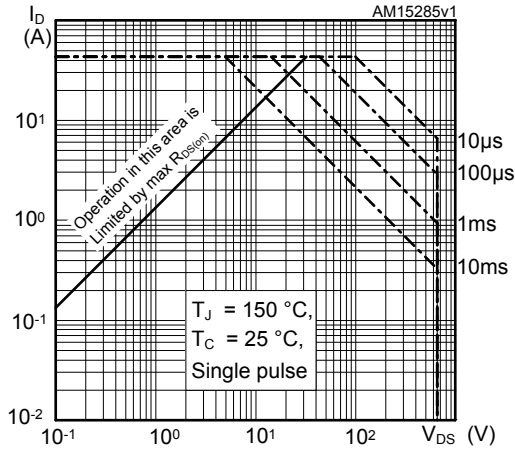
**Table 7. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-	-	11	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-	-	44	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 11\text{ A}$ , $V_{GS} = 0\text{ V}$	-	-	1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 11\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,	-	247	-	ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 100\text{ V}$	-	2.4	-	$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see the Figure 16. Test circuit for inductive load switching and diode recovery times)	-	19.5	-	A
$t_{rr}$	Reverse recovery time	$I_{SD} = 11\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,	-	312	-	ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 100\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$	-	3	-	$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see the Figure 16. Test circuit for inductive load switching and diode recovery times)	-	19	-	A

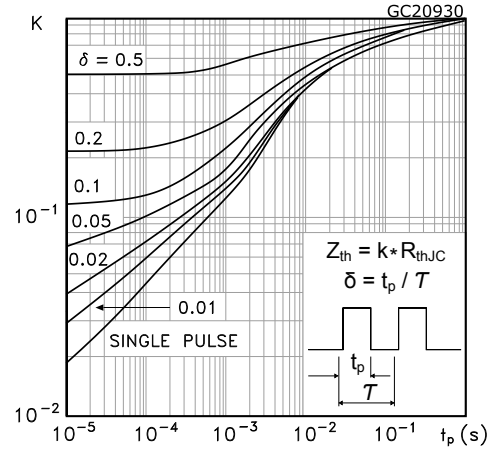
1. Pulse width is limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics curves

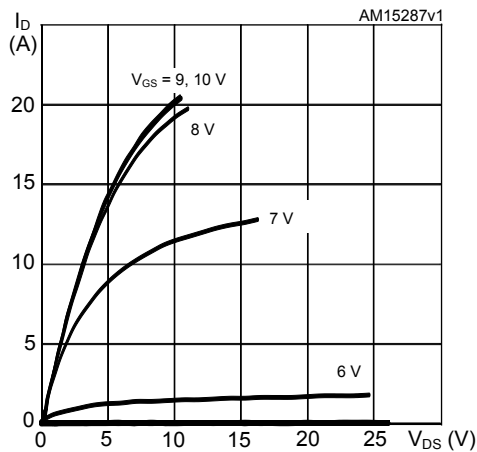
**Figure 1. Safe operating area**



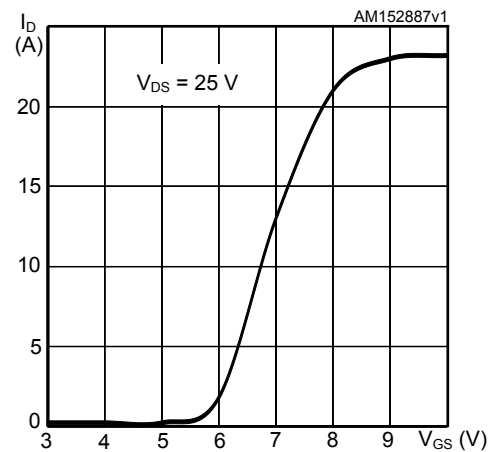
**Figure 2. Normalized transient thermal impedance**



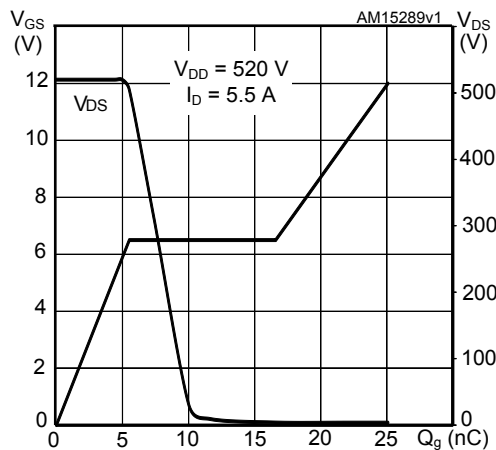
**Figure 3. Typical output characteristics**



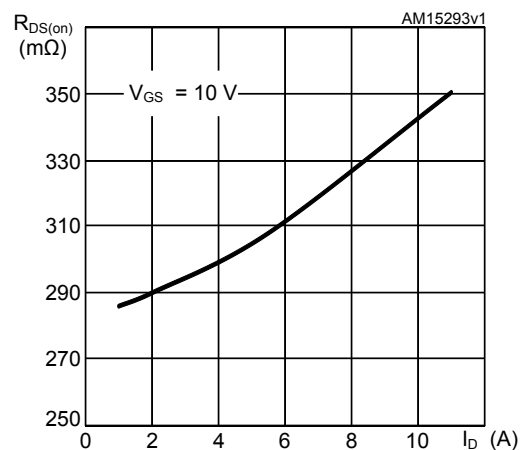
**Figure 4. Typical transfer characteristics**



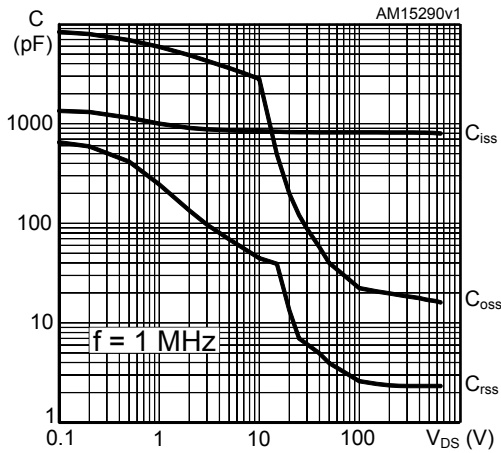
**Figure 5. Typical gate charge characteristics**



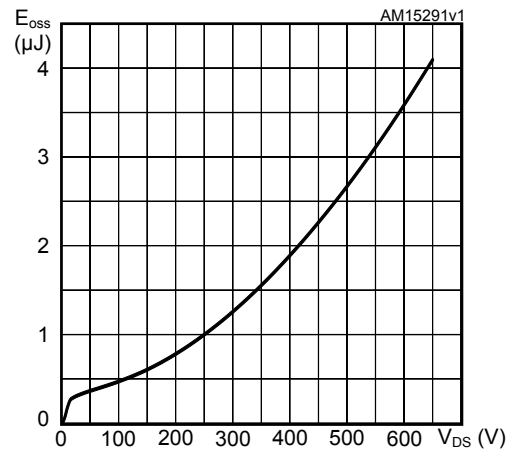
**Figure 6. Typical drain-source on-resistance**



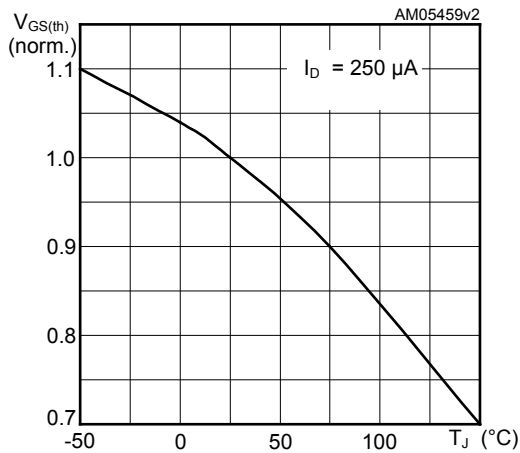
**Figure 7. Typical capacitance characteristics**



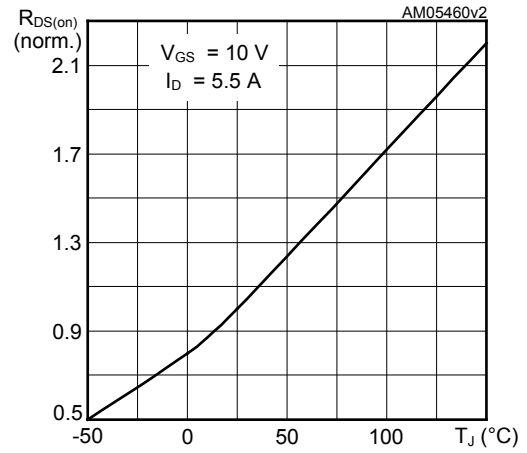
**Figure 8. Typical output capacitance stored energy**



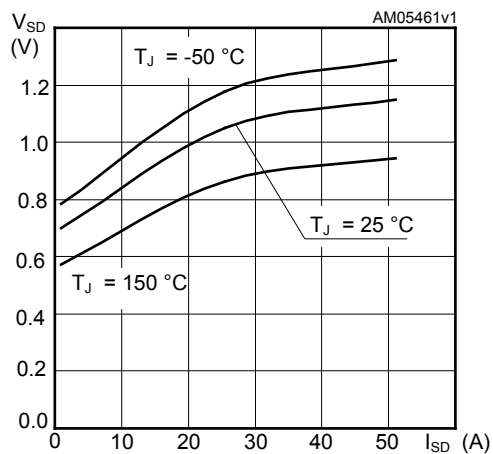
**Figure 9. Normalized gate threshold vs temperature**



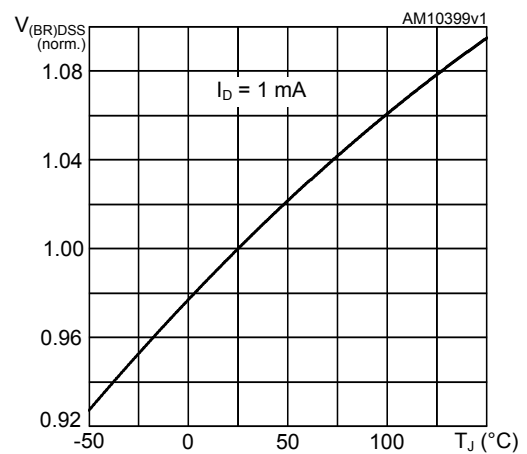
**Figure 10. Normalized on-resistance vs temperature**



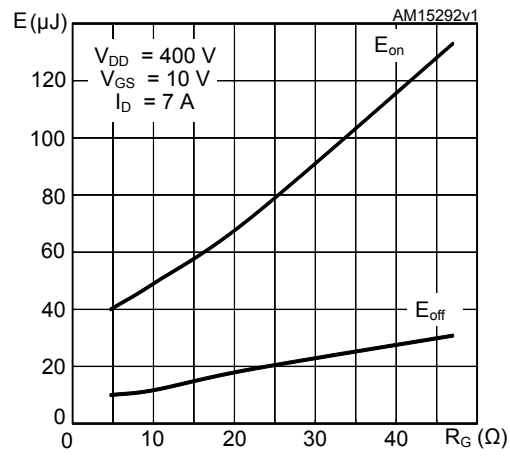
**Figure 11. Typical reverse diode forward characteristics**



**Figure 12. Normalized breakdown voltage vs temperature**

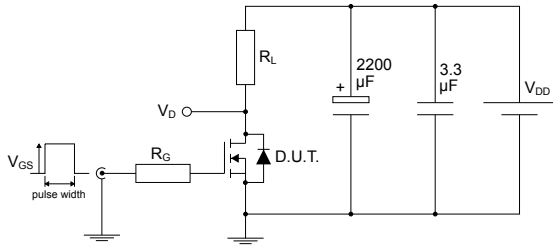


**Figure 13. Typical switching energy vs gate resistance**

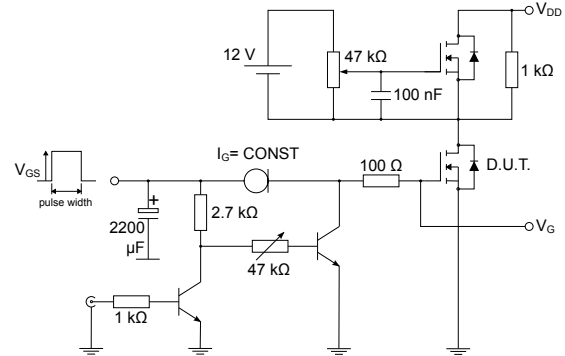


Note:  $E_{on}$  including reverse recovery of a SiC diode.

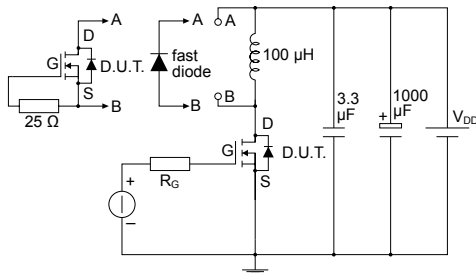
### 3 Test circuits

**Figure 14. Test circuit for resistive load switching times**


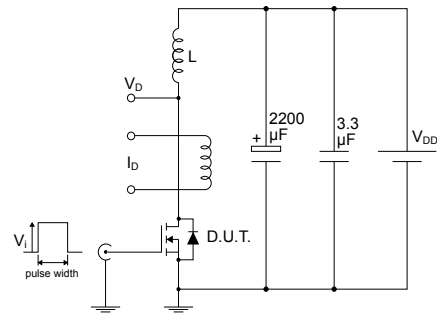
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**Figure 15. Test circuit for gate charge behavior**


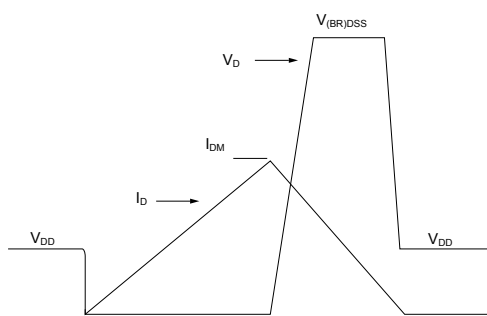
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**Figure 16. Test circuit for inductive load switching and diode recovery times**


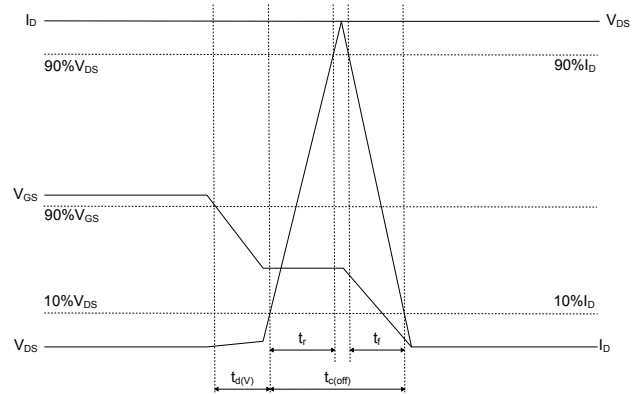
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**Figure 17. Unclamped inductive load test circuit**


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**Figure 18. Unclamped inductive waveform**


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**Figure 19. Switching time waveform**


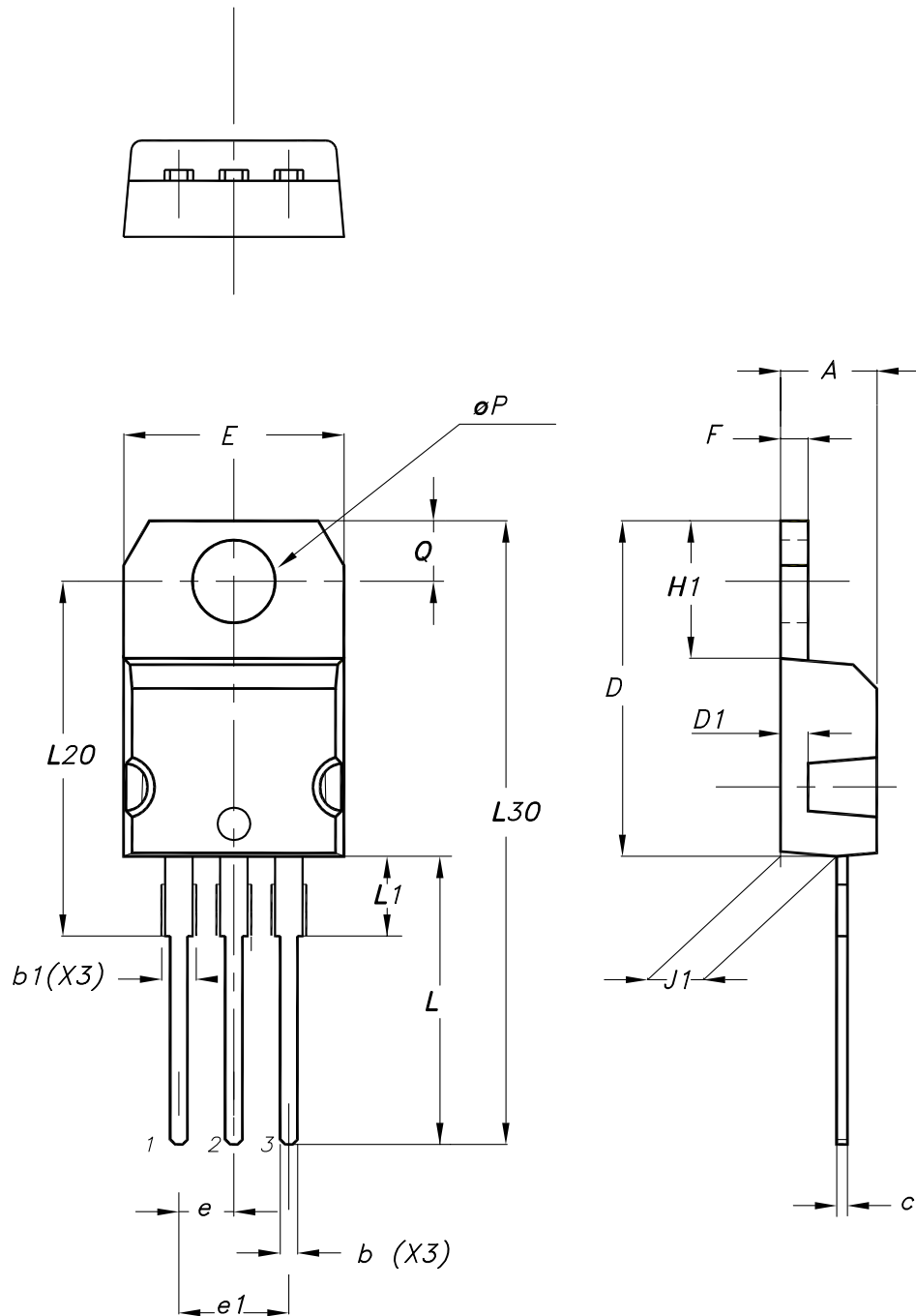
AM05540v2

## 4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 TO-220 type A package information

Figure 20. TO-220 type A package outline



0015988\_typeA\_Rev\_24

**Table 8. TO-220 type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

## Revision history

Table 9. Document revision history

Date	Revision	Changes
05-Mar-2012	1	First release.
09-Nov-2012	2	The part number STB15N65M5 has been moved to a separate datasheet. Added <i>Section 2.1: Electrical characteristics (curves)</i> . Minor text changes.
03-Feb-2026	3	Removed order code STF15N65M5 and STFI15N65M5. Updated <i>Section 4: Package information</i> . Minor text changes.

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