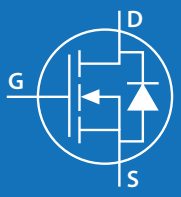
EPC8009 – Enhancement Mode Power Transistor

V_{DS}, 65 V
$R_{DS(on)}$, 130 mΩ
I_D, 4 A



EFFICIENT POWER CONVERSION

RoHS Halogen-Free

Revised July 7, 2023

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Questions: Ask a GaN Expert

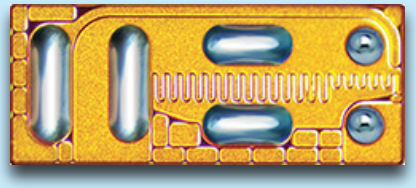
Maximum Ratings			
PARAMETER		**VALUE**	**UNIT**
V_{DS}	Drain-to-Source Voltage (Continuous)	65	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 125°C)	78	
I_D	Continuous (T_A = 25°C, $R_{\theta JA}$ = 33°C/W)	4	A
	Pulsed (25°C, T_{PULSE} = 300 µs)	7.5	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	–4	
T_J	Operating Temperature	–40 to 150	°C
T_{STG}	Storage Temperature	–40 to 150	

Thermal Characteristics			
PARAMETER		**TYP**	**UNIT**
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	8.2	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	16	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	82	

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details

Static Characteristics (T_J = 25°C unless otherwise stated)						
PARAMETER		**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 125 µA	65			V
I_{DSS}	Drain-Source Leakage	V_{GS} = 0 V, V_{DS} = 52 V		50	100	µA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		100	500	µA
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		50	100	
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 0.25 mA	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 0.5 A		90	130	mΩ
V_{SD}	Source-Drain Forward Voltage#	V_{GS} = 0 V, I_S = 0.5 A		2.2		V

Defined by design. Not subject to production test.
All measurements were done with substrate connected to source.
Specifications are with substrate connected to source where applicable.



Die size: 2.1 x 0.85 mm

EPC8009 eGaN FETs are supplied only in passivated die form with solder bars.

Applications

- Ultra high speed DC-DC conversion
- RF envelope tracking
- Wireless power transfer
- Game console and industrial movement sensing (Lidar)

Benefits

- Ultra high efficiency
- Ultra low $R_{DS(on)}$
- Ultra low Q_G
- Ultra small footprint

Scan QR code or click link below for more information including reliability reports, device models, demo boards!

https://l.ead.me/EPC8009

Dynamic Characteristics# (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 32.5 V		45	52	pF
C_{OSS}	Output Capacitance			19	28	
C_{RSS}	Reverse Transfer Capacitance			0.5	0.8	
R_G	Gate Resistance			0.3		Ω
Q_G	Total Gate Charge	V_{GS} = 5 V, V_{DS} = 32.5 V, I_D = 1 A		370	450	pC
Q_{GS}	Gate-to-Source Charge			120		
Q_{GD}	Gate-to-Drain Charge			55	94	
$Q_{G(TH)}$	Gate Charge at Threshold			96		
Q_{OSS}	Output Charge	V_{GS} = 0 V, V_{DS} = 32.5 V		940	1400	
Q_{RR}	Source-Drain Recovery Charge			0		

Defined by design. Not subject to production test.
All measurements were done with substrate connected to source.
Specifications are with substrate connected to source where applicable.

Figure 1: Typical Output Characteristics at 25°C

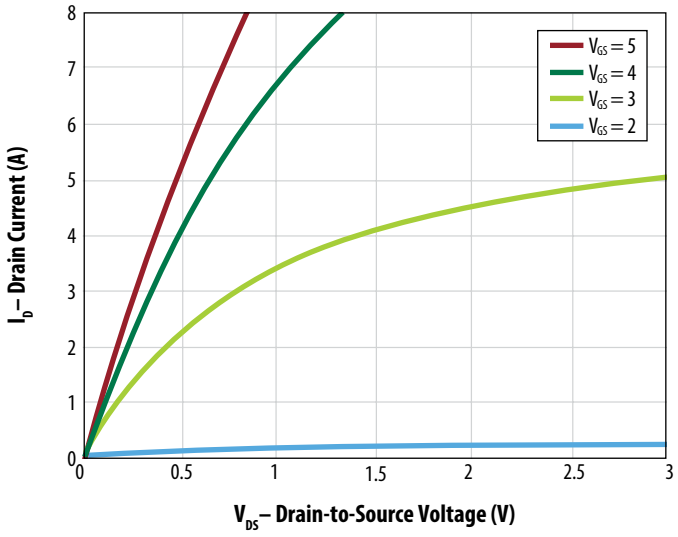


Figure 2: Typical Transfer Characteristics

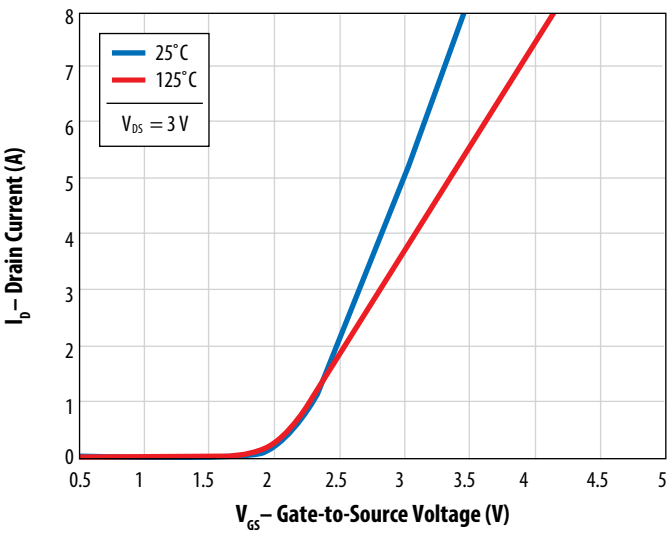


Figure 3: Typical $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

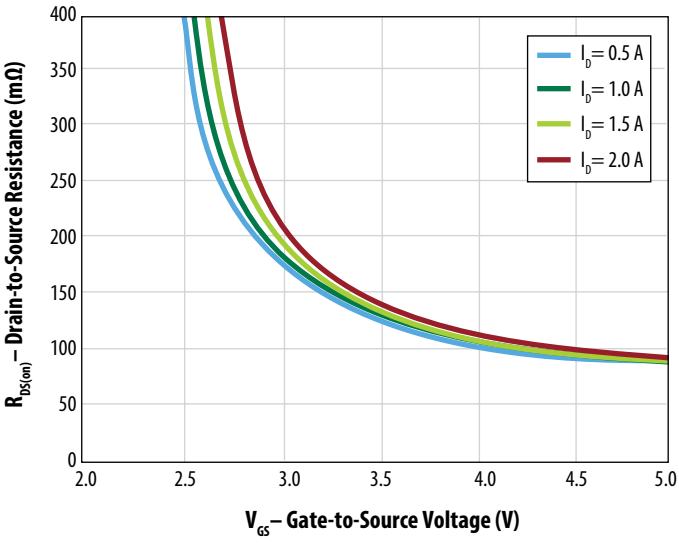


Figure 4: Typical $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

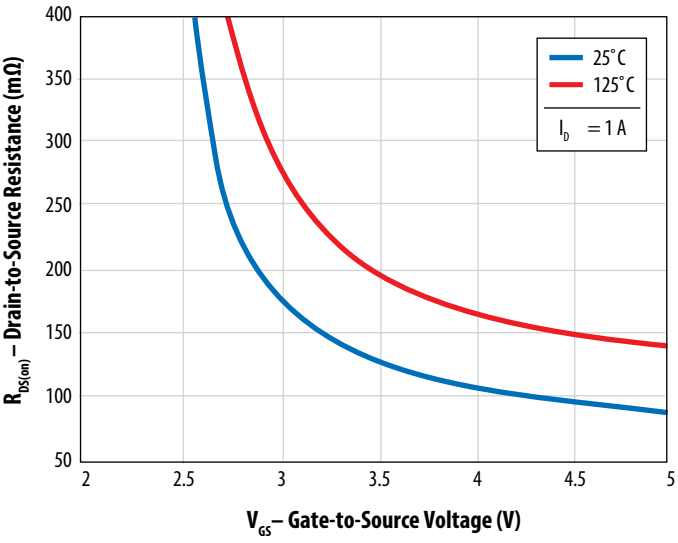


Figure 5: Typical Capacitance (Linear Scale)

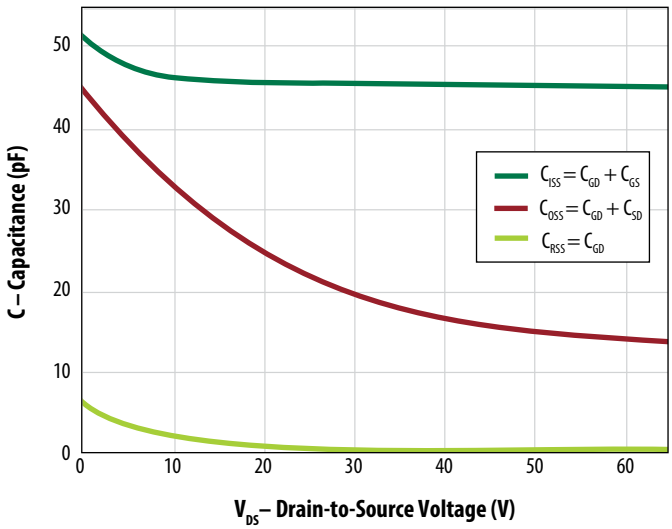


Figure 5A: Typical Capacitance (Log Scale)

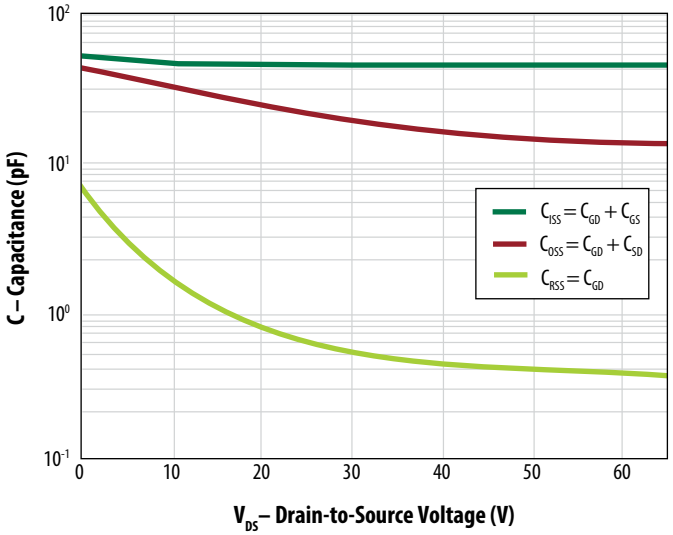


Figure 6: Typical Gate Charge

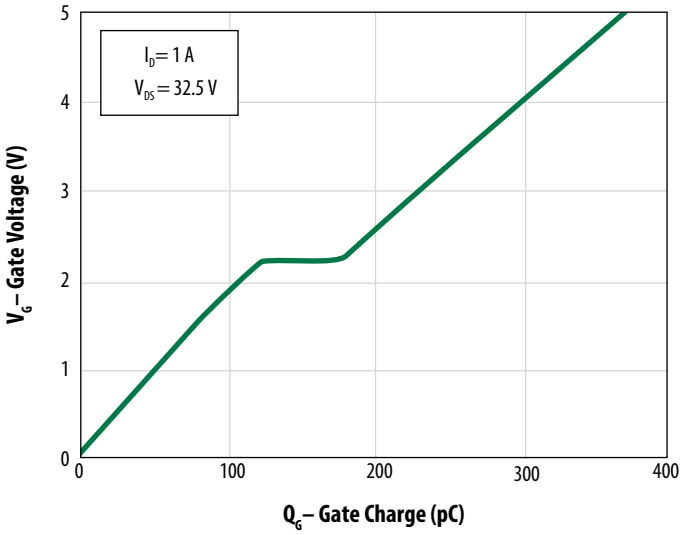
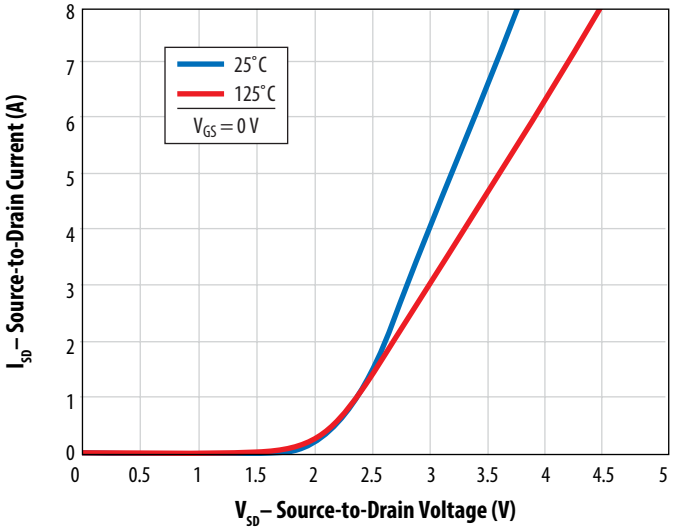


Figure 7: Typical Reverse Drain-Source Characteristics



Note: Negative gate drive voltage increases the reverse drain-source voltage. EPC recommends 0 V for OFF.

Figure 8: Typical Normalized $R_{DS(on)}$

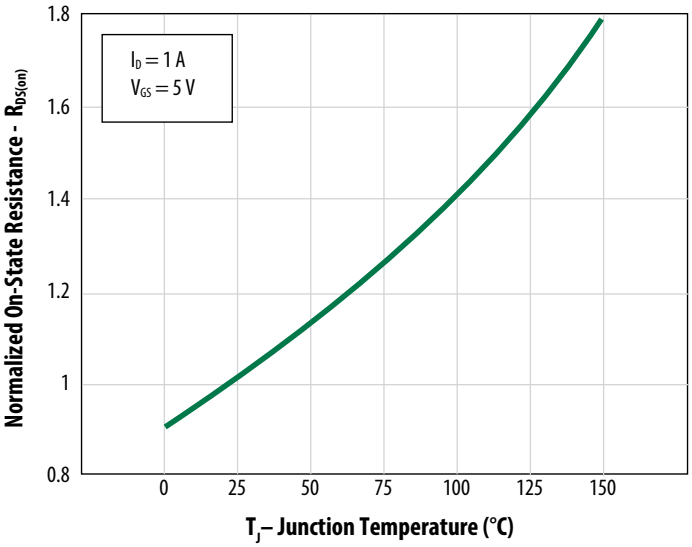


Figure 9: Typical Normalized Threshold Voltage vs. Temp.

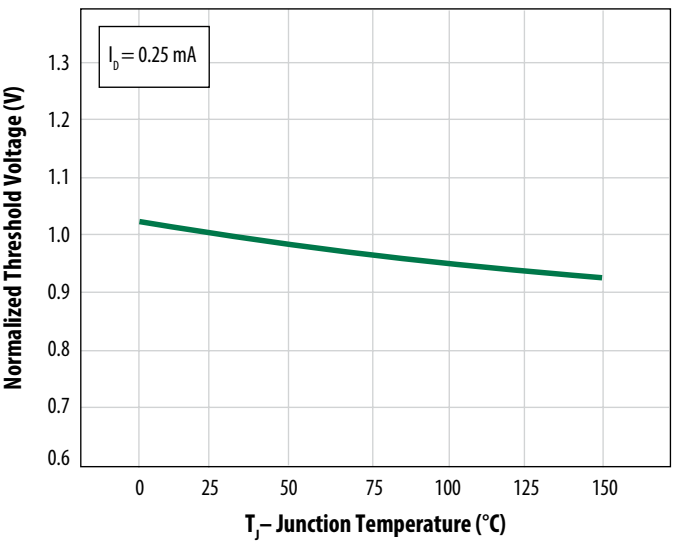


Figure 10: Typical Gate Current

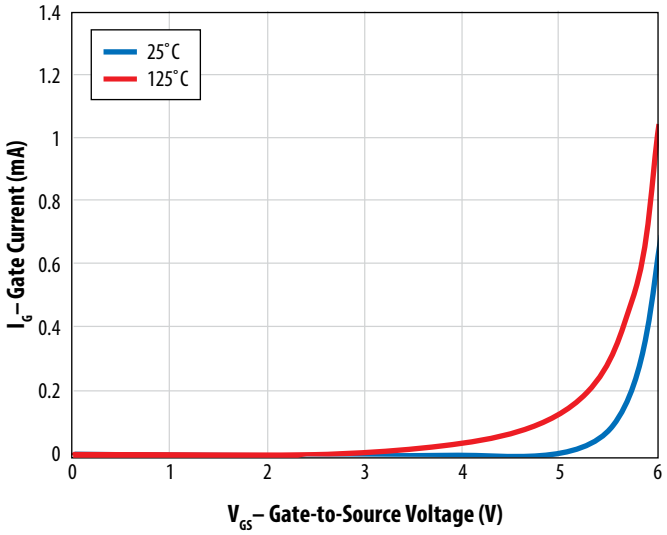


Figure 11: Smith Chart

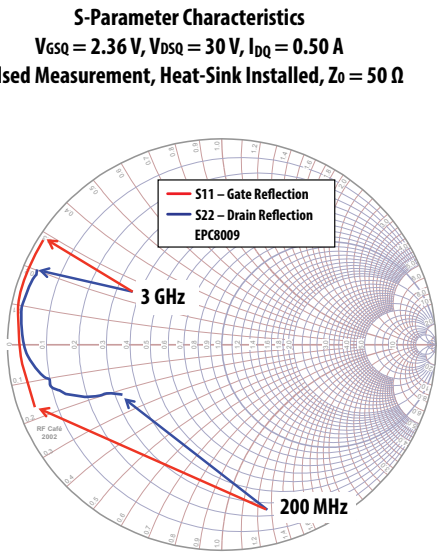


Figure 12: Gain Chart

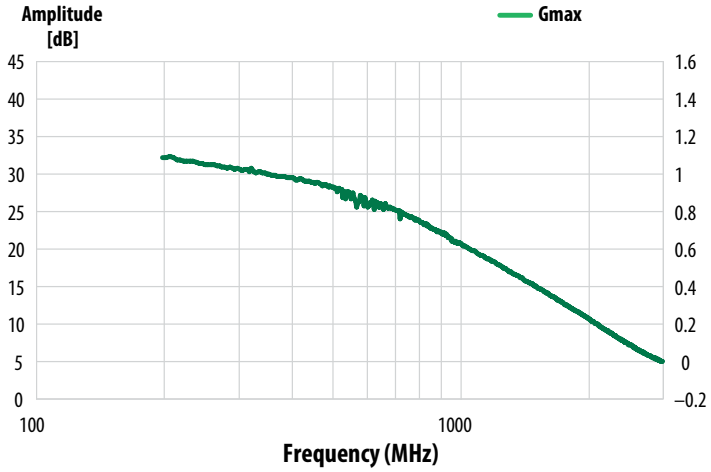
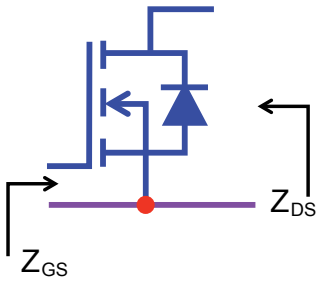


Figure 13: Device Reflection



Frequency	Gate (Z_{GS})	Drain (Z_{DS})
[MHz]	[Ω]	[Ω]
200	1.98 – j8.58	16.83 – j11.29
500	1.87 – j2.15	10.69 – j9.69
1000	1.39 + j2.14	5.22 – j5.45
1200	1.21 + j3.56	3.53 – j3.42
1500	1.01 + j4.96	2.35 – j0.81
2000	0.83 + j7.83	1.57 + j3.52
2400	0.73 + j10.14	1.54 + j6.19
3000	0.58 + j14.27	1.84 + j10.20

S-Parameter Table - Download S-parameter files at ***www.epc-co.com***

Figure 14: Taper and Reference Plane details – Device Connection

Micro-Strip design: 2-layer
½ oz (17.5 µm) thick copper
30 mil thick RO4350 substrate

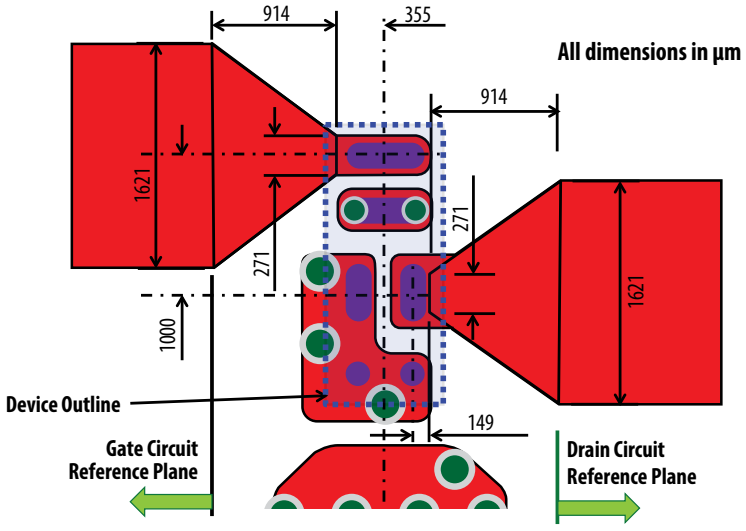


Figure 15: Typical Transient Thermal Response Curves

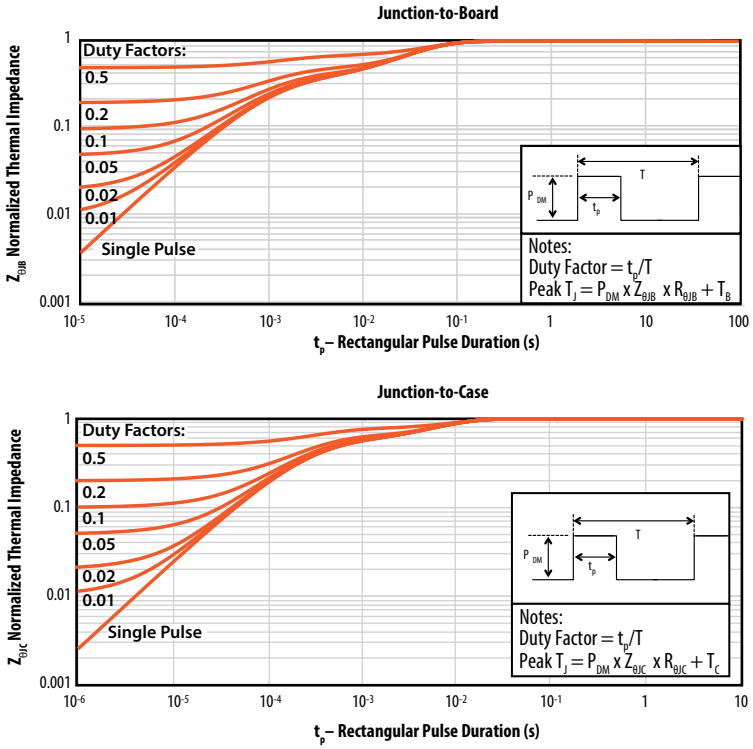
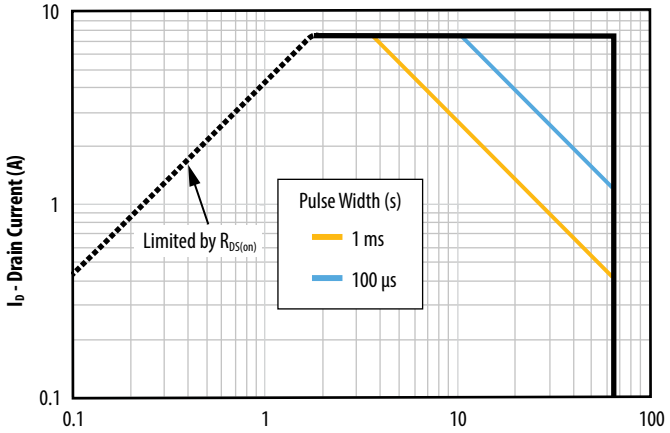
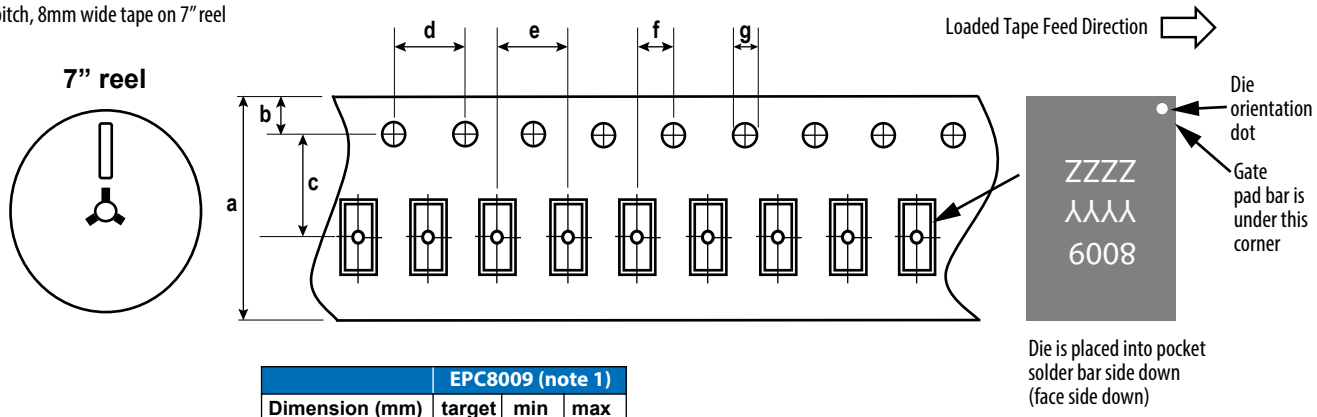


Figure 16: Safe Operating Area



TAPE AND REEL CONFIGURATION

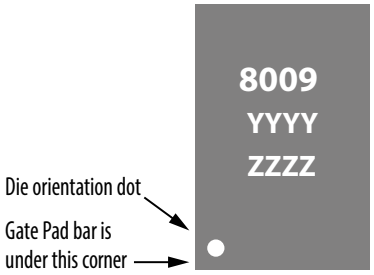
4mm pitch, 8mm wide tape on 7" reel



	EPC8009 (note 1)		
Dimension (mm)	**target**	**min**	**max**
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (see note)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (see note)	2.00	1.95	2.05
g	1.5	1.5	1.6

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.
Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

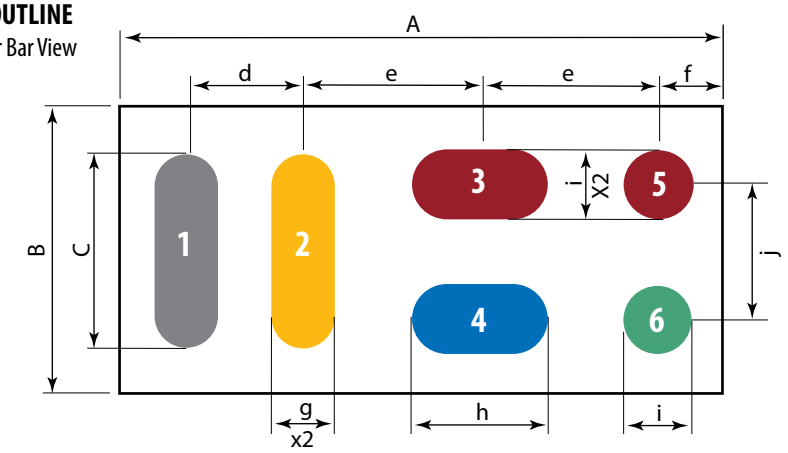
DIE MARKINGS

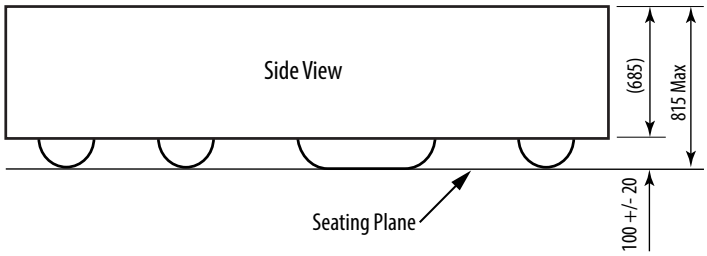


Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking line 2	Lot_Date Code Marking Line 3
EPC8009	8009	YYYY	ZZZZ

DIE OUTLINE

Solder Bar View



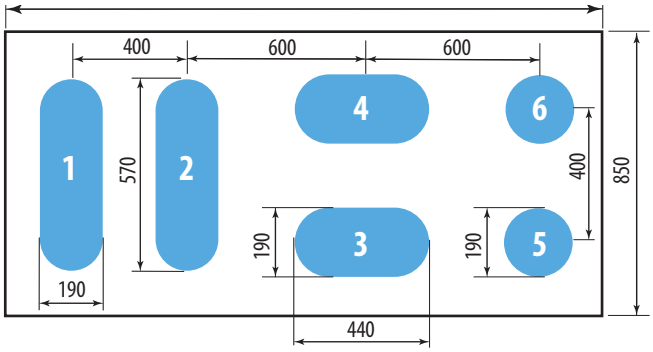


Dim	Micrometers		
	Min	Nominal	Max
A	2020	2050	2080
B	820	850	880
C	555	580	605
d	400	400	400
e	600	600	600
f	200	225	250
g	175	200	225
h	425	450	475
i	175	200	225
j	400	400	400

Pad no. 1 is Gate
Pad no. 2 is Source Return for Gate Driver
Pad no. 3 and 5 are Source
Pad no. 4 is Drain
Pad no. 6 is Substrate*

*Substrate pin should be connected to Source

RECOMMENDED LAND PATTERN *(measurements in µm)*

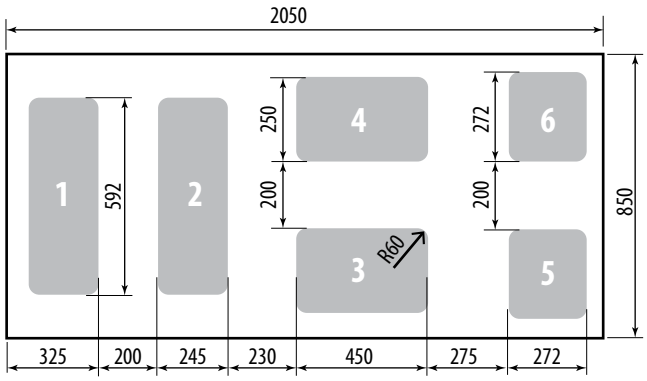


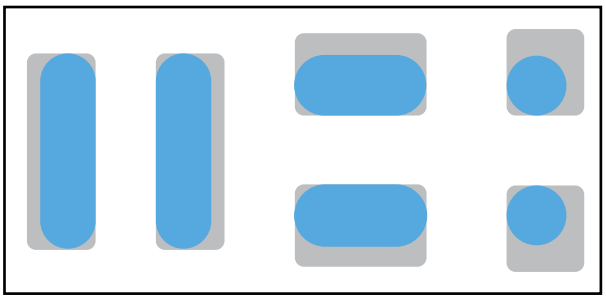
The land pattern is solder mask defined.

Pad no. 1 is Gate
Pad no. 2 is Source Return for Gate Driver
Pad no. 3 and 5 are Source
Pad no. 4 is Drain
Pad no. 6 is Substrate*

*Substrate pin should be connected to Source

RECOMMENDED STENCIL DRAWING *(measurements in µm)*





Blue = bump, Gray = stencil

Recommended stencil should be 4 mil (100 µm) thick, must be laser cut, openings per drawing. Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Additional assembly resources available at: https://epc-co.com/epc/design-support