



32K x 8 Static RAM

Features

- 55, 70 ns access time
- CMOS for optimum speed/power
- Wide voltage range: 2.7V–3.6V
- Low active power (70 ns, LL version)
— 108 mW (max.)
- Low standby power (70 ns, LL version)
— 18 μ W (max.)
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- TTL-compatible inputs and outputs
- Automatic power-down when deselected

Functional Description

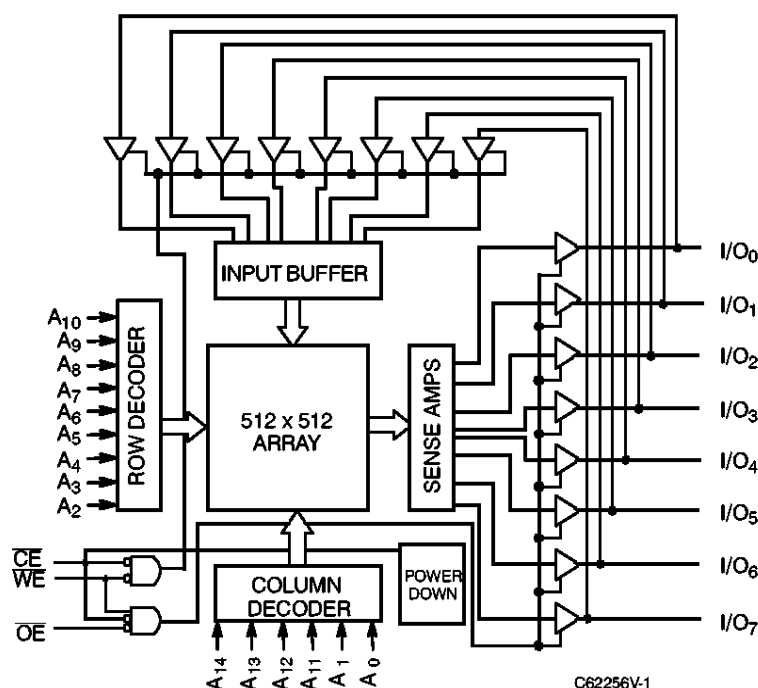
The CY62256V is a high-performance CMOS static RAM organized as 32,768 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and active LOW output enable ($\overline{OE}$) and three-state drivers. This device has an automatic power-down feature, reducing the power consumption by 98% when deselected. The CY62256V is in the standard 450-mil-wide (300-mil body width) SOIC, TSOP, and reverse TSOP packages.

An active LOW write enable signal ($\overline{WE}$) controls the writing/reading operation of the memory. When $\overline{CE}$ and $\overline{WE}$ inputs are both LOW, data on the eight data input/output pins

output pins (I/O₀ through I/O₇) is written into the memory location addressed by the address present on the address pins (A₀ through A₁₄). Reading the device is accomplished by selecting the device and enabling the outputs, $\overline{CE}$ and $\overline{OE}$ active LOW, while $\overline{WE}$ remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins is present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable ($\overline{WE}$) is HIGH. A die coat is used to ensure alpha immunity.

Logic Block Diagram



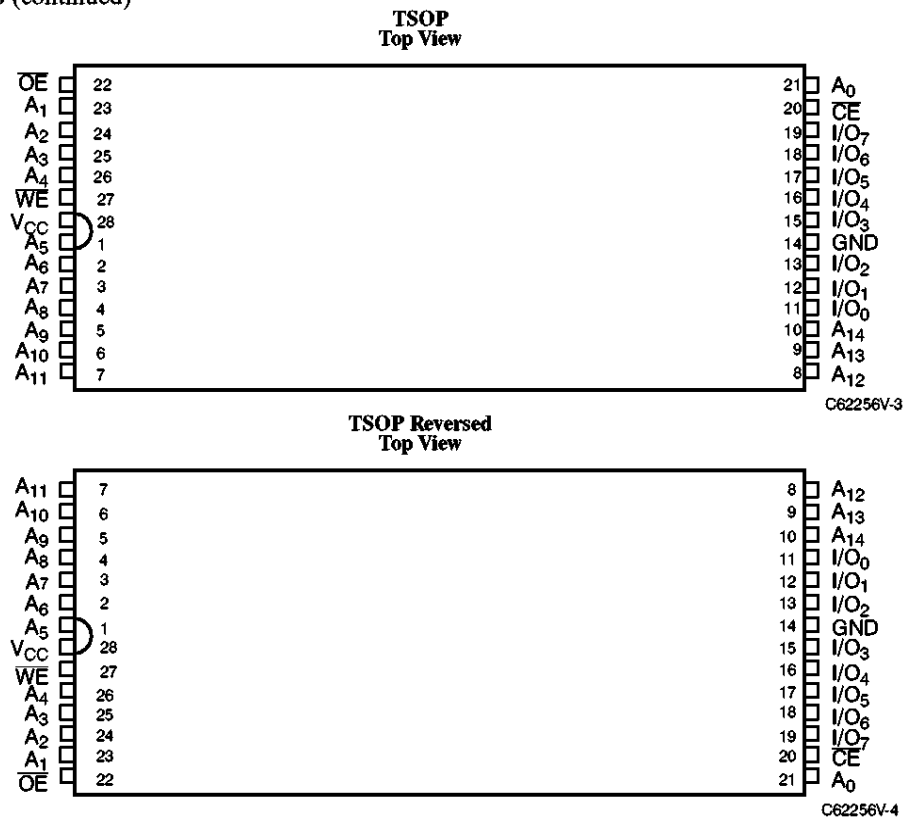
Pin Configurations

SOIC Top View			
A ₅	1	28	V _{CC}
A ₆	2	27	$\overline{WE}$
A ₇	3	26	A ₄
A ₈	4	25	A ₃
A ₉	5	24	A ₂
A ₁₀	6	23	A ₁
A ₁₁	7	22	$\overline{OE}$
A ₁₂	8	21	A ₀
A ₁₃	9	20	$\overline{CE}$
A ₁₄	10	19	I/O ₇
I/O ₀	11	18	I/O ₆
I/O ₁	12	17	I/O ₅
I/O ₂	13	16	I/O ₄
GND	14	15	I/O ₃

C62256V-2



Pin Configurations (continued)



Selection Guide

		CY62256V-55	CY62256V-70
Maximum Access Time (ns)		55	70
Maximum Operating Current (mA)		50	50
	L	50	50
	LL	30	30
Maximum Standby Current (μA)		500	500
	L	50	50
	LL	5	5

Shaded area contains advanced information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C
 Ambient Temperature with
 Power Applied 0°C to +70°C
 Supply Voltage to Ground Potential
 (Pin 28 to Pin 14) -0.5V to +4.6V
 DC Voltage Applied to Outputs
 in High Z State^[1] -0.5V to V_{CC} + 0.5V

DC Input Voltage^[1] -0.5V to V_{CC} + 0.5V
 Output Current into Outputs (LOW) 20 mA
 Static Discharge Voltage >2001V
 (per MIL-STD-883, Method 3015)
 Latch-Up Current >200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	2.7V to 3.6V

Notes:

1. V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.



Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CY62256V-55		CY62256V-70		Unit
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -1.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 2.1 mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC} + 0.3V	2.2	V _{CC} + 0.3V	V
V _{IL}	Input LOW Voltage		-0.5	0.8	-0.5	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-1	+1	-1	+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-5	+5	-5	+5	μA
I _{OS}	Output Short Circuit Current ^[2]	V _{CC} = Max., V _{OUT} = GND		-200		-200	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}		50		50	mA
			L	50		50	
			LL	30		30	
I _{SB1}	Automatic CE Power-Down Current—TTL Inputs	Max. V _{CC} , $\overline{CE} \geq V_{IH}$, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}		5		5	mA
			L	3		3	
			LL	1		1	
I _{SB2}	Automatic CE Power-Down Current—CMOS Inputs	Max. V _{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V, f = 0		500		500	μA
			L	50		50	
			LL	5		5	

Shaded area contains advanced information.

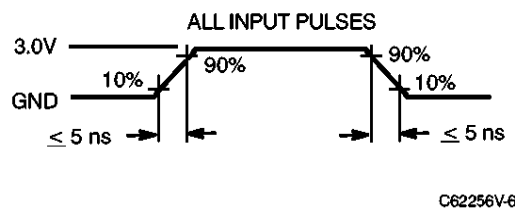
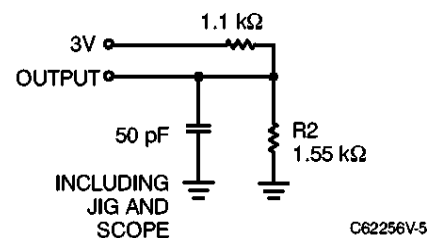
Capacitance^[3]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 3.0V	6	pF
C _{OUT}	Output Capacitance		8	pF

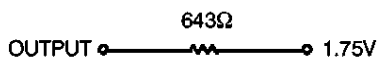
Note:

- Not more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms

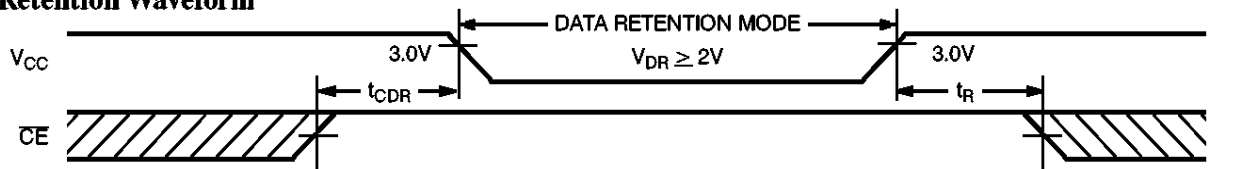


Equivalent to: THÉVENIN EQUIVALENT



Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions ^[4]	Min.	Max.	Unit
V_{DR}	V_{CC} for Data Retention		2.0		V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 3.0V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		200	μA
				20	μA
				5	μA
$t_{CDR}^{[3]}$	Chip Deselect to Data Retention Time		0		ns
$t_R^{[3]}$	Operation Recovery Time		t_{RC}		ns

Data Retention Waveform


C62256V-7

Switching Characteristics Over the Operating Range^[5]

Parameter	Description	CY62256V–55		CY62256V–70		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t _{RC}	Read Cycle Time	55		70		ns
t _{AA}	Address to Data Valid		55		70	ns
t _{OHA}	Data Hold from Address Change	3		3		ns
t _{ACE}	$\overline{CE}$ LOW to Data Valid		55		70	ns
t _{DOE}	$\overline{OE}$ LOW to Data Valid		25		35	ns
t _{LZOE}	$\overline{OE}$ LOW to Low Z ^[6]	3		3		ns
t _{HZOE}	$\overline{OE}$ HIGH to High Z ^[6, 7]		20		25	ns
t _{LZCE}	$\overline{CE}$ LOW to Low Z ^[6]	3		3		ns
t _{HZCE}	$\overline{CE}$ HIGH to High Z ^[6, 7]		20		25	ns
t _{PU}	$\overline{CE}$ LOW to Power-Up	0		0		ns
t _{PD}	$\overline{CE}$ HIGH to Power-Down		55		70	ns

Shaded area contains advanced information.

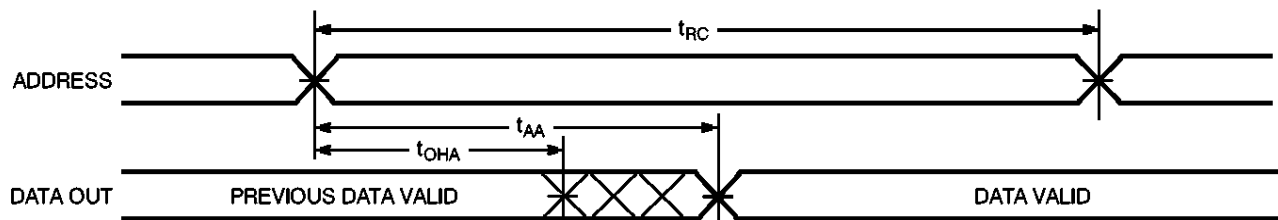
Notes:

- No input may exceed $V_{CC} + 0.3V$.
- Test conditions assume signal transition time of 5 ns or less timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 100-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.

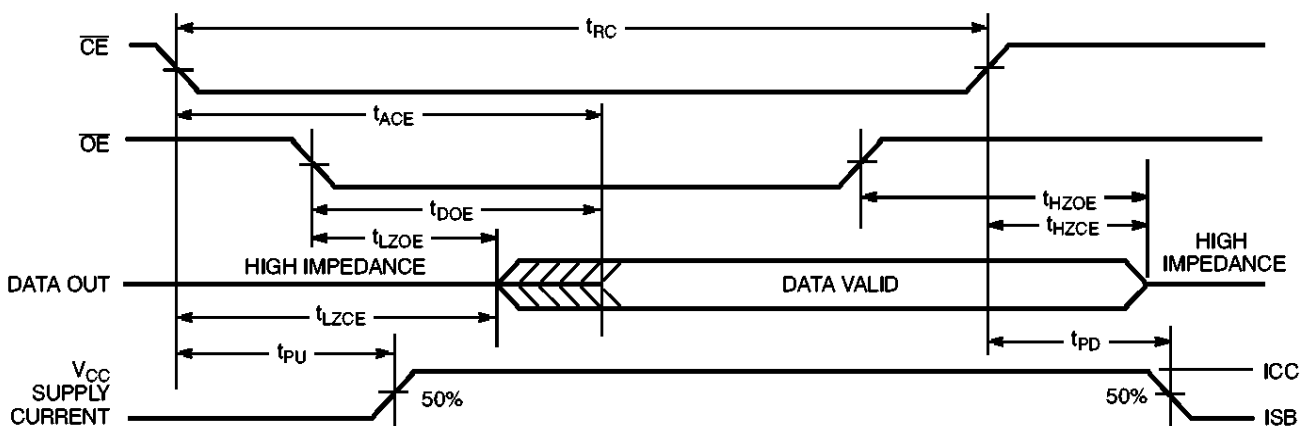
Switching Characteristics Over the Operating Range^[5]

Parameter	Description	CY62256V–55		CY62256V–70		Unit
		Min.	Max.	Min.	Max.	
WRITE CYCLE ^[8, 9]						
tWC	Write Cycle Time	55		70		ns
tSCE	$\overline{\text{CE}}$ LOW to Write End	45		60		ns
tAW	Address Set-Up to Write End	45		60		ns
tHA	Address Hold from Write End	0		0		ns
tSA	Address Set-Up to Write Start	0		0		ns
tPWE	$\overline{\text{WE}}$ Pulse Width	40		50		ns
tSD	Data Set-Up to Write End	25		30		ns
tHD	Data Hold from Write End	0		0		ns
tHZWE	$\overline{\text{WE}}$ LOW to High Z ^[6, 7]		20		25	ns
tLZWE	$\overline{\text{WE}}$ HIGH to Low Z ^[6]	3		3		ns

Shaded area contains advanced information.

Switching Waveforms
Read Cycle No. 1^[10, 11]


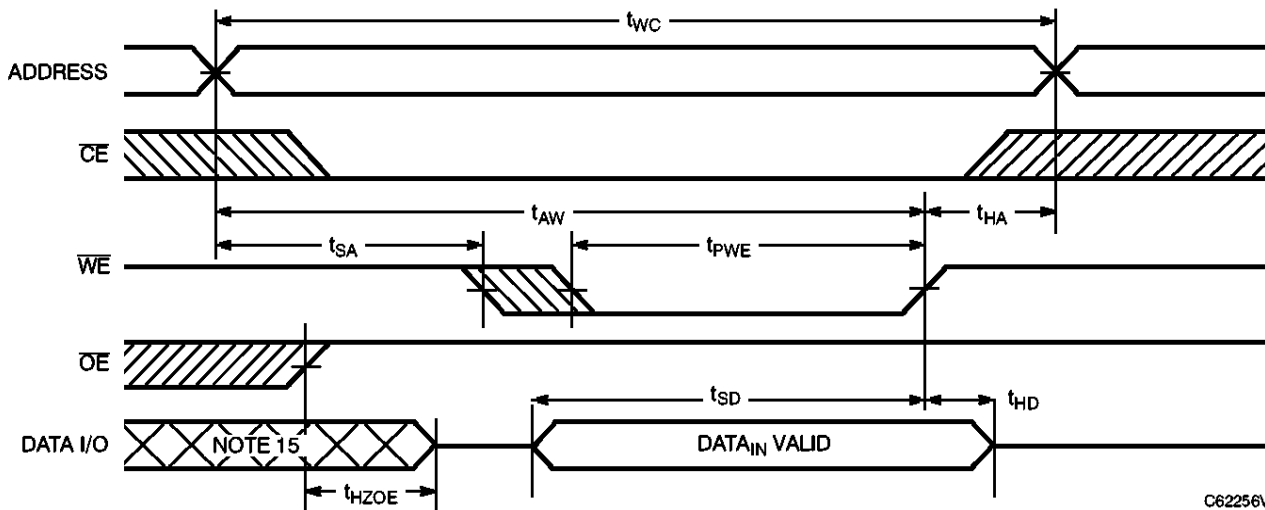
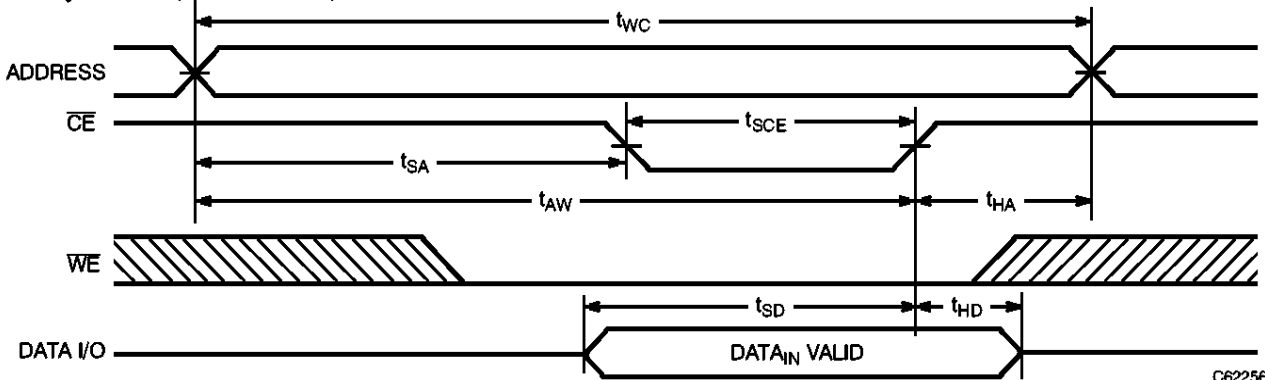
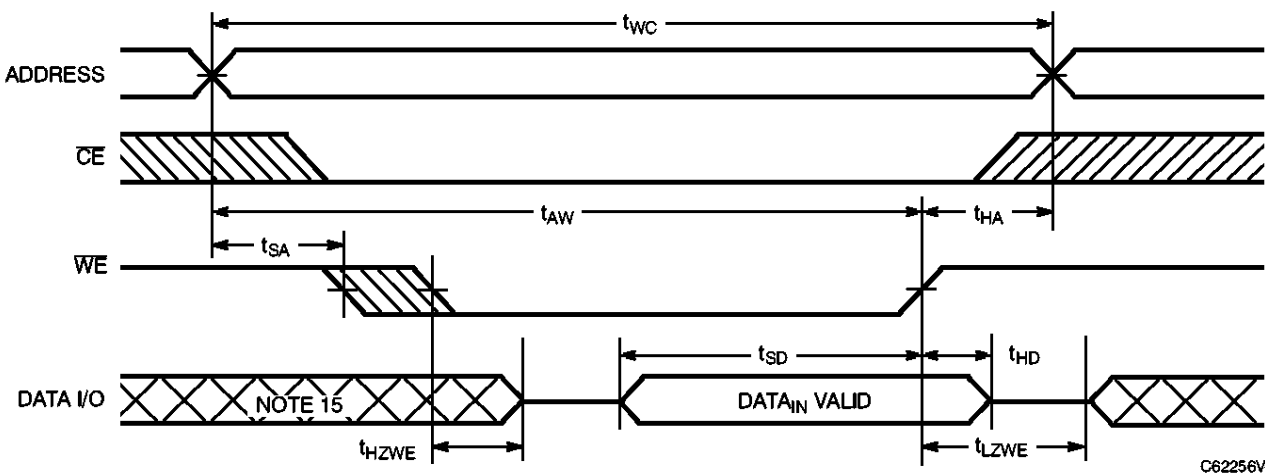
C62256V-8

Read Cycle No. 2^[11, 12]


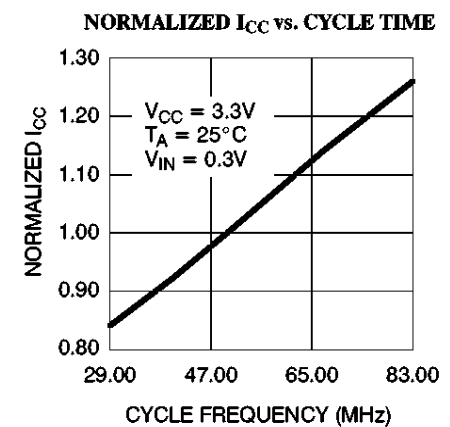
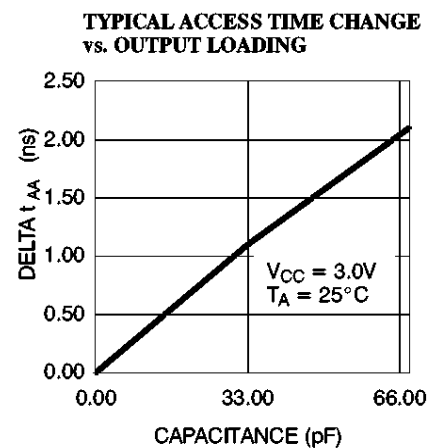
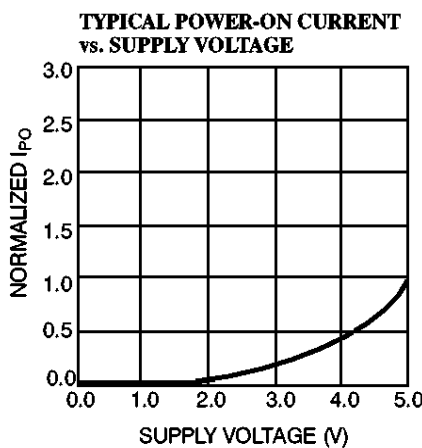
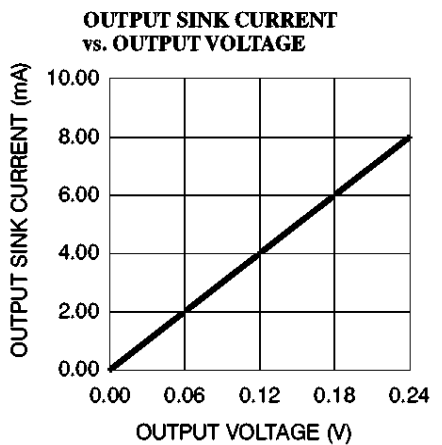
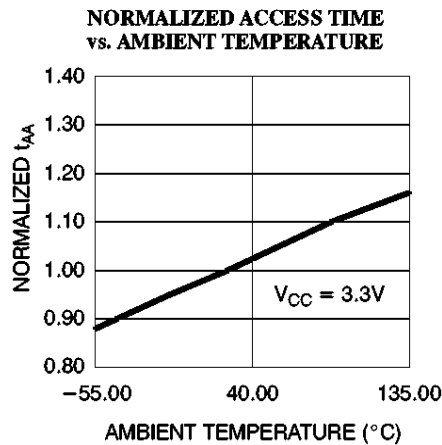
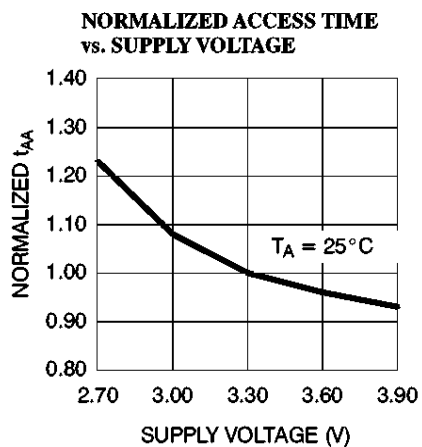
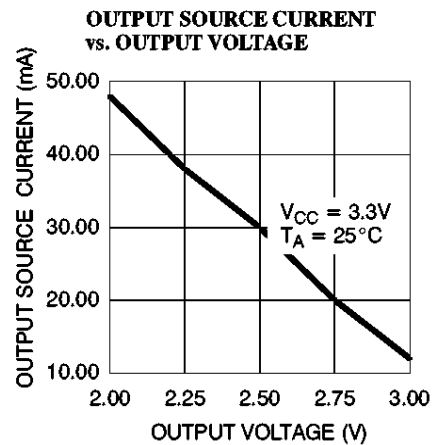
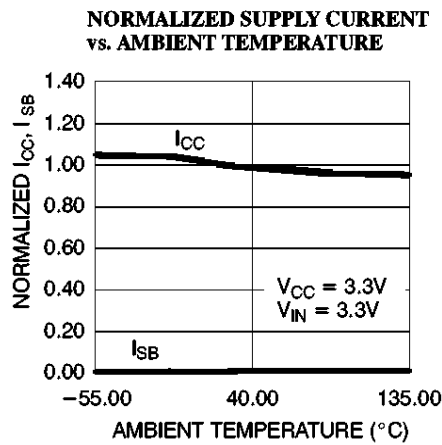
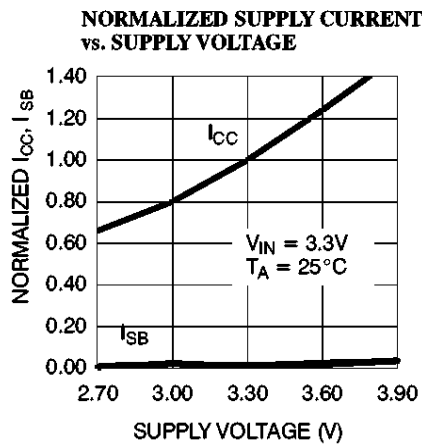
C62256V-9

Notes:

- The internal write time of the memory is defined by the overlap of $\overline{\text{CE}}$ LOW and $\overline{\text{WE}}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- The minimum write cycle time for write cycle #3 ($\overline{\text{WE}}$ controlled, $\overline{\text{OE}}$ LOW) is the sum of t_{HZWE} and t_{SD}.
- Device is continuously selected. $\overline{\text{OE}}, \overline{\text{CE}} = \text{V}_{\text{IL}}$.
- $\overline{\text{WE}}$ is HIGH for read cycle.
- Address valid prior to or coincident with $\overline{\text{CE}}$ transition LOW.

Switching Waveforms (continued)
Write Cycle No. 1 ($\overline{WE}$ Controlled)[8, 13, 14]

Write Cycle No. 2 ($\overline{CE}$ Controlled)[8, 13, 14]

Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[9, 14]

Notes:

13. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
14. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
15. During this period, the I/Os are in output state and input signals should not be applied.

Typical DC and AC Characteristics




Truth Table

CE	WE	OE	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	Data Out	Read	Active (I_{CC})
L	L	X	Data In	Write	Active (I_{CC})
L	H	H	High Z	Deselect, Output Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY62256V-55SNC	S22	28-Lead 450-Mil (300-Mil Body Width) SOIC	Commercial
	CY62256VL-55SNC	S22	28-Lead 450-Mil (300-Mil Body Width) SOIC	
	CY62256VLL-55SNC	S22	28-Lead 450-Mil (300-Mil Body Width) SOIC	
	CY62256V-55RZC	RZ28	28-Lead Reverse Thin Small Outline Package	
	CY62256VL-55RZC	RZ28	28-Lead Reverse Thin Small Outline Package	
	CY62256VLL-55RZC	RZ28	28-Lead Reverse Thin Small Outline Package	
	CY62256V-55ZC	Z28	28-Lead Thin Small Outline Package	
	CY62256VL-55ZC	Z28	28-Lead Thin Small Outline Package	
	CY62256VLL-55ZC	Z28	28-Lead Thin Small Outline Package	
70	CY62256V-70SNC	S22	28-Lead 450-Mil (300-Mil Body Width) SOIC	Commercial
	CY62256VL-70SNC	S22	28-Lead 450-Mil (300-Mil Body Width) SOIC	
	CY62256VLL-70SNC	S22	28-Lead 450-Mil (300-Mil Body Width) SOIC	
	CY62256V-70RZC	RZ28	28-Lead Reverse Thin Small Outline Package	
	CY62256VL-70RZC	RZ28	28-Lead Reverse Thin Small Outline Package	
	CY62256VLL-70RZC	RZ28	28-Lead Reverse Thin Small Outline Package	
	CY62256V-70ZC	Z28	28-Lead Thin Small Outline Package	
	CY62256VL-70ZC	Z28	28-Lead Thin Small Outline Package	
	CY62256VLL-70ZC	Z28	28-Lead Thin Small Outline Package	

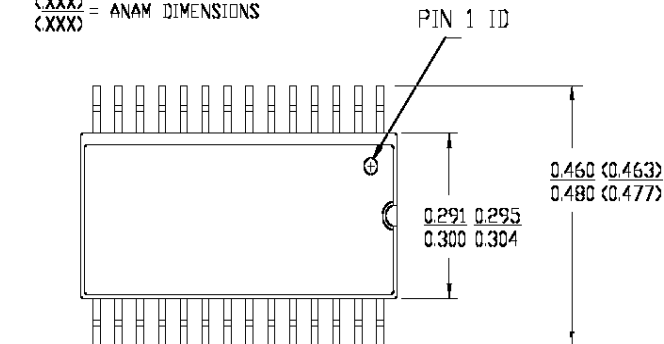
Shaded area contains advanced information.

Document #: 38-00519

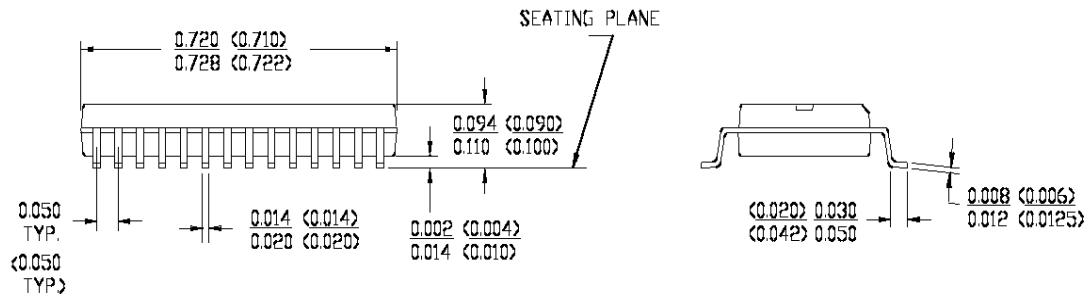
Package Diagrams
28-Lead 450-Mil (300-Mil Body Width) SOIC S22

XXX = HYUNDAI DIMENSIONS
xxx

(XXX) = ANAM DIMENSIONS
(xxx)

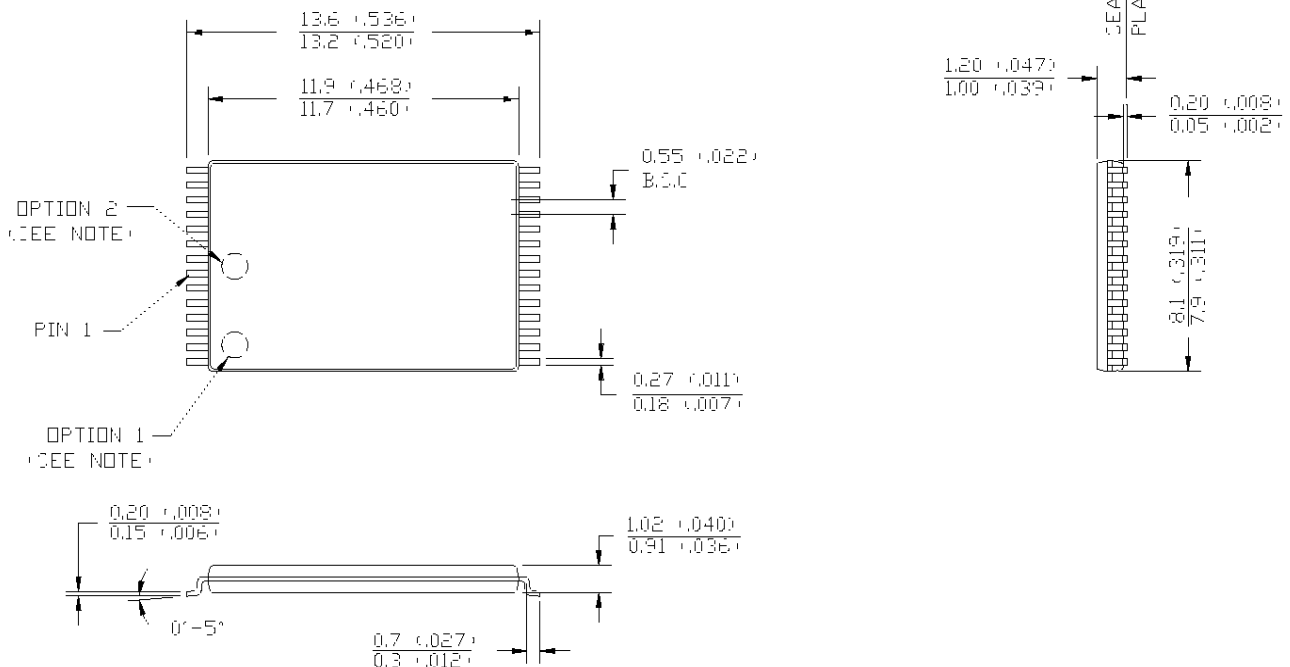


DIMENSIONS IN INCHES MIN.
MAX.
LEAD COPLANARITY 0.004 MAX.


28-Lead Reverse Thin Small Outline Package RZ28

NOTE: ORIENTATION I.D. MAY BE LOCATED EITHER
AS SHOWN IN OPTION 1 OR OPTION 2

DIMENSION IN MM (INCH)
MAX.
MIN.





Package Diagrams (continued)

28-Lead Thin Small Outline Package Z28

NOTE: ORIENTATION I.D. MAY BE LOCATED EITHER
AS SHOWN IN OPTION 1 OR OPTION 2

DIMENSION IN MM (INCH)
MAX.
MIN.

