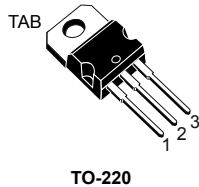
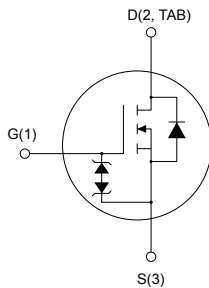


# N-channel 900 V, 720 mΩ typ., 7 A MDmesh K5 Power MOSFET in a TO-220 package



TO-220



AM01476v1\_tab

## Features

Order code	$V_{DS}$	$R_{DS(on)}$ max.	$I_D$
STP7N90K5	900 V	810 mΩ	7 A

- Very low FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

## Applications

- Switching applications

## Description

This very high voltage N-channel Power MOSFET is designed using MDmesh K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.



### Product status

STP7N90K5

### Device summary

<b>Order code</b>	STP7N90K5
<b>Marking</b>	7N90K5
<b>Package</b>	TO-220
<b>Packing</b>	Tube

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	7	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	4.4	A
$I_{DM}^{(1)}$	Drain current (pulsed)	28	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	110	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
$dv/dt^{(3)}$	MOSFET $dv/dt$ ruggedness	50	
$T_J$	Operating junction temperature range	- 55 to 150	$^\circ\text{C}$
$T_{stg}$	Storage temperature range		

1. Pulse width limited by safe operating area
2.  $I_{SD} \leq 7\text{ A}$ ,  $di/dt \leq 100\text{ A}/\mu\text{s}$ ;  $V_{DS(peak)} < V_{(BR)DSS}$ ,  $V_{DD} = 450\text{ V}$
3.  $V_{DD} \leq 720\text{ V}$

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Thermal resistance, junction-to-case	1.14	$^\circ\text{C}/\text{W}$
$R_{thJA}$	Thermal resistance, junction-to-ambient	62.5	$^\circ\text{C}/\text{W}$

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not repetitive (pulse width limited by $T_J$ max.)	2.4	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	230	mJ

## 2 Electrical characteristics

$T_C = 25\text{ °C}$  unless otherwise specified

**Table 4. On/off-state**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	900			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 900\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 900\text{ V}$ $T_C = 125\text{ °C}$ <sup>(1)</sup>			50	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DD} = V_{GS}$ , $I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 3.5\text{ A}$		720	810	$\text{m}\Omega$

1. Specified by design, not tested in production.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	425	-	$\text{pF}$
$C_{oss}$	Output capacitance		-	41	-	$\text{pF}$
$C_{riss}$	Reverse transfer capacitance		-	1.2	-	$\text{pF}$
$C_{o(tr)}$ <sup>(1)</sup>	Equivalent capacitance time related	$V_{GS} = 0$ , $V_{DS} = 0\text{ to }720\text{ V}$	-	64	-	$\text{pF}$
$C_{o(er)}$ <sup>(2)</sup>	Equivalent capacitance energy related				24	$\text{pF}$
$R_g$	Intrinsic gate resistance	$f = 1\text{ MHz}$ , $I_D = 0\text{ A}$	-	6.7	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 720\text{ V}$ , $I_D = 7\text{ A}$	-	12	-	$\text{nC}$
$Q_{gs}$	Gate-source charge	$V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior )	-	3.5	-	$\text{nC}$
$Q_{gd}$	Gate-drain charge		-	6.5	-	$\text{nC}$

1.  $C_{o(tr)}$  is a constant capacitance value that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

2.  $C_{o(er)}$  is a constant capacitance value that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 450\text{ V}$ , $I_D = 3.5\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	13.2	-	ns
$t_r$	Rise time		-	14.2	-	ns
$t_{d(off)}$	Turn-off delay time		-	31.6	-	ns
$t_f$	Fall time		-	14.7	-	ns

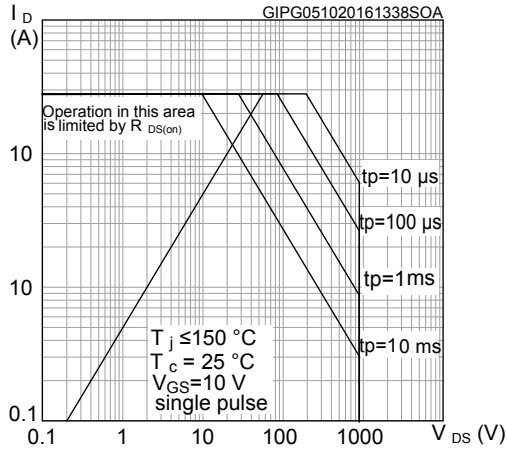
**Table 7. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		7	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		28	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 7\text{ A}$ , $V_{GS} = 0\text{ V}$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 7\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	352		ns
$Q_{rr}$	Reverse recovery charge		-	3.63		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	20.6		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 7\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	525		ns
$Q_{rr}$	Reverse recovery charge		-	4.94		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	18.8		A

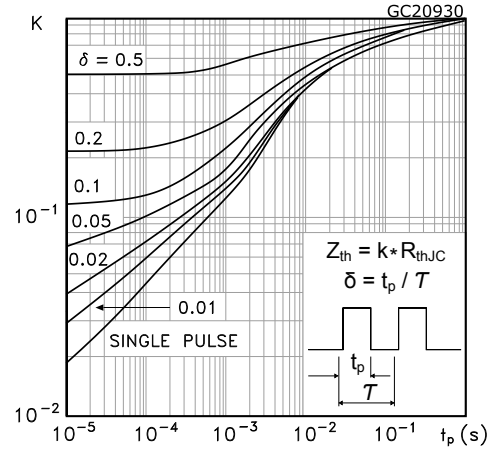
1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

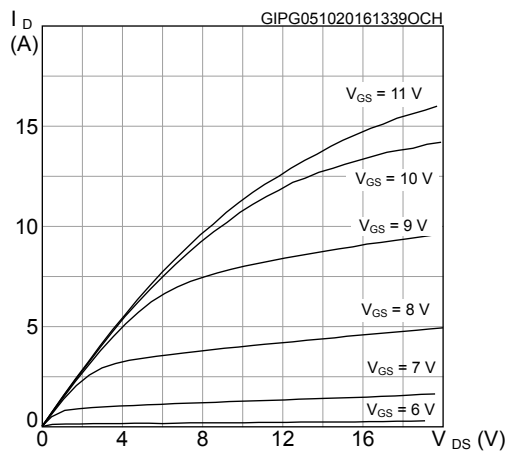
**Figure 1. Safe operating area**



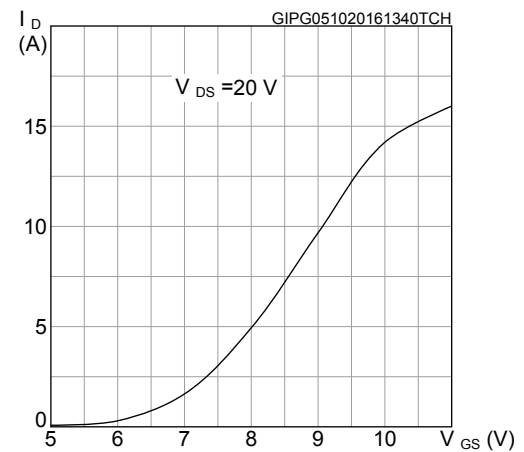
**Figure 2. Thermal impedance**



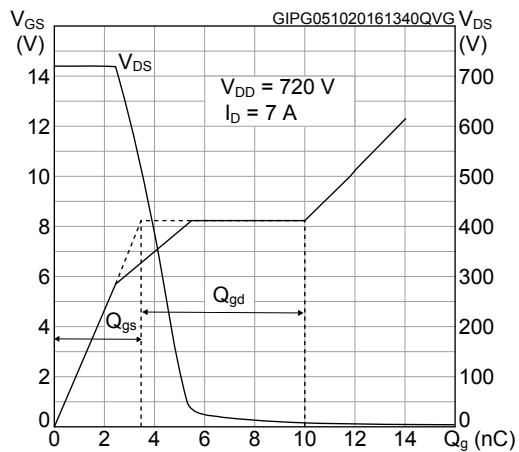
**Figure 3. Output characteristics**



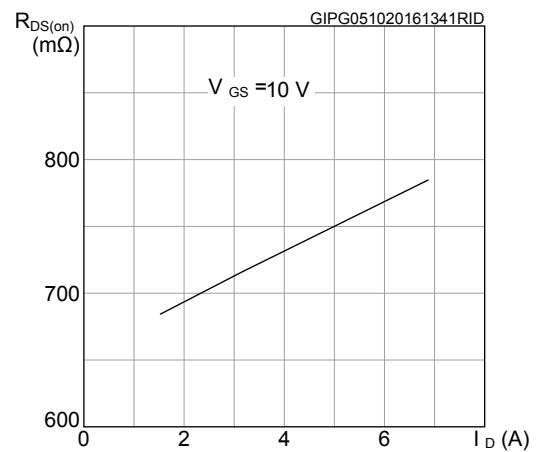
**Figure 4. Transfer characteristics**



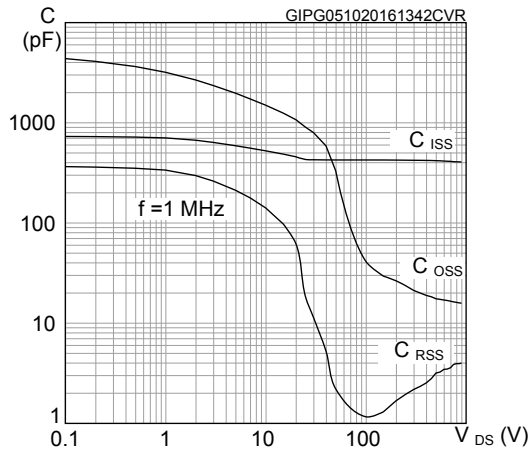
**Figure 5. Gate charge vs gate-source voltage**



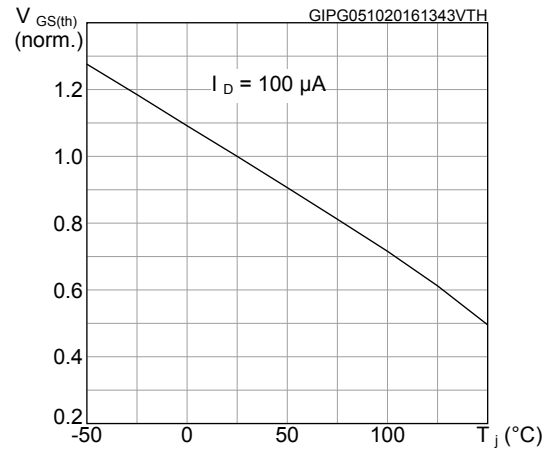
**Figure 6. Static drain-source on-resistance**



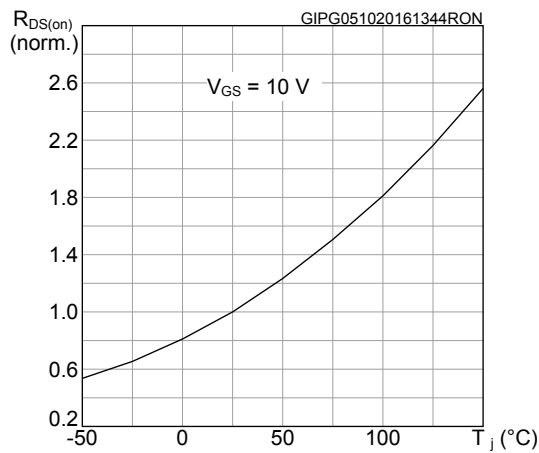
**Figure 7. Capacitance variations**



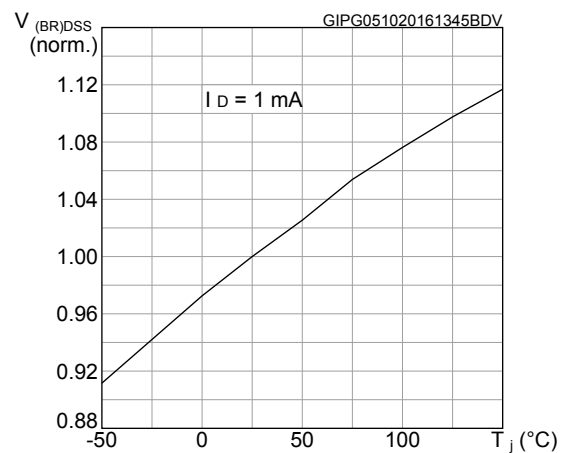
**Figure 8. Normalized gate threshold voltage vs temperature**



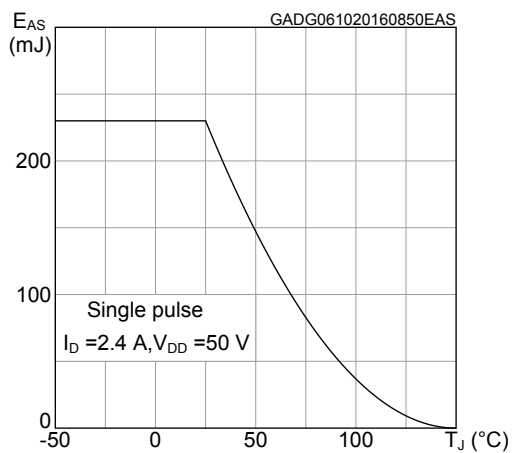
**Figure 9. Normalized on-resistance vs temperature**



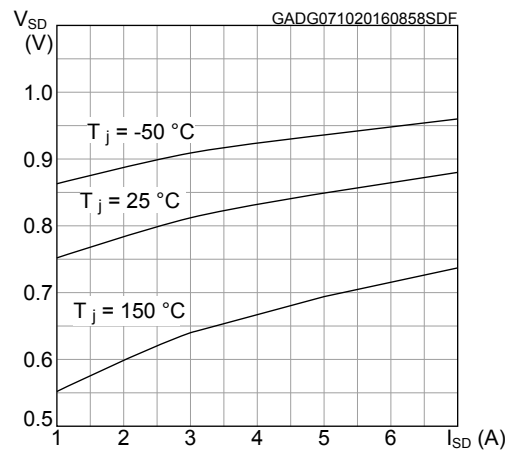
**Figure 10. Normalized V<sub>(BR)DSS</sub> vs temperature**



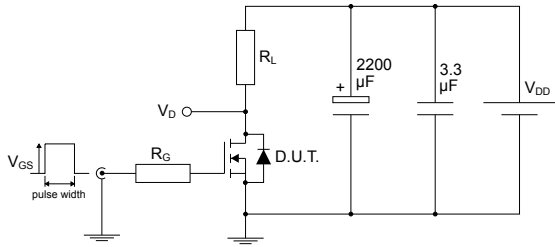
**Figure 11. Maximum avalanche energy vs starting T<sub>J</sub>**



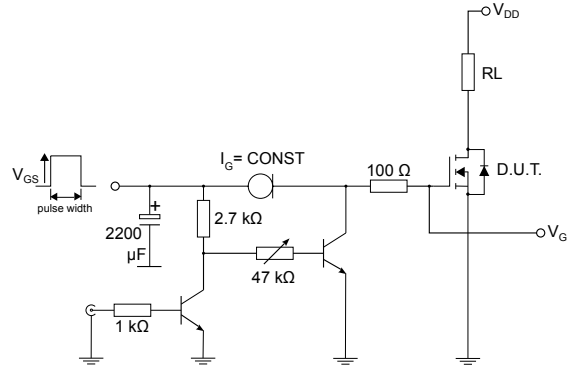
**Figure 12. Source-drain diode forward characteristics**



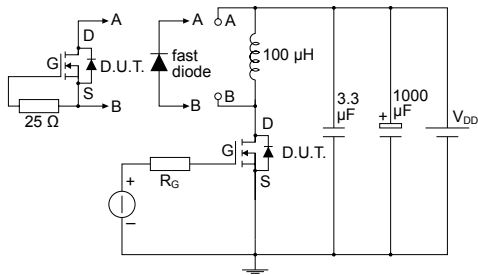
### 3 Test circuits

**Figure 13. Test circuit for resistive load switching times**


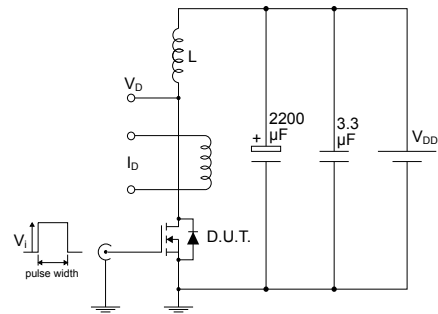
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**Figure 14. Test circuit for gate charge behavior**


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**Figure 15. Test circuit for inductive load switching and diode recovery times**


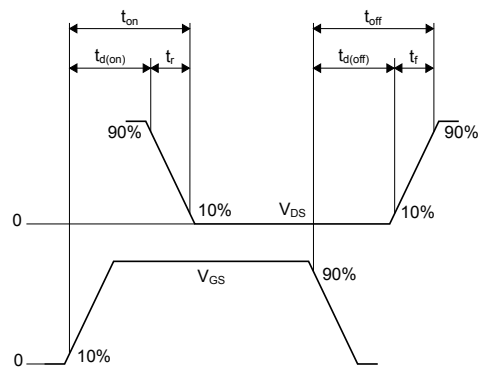
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**Figure 16. Unclamped inductive load test circuit**


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**Figure 17. Unclamped inductive waveform**


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**Figure 18. Switching time waveform**


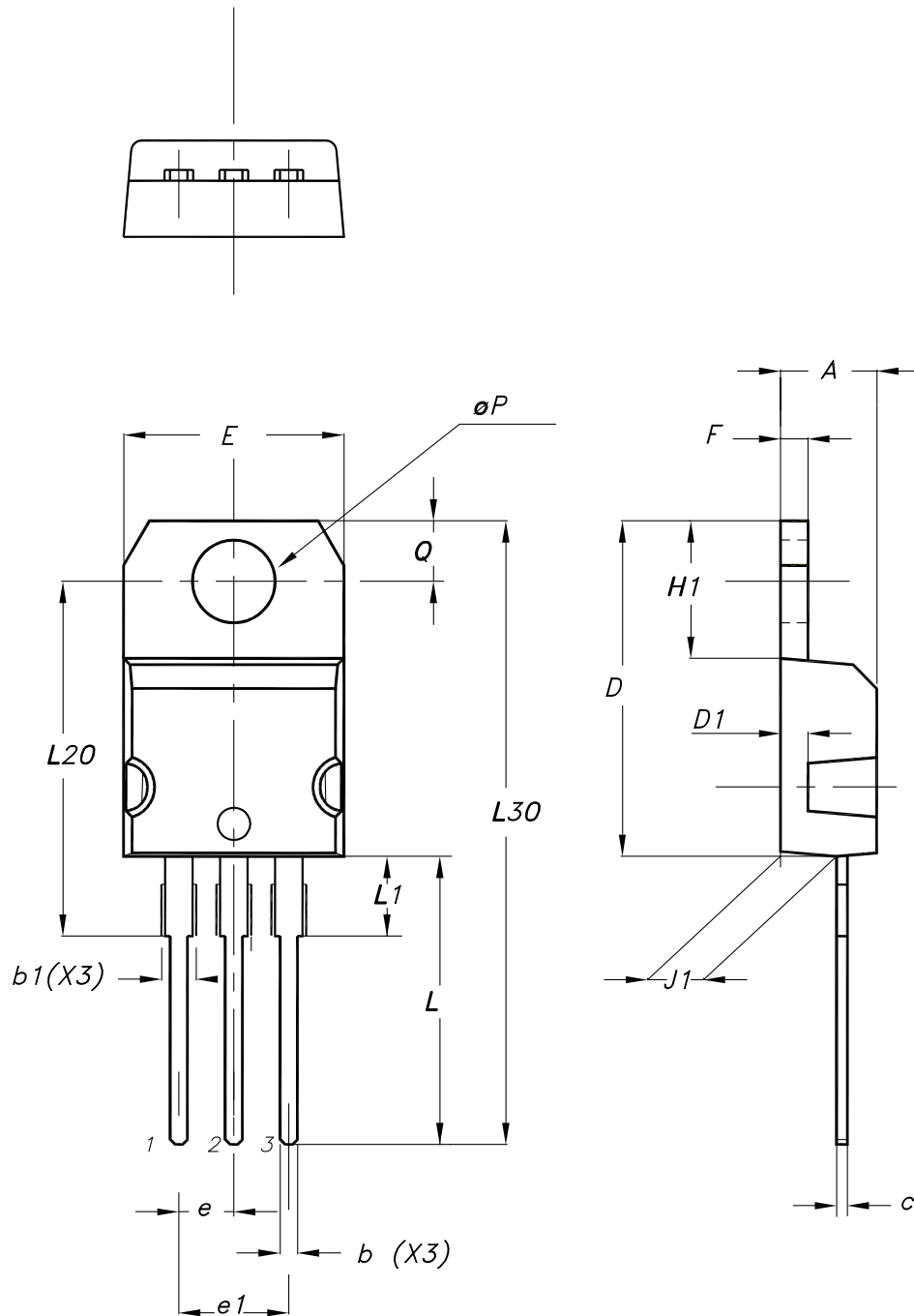
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## 4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 TO-220 type A package information

Figure 19. TO-220 type A package outline



0015988\_typeA\_Rev\_24

**Table 8. TO-220 type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

## Revision history

**Table 9. Document revision history**

Date	Revision	Changes
07-Oct-2016	1	First release.
15-Feb-2018	2	Removed maturity status indication from cover page. The document status is production data. Modified <i>Table 5. Dynamic</i> . Modified <i>Figure 5. Gate charge vs gate-source voltage</i> . Minor text changes.
04-Mar-2026	3	Updated <a href="#">Section 4.1: TO-220 type A package information</a> . Minor text changes.

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