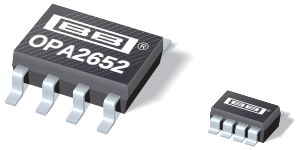
BURR-BROWN®



OPA2652

For most current data sheet and other product information, visit www.burr-brown.com

SpeedPlus™ Dual, 700MHz, Voltage-Feedback OPERATIONAL AMPLIFIER

FEATURES

- WIDEBAND BUFFER: 700MHz, G = +1
- WIDEBAND LINE DRIVER: 200MHz, G = +2
- HIGH OUTPUT CURRENT: 140mA
- LOW SUPPLY CURRENT: 5.5mA/Ch
- ULTRA-SMALL PACKAGE: SOT23-8
- LOW dG/dϕ: 0.05%/0.03°
- HIGH SLEW RATE: 335V/μsec
- SUPPLY VOLTAGE: ±3V to ±6V

APPLICATIONS

- A/D DRIVERS
- CONSUMER VIDEO
- ACTIVE FILTERS
- PULSE DELAY CIRCUITS
- LOW COST UPGRADE TO THE AD8056 OR EL2210

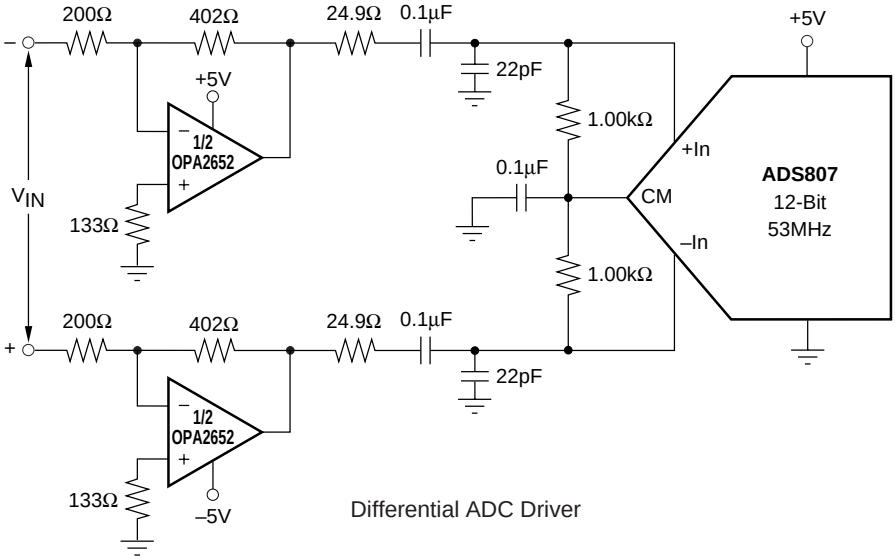
DESCRIPTION

The OPA2652 is a dual, low-cost, wideband voltage-feedback amplifier intended for price sensitive applications. It features a high gain bandwidth product of 200MHz on only 5.5mA/chan quiescent current. Intended for operation on ±5V supplies, it will also support applications on a single supply from +6V to +12V with 140mA output current. Its classical differential input, voltage-feedback design allows wide application in active filters, integrators, transimpedance amplifiers, and differential receivers.

The OPA2652 is internally compensated for unity gain stability. It has exceptional bandwidth (700MHz) as a unity gain buffer, with little peaking (0dB typically). Excellent DC accuracy is achieved with a low 1.5mV input offset voltage and 300nA input offset current.

RELATED PRODUCTS

SINGLES	DUALS	TRIPLES	QUADS	NOTES
OPA650	OPA2650	—	OPA4650	±5V Spec
OPA680	OPA2680	OPA3680	—	+5V Capable
OPA631	OPA2631	—	—	+3V Capable
OPA634	OPA2634	—	—	+3V Capable



Differential ADC Driver

International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111
Twx: 910-952-1111 • Internet: http://www.burr-brown.com/ • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1588B
Printed in U.S.A. June, 2000
SBOS125

SPECIFICATIONS: $V_S = \pm 5V$

At T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted. See Figures 1 and 2 for AC performance only.

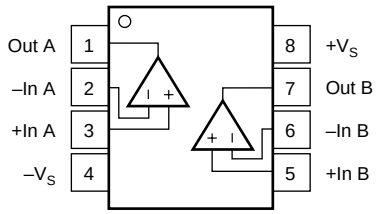
PARAMETER	CONDITIONS	OPA2652U, E				UNITS	MIN/ MAX	TEST LEVEL[1]
		TYP	GUARANTEED					
		+25°C	+25°C[2]	0°C to 70°C[3]	–40°C to +85°C[3]			
AC PERFORMANCE	(Figures 1 and 2)							
Small-Signal Bandwidth	G = +1, R_F = 25Ω, V_O = 200mVp-p	700				MHz	typ	C
	G = +2, V_O = 200mVp-p	200				MHz	typ	C
	G = +5, V_O = 200mVp-p	45				MHz	typ	C
Gain Bandwidth Product	G ≥ +10	200				MHz	typ	C
Bandwidth for 0.1dB Flatness	V_O = 200mVp-p	50				MHz	typ	C
Peaking at a Gain of +1	G = +1, R_F = 25Ω,V_O = 200mVp-p	0				dB	typ	C
Slew Rate	4V Step	335				V/µs	typ	C
Rise/Fall Time	200mV Step	2.0				ns	typ	C
	4V Step	10				ns	typ	C
Large Signal Bandwidth	V_O = 4Vp-p	50				MHz	typ	C
SFDR	V_O = 2Vp-p, 5MHz	66				dB	typ	C
Input Voltage Noise	f > 1MHz	8				nV/√Hz	typ	C
Input Current Noise	f > 1MHz	1.4				pA/√Hz	typ	C
Differential Gain Error	NTSC, R_L = 150Ω	0.05				%	typ	C
Differential Phase Error	NTSC, R_L = 150Ω	0.03				degrees	typ	C
Channel-to-Channel Crosstalk	f = 5MHz	–100				dBc	typ	C
DC PERFORMANCE[4]	V_{CM} = 0V							
Open-Loop Voltage Gain		63	56	55	54	dB	min	A
Input Offset Voltage		±1.5	±7			mV	max	A
Average Offset Drift				5	7	µV/°C	max	B
Input Bias Current		4	15	20	25	µA	max	A
Input Bias Current Drift						µA/°C	max	B
Input Offset Current		±0.3	±1.0	±1.4	±2.0	µA	max	A
Input Offset Current Drift						µA/°C	max	B
INPUT[4]								
Common-Mode Input Range		±4.0	±3.0	±2.8	±2.7	V	min	A
Common-Mode Rejection Ratio		95	75			dB	min	A
Input Impedance	V_{CM} = 0V							
Differential		35 || 1				kΩ || pF	typ	C
Common Mode		18 || 1				MΩ || pF	typ	C
OUTPUT								
Voltage Output Swing	1kΩ Load	±3.0	±2.4			V	min	A
	100Ω Load	±2.5	±2.2			V	min	A
Output Current, Sourcing	V_O = 0V	140	100	85	75	mA	min	A
Output Current, Sinking	V_O = 0V	140	100	85	75	mA	min	A
Closed-Loop Output Impedance	f < 100kHz	0.06				Ω	typ	C
POWER SUPPLY								
Specified Operating Voltage		±5				V	typ	C
Maximum Operating Voltage			±6	±6	±6	V	max	A
Maximum Quiescent Current	Total Both Channels	11	13.2	14	15.5	mA	max	A
Minimum Quiescent Current	Total Both Channels	11	8.8	8	7.5	mA	min	A
Power Supply Rejection Ratio (–PSRR)	Input Referred	58	54			dB	min	A
THERMAL CHARACTERISTICS								
Specified Operating Temperature Range	U, E Package	–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}	Junction-to-Ambient							
U SO-8		125				°C/W	typ	C
E SOT23-8		150				°C/W	typ	C

NOTES: (1) Test Levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information. (2) Junction temperature = ambient for 25°C guaranteed specifications. (3) Junction temperature = ambient at low temperature limit: junction temperature = ambient +23°C at high temperature limit for over temperature guaranteed specifications. (4) Current is considered positive-out-of node. V_{CM} is the input common-mode voltage.

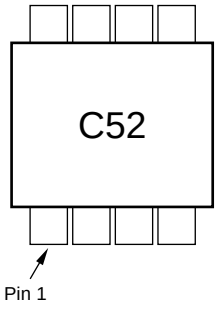
PIN CONFIGURATION

Top View **SO-8**
SOT23-8

OPA2652



SOT23-8 Marking / Pin Orientation



ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±6.5V
Internal Power Dissipation	See Thermal Characteristics
Differential Input Voltage	±1.2V
Input Voltage Range	±V_S
Storage Temperature Range	–40°C to +125°C
Lead Temperature (SO-8)	+260°C
Junction Temperature (T_J)	+175°C
ESD Rating (Human Body Model)	2000V
(Machine Model)	200V

PACKAGE/ORDERING INFORMATION

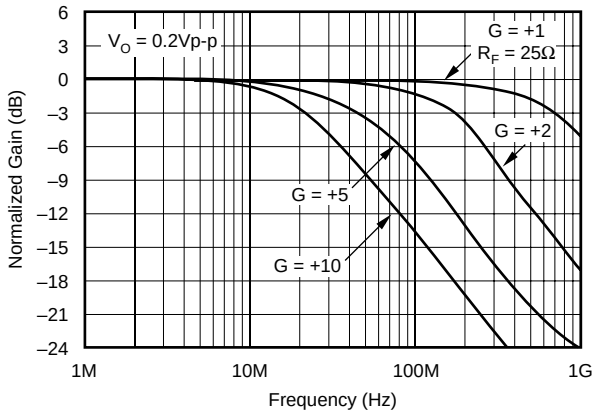
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER(1)	TRANSPORT MEDIA
OPA2652U	SO-8 Surface Mount	182	–40°C to +85°C	OPA2652U	OPA2652U	Rails
"	"	"	"	"	OPA2652U/2K5	Tape and Reel
OPA2652E	SOT23-8 Surface Mount	348	–40°C to +85°C	C52	OPA2652E/250	Tape and Reel
"	"	"	"	"	OPA2652E/3K	Tape and Reel

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /3K indicates 3000 devices per reel). Ordering 3000 pieces of "OPA2652U/3K" will get a single 3000-piece Tape and Reel.

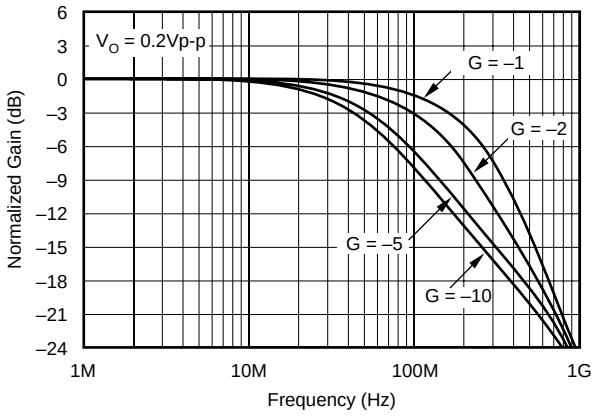
TYPICAL PERFORMANCE CURVES: $V_S = \pm 5V$

At T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted. See Figures 1 and 2.

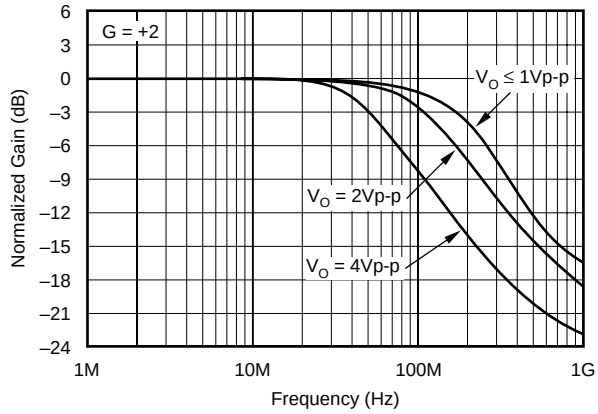
NON-INVERTING
SMALL-SIGNAL FREQUENCY RESPONSE



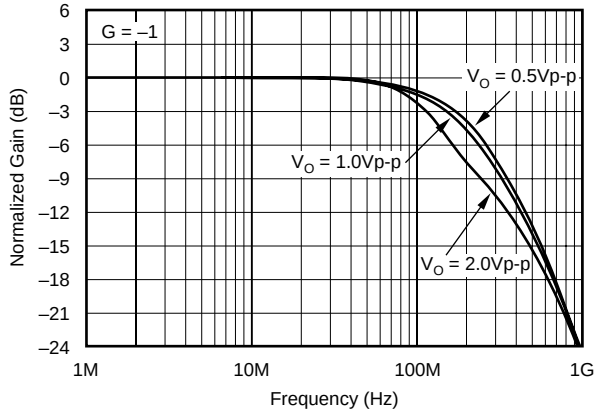
INVERTING
SMALL-SIGNAL FREQUENCY RESPONSE



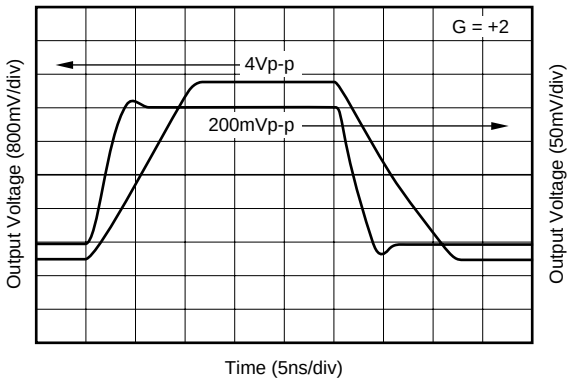
NON-INVERTING
LARGE-SIGNAL FREQUENCY RESPONSE



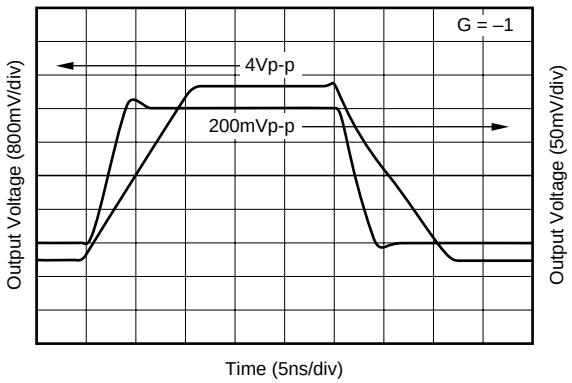
INVERTING
LARGE-SIGNAL FREQUENCY RESPONSE



NON-INVERTING PULSE RESPONSE



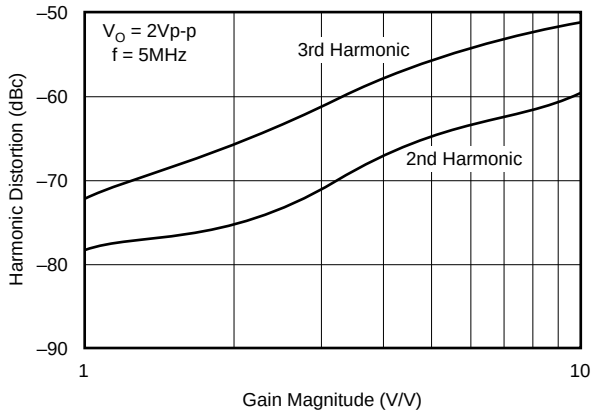
INVERTING PULSE RESPONSE



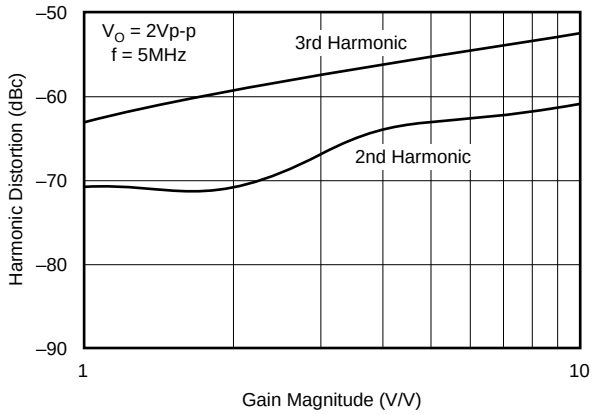
TYPICAL PERFORMANCE CURVES: $V_S = \pm 5V$ (Cont.)

At T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted. See Figures 1 and 2.

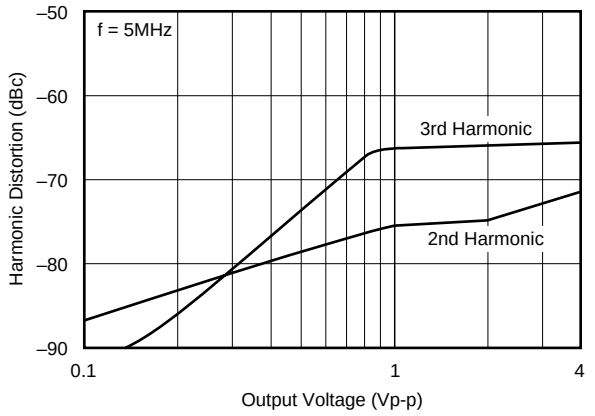
HARMONIC DISTORTION vs NON-INVERTING GAIN



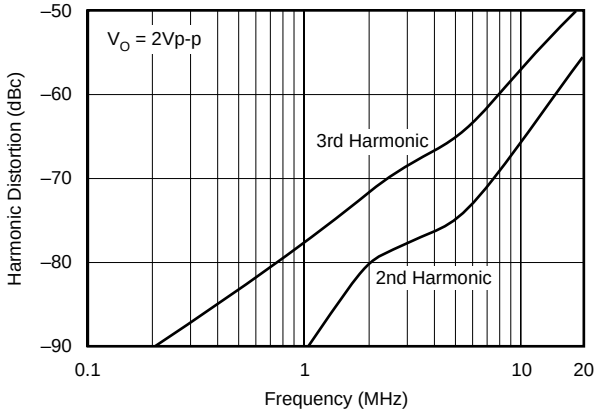
HARMONIC DISTORTION vs INVERTING GAIN



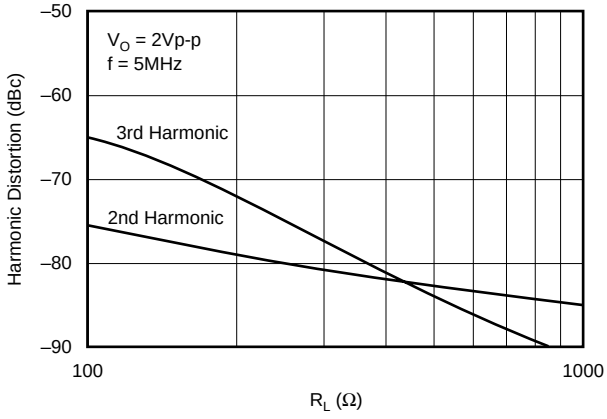
HARMONIC DISTORTION vs OUTPUT VOLTAGE



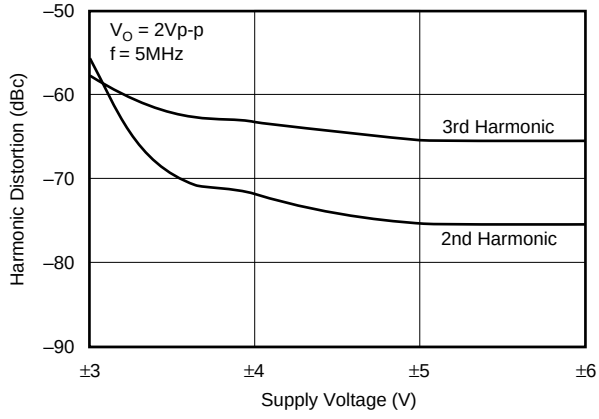
HARMONIC DISTORTION vs FREQUENCY



HARMONIC DISTORTION vs LOAD RESISTANCE



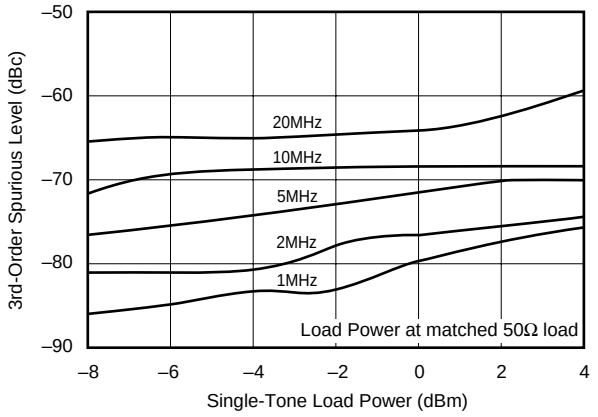
HARMONIC DISTORTION vs SUPPLY VOLTAGE



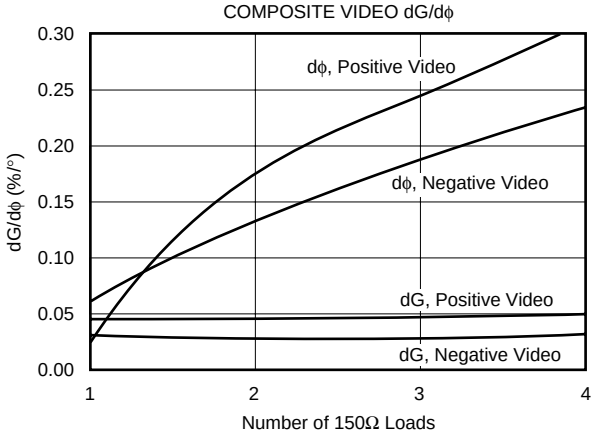
TYPICAL PERFORMANCE CURVES: $V_S = \pm 5V$ (Cont.)

At T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted. See Figures 1 and 2.

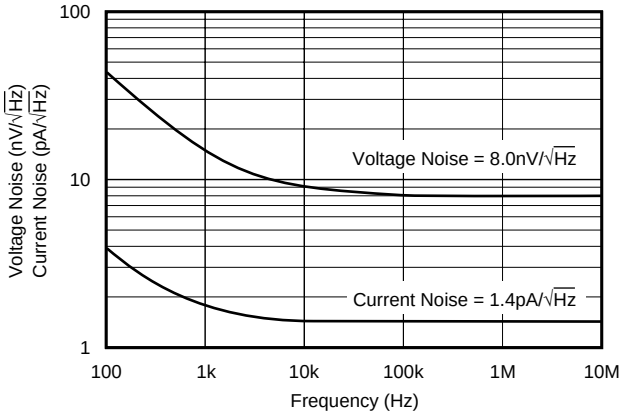
TWO-TONE, 3rd-ORDER SPURIOUS LEVEL



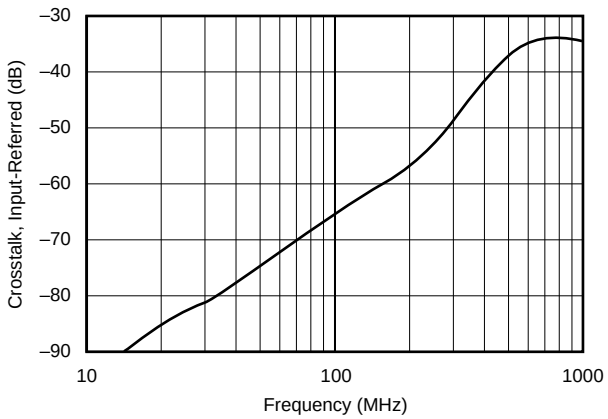
COMPOSITE VIDEO dG/dϕ



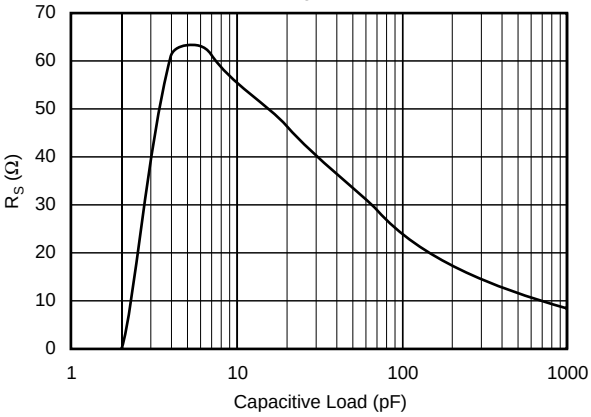
INPUT VOLTAGE AND CURRENT NOISE DENSITY



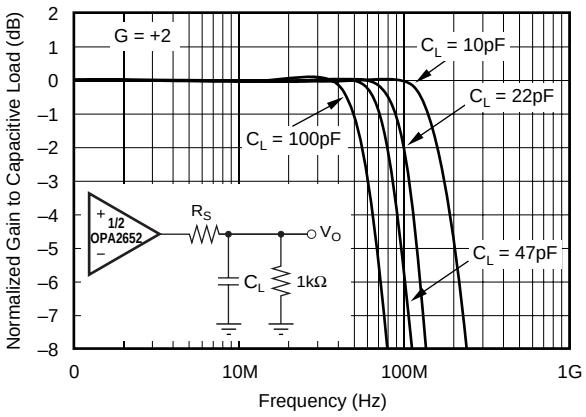
CHANNEL-TO-CHANNEL CROSSTALK



RECOMMENDED R_S vs CAPACITIVE LOAD



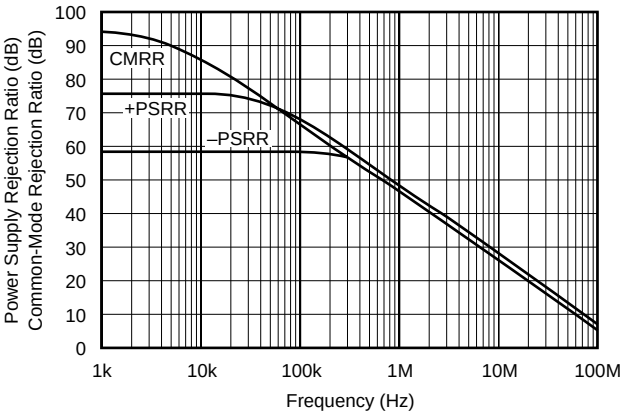
FREQUENCY RESPONSE vs CAPACITIVE LOAD



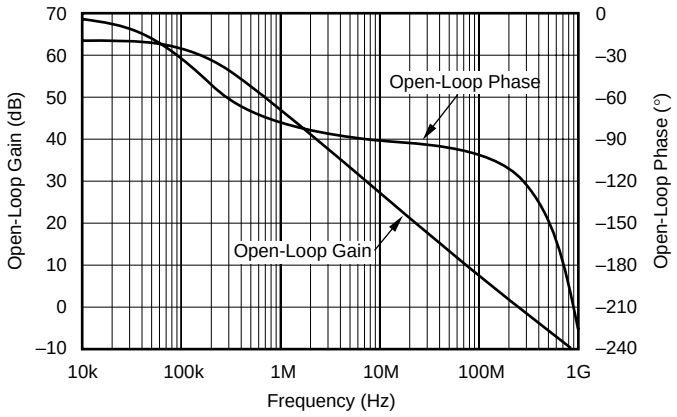
TYPICAL PERFORMANCE CURVES: $V_S = \pm 5V$ (Cont.)

At T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted. See Figures 1 and 2.

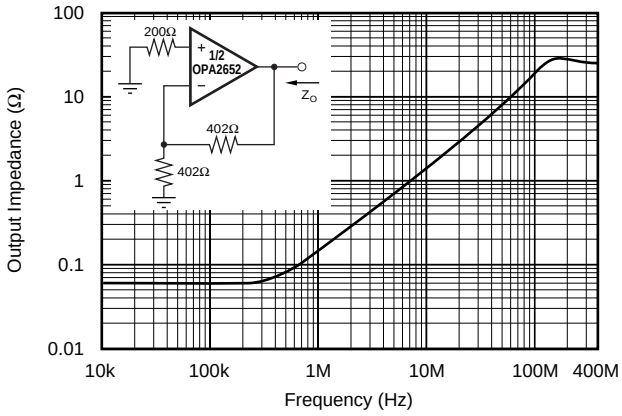
CMRR AND PSRR vs FREQUENCY



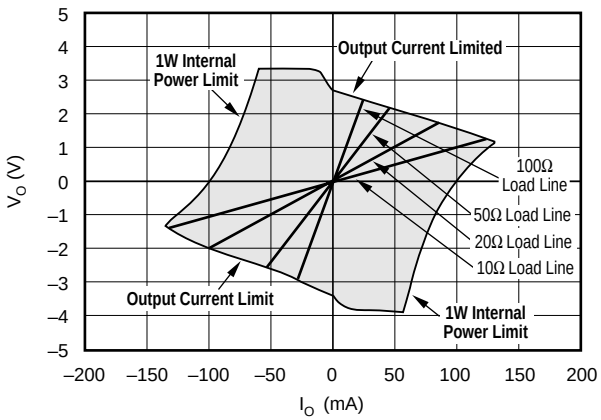
OPEN-LOOP GAIN AND PHASE



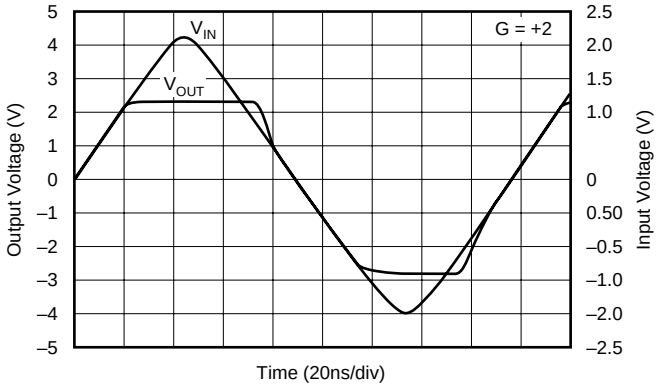
CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY



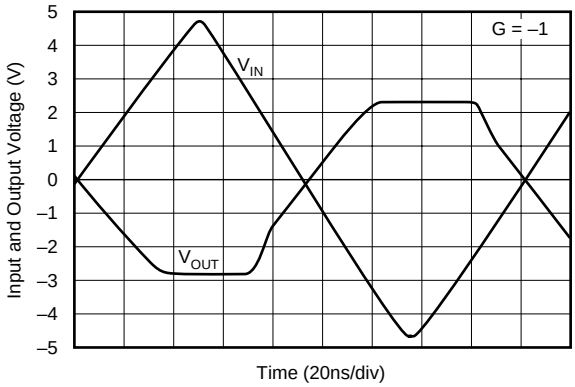
OUTPUT VOLTAGE AND CURRENT LIMITATIONS



NON-INVERTING OVERDRIVE RECOVERY



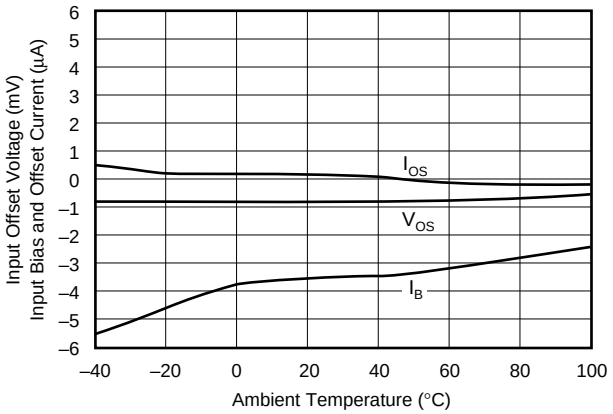
INVERTING OVERDRIVE RECOVERY



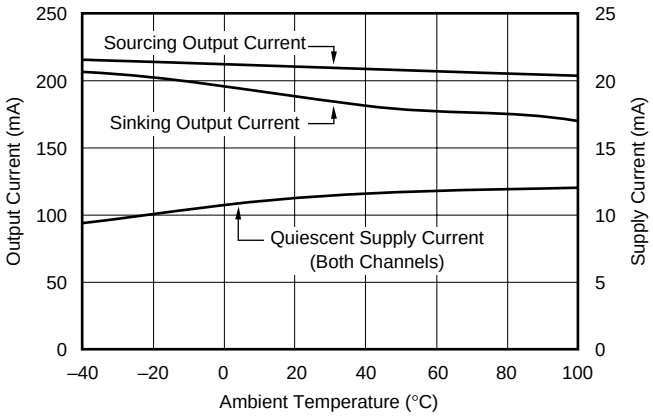
TYPICAL PERFORMANCE CURVES: $V_S = \pm 5V$ (Cont.)

At T_A = +25°C, G = +2, R_F = 402Ω, and R_L = 100Ω, unless otherwise noted. See Figures 1 and 2.

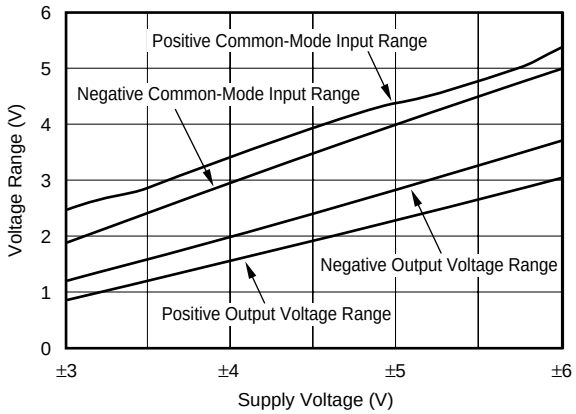
TYPICAL DC DRIFT OVER TEMPERATURE



SUPPLY AND OUTPUT CURRENT vs TEMPERATURE



COMMON-MODE INPUT VOLTAGE RANGE
AND OUTPUT SWING vs SUPPLY VOLTAGE



APPLICATIONS INFORMATION

WIDEBAND VOLTAGE FEEDBACK OPERATION

The OPA2652 is a dual low power, wideband voltage feedback operational amplifier. Each channel is internally compensated to provide unity gain stability. The OPA2652's voltage feedback architecture features true differential and fully symmetrical inputs. This minimizes offset errors, making the OPA2652 well suited for implementing filter and instrumentation designs. As a dual operational amplifier, OPA2652 is an ideal choice for designs requiring multiple channels where reduction of board space, power dissipation and cost are critical. Its AC performance is optimized to provide a gain bandwidth product of 200MHz and a fast rise time of 2.0ns, which is an important consideration in high speed data conversion applications. The low DC input offset of ±1.5mV and drift of ±5µV/°C support high accuracy requirements. In applications requiring a higher slew rate and wider bandwidth, such as video and high bit rate digital communications, consider the dual current feedback OPA2658, or OPA2681.

Figure 1 shows the DC-coupled, gain of +2, dual power supply circuit configuration used as the basis of the ±5V Specifications and Typical Performance Curves. This is for one channel. The other channel is connected similarly. For test purposes, the input impedance is set to 50Ω with a resistor to ground and the output impedance is set to 50Ω with a series output resistor. Voltage swings reported in the specifications are taken directly at the input and output pins, while output powers (dBm) are at the matched 50Ω load. For the circuit of Figure 1, the total effective load will be 100Ω || 804Ω. Two optional components are included in Figure 1.

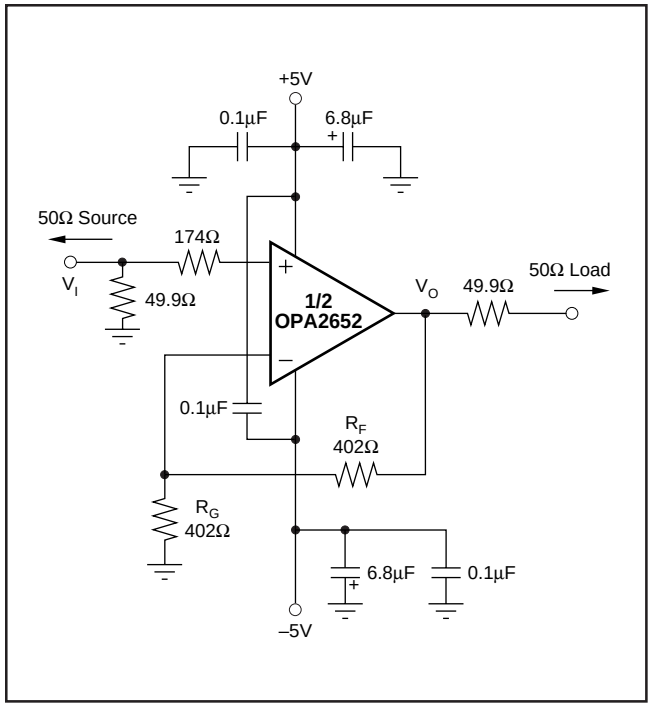


FIGURE 1. DC-Coupled, G = +2, Bipolar Supply, Specification and Test Circuit.

An additional resistor (174Ω) is included in series with the non-inverting input. Combined with the 25Ω DC source resistance looking back towards the signal generator, this gives an input bias current cancelling resistance that matches the 201Ω source resistance seen at the inverting input (see the DC Accuracy and Offset Control section). In addition to the usual power supply decoupling capacitors to ground, a 0.1µF capacitor is included between the two power supply pins. In practical PC board layouts, this optional-added capacitor will typically improve the 2nd harmonic distortion performance by 3dB to 6dB.

Figure 2 shows the DC-coupled gain of –1, bipolar supply circuit configuration which is the basis of the Specifications and Typical Performance Curves at G = –1. The input impedance matching resistor (57.6Ω) used for testing gives a 50Ω input load. A resistor (205Ω) connects the non-inverting input to ground. This provides the DC source resistance matching to cancel outputs errors due to input bias current.

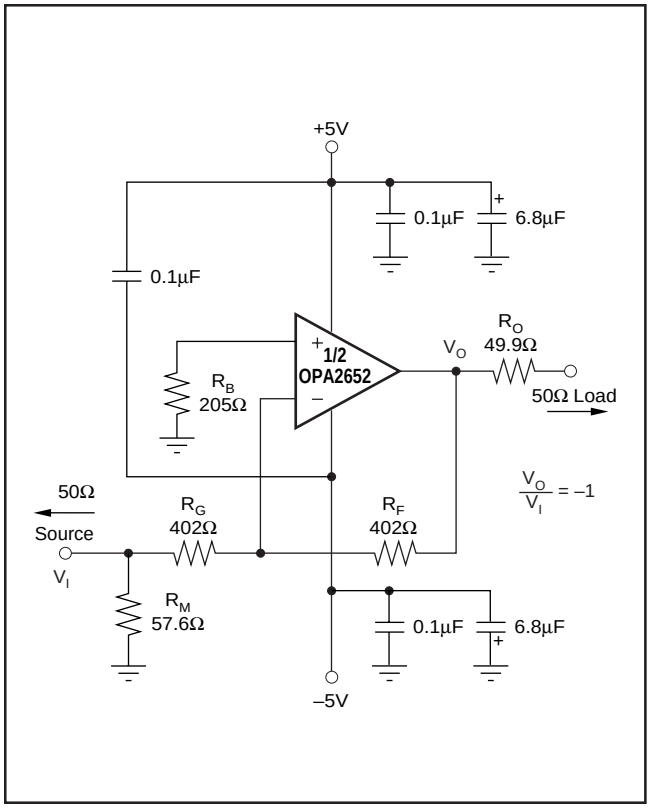


FIGURE 2. DC-Coupled, G = –1, Bipolar Supply, Specification and Test Circuit.

DIFFERENTIAL ADC DRIVER

The circuit on the front page shows an OPA2652 driving the ADS807 A/D converter differentially, at a gain of +2V/V. The outputs are AC-coupled to the converter to adjust for the difference in supply voltages. The 133Ω resistors at the non-inverting inputs minimize DC offset errors. The differential topology minimizes even-order distortion products, such as second-harmonic distortion.

BANDPASS FILTER

Figure 3 shows a single OPA2652 implementing a sixth-order bandpass filter. This filter cascades two second-order Sallen-Key sections with transmission zeros, and a double real pole section. It has 0.3dB of ripple, –3dB frequencies of 450kHz and 11MHz, and –23dB frequencies of 315kHz and 16MHz. The 20.0Ω resistor isolates the first OPA2652 output from capacitive loading. This improves stability with minimal impact on the filter response. Figure 4 shows the nominal response simulated by SPICE.

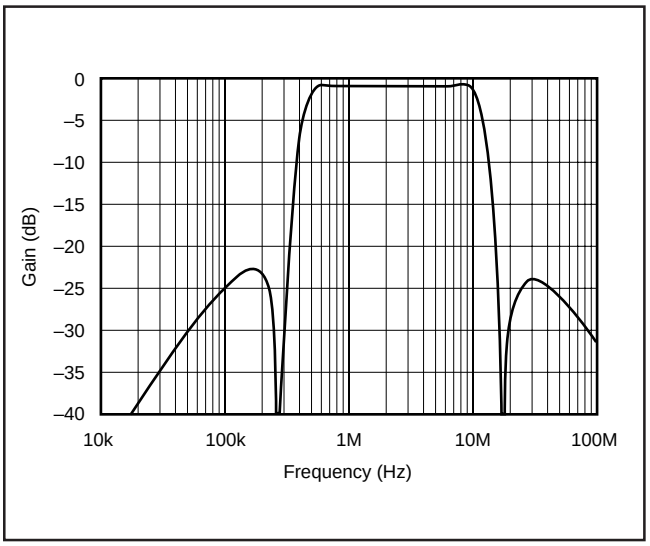


FIGURE 4. Nominal Filter Response.

VIDEO LINE DRIVER

Figure 5 shows the OPA2652 used as a video line driver. Its outstanding differential gain and phase allow it to be used in studio equipment, while its low cost and SOT23-8 package option will support consumer applications.

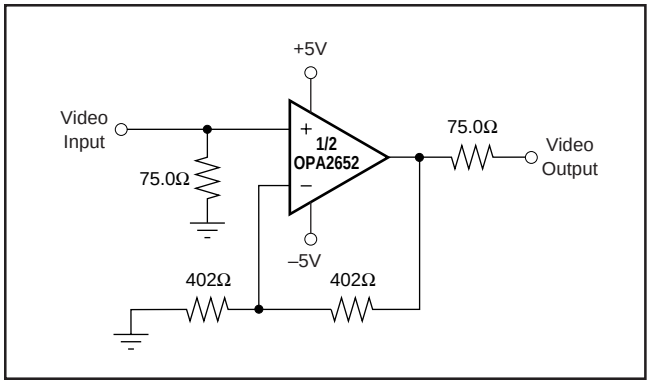


FIGURE 5. Video Line Driver.

PULSE DELAY CIRCUIT

Figure 6 shows the OPA2652 used in a pulse delay circuit. This circuit cascades the two op amps in the OPA2652, each forming a single pole, active allpass filter. The overall gain is +1, and the overall delay through the filter is:

$$t_{GD} = n(2RC), \text{ overall group delay}$$

n= 2, the number of cascaded stages

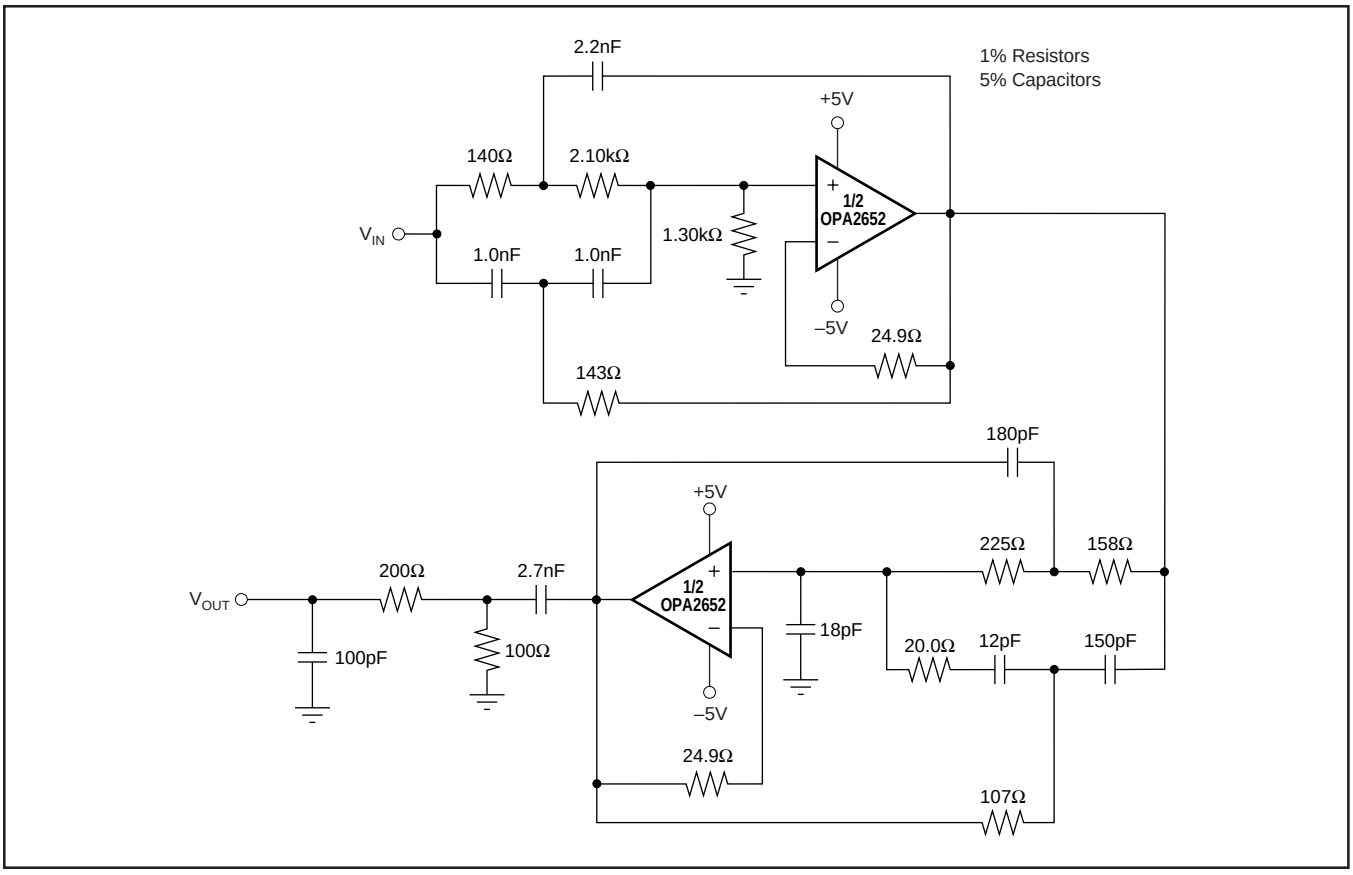


FIGURE 3. Bandpass Filter.

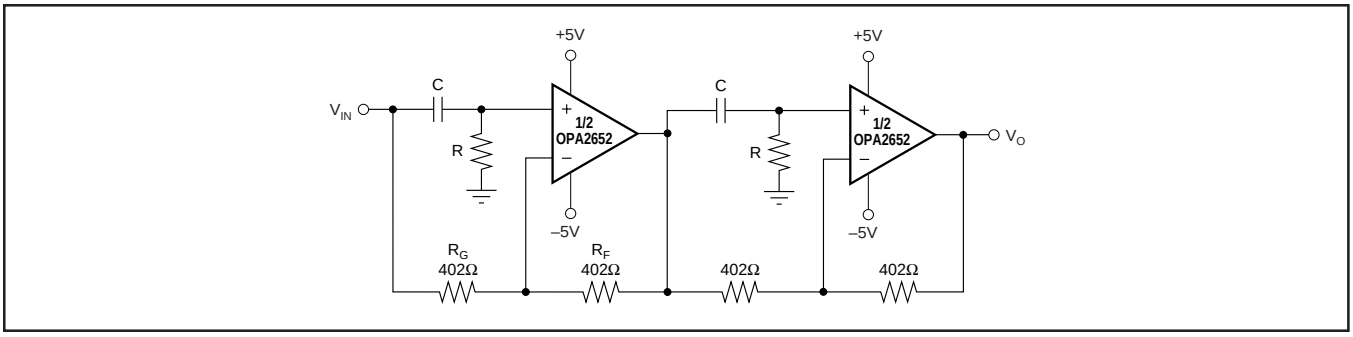


FIGURE 6. Pulse Delay Circuit.

R_F and R_G need to be equal to maintain a constant gain magnitude. The rise and fall times of the input pulses ($t_{r(IN)}$) should be slow enough to prevent pre-shoot artifacts in the response.

$$t_{r(IN)} \geq 5RC, \text{ minimal pre-shoot}$$

SIMPLE BANDPASS FILTER

Figure 7 shows the OPA2652 used as simple bandpass filter. The OPA2652 is well suited for this type of circuit because it is very stable at a noise gain of +1.

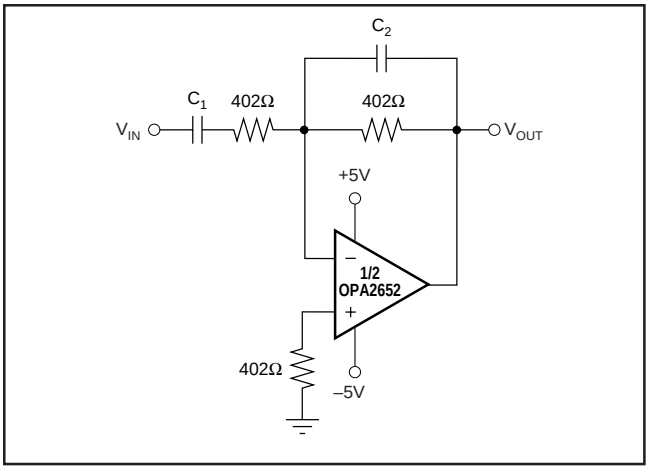


FIGURE 7. Inverting Bandpass Filter.

DESIGN-IN TOOLS

DEMONSTRATION BOARDS

PC boards are available to assist in the initial evaluation of circuit performance using the OPA2652. They are available free as unpopulated PC boards delivered with descriptive documentation. The summary information for these boards is shown below:

PRODUCT	PACKAGE	BOARD PART NUMBER	ORDERING NUMBER
OPA2652U	8-Lead SO-8	DEM-OPA26xU	MKT-352
OPA2652E	SOT23-8	DEM-OPA2652E	MKT-365

Contact the Burr-Brown Applications support line to request this board.

MACROMODELS AND APPLICATIONS SUPPORT

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. Check the Burr-Brown web site (www.burr-brown.com) for available SPICE products (not all parts have models). These models do a good job of predicting small-signal AC and transient performance under a wide variety of operating conditions. They do not do as well in predicting the harmonic distortion or dG/dϕ characteristics. These models do not attempt to distinguish between the package types in their small-signal AC performance.

OPERATING SUGGESTIONS

OPTIMIZING RESISTOR VALUES

Since the OPA2652 is a unity gain stable voltage feedback op amp, a wide range of resistor values may be used for the feedback and gain setting resistors. The primary limits on these values are set by dynamic range (noise and distortion) and parasitic capacitance considerations. For a non-inverting unity gain follower application, the feedback connection should be made with a 25Ω resistor, not a direct short. This will isolate the inverting input capacitance from the output pin and improve the frequency response flatness. Usually, the feedback resistor value should be between 200Ω and 1.5kΩ. Below 200Ω, the feedback network will present additional output loading which can degrade the harmonic distortion performance of the OPA2652. Above 1.5kΩ, the typical parasitic capacitance (approximately 0.2pF) across the feedback resistor may cause unintentional band-limiting in the amplifier response.

A good rule of thumb is to target the parallel combination of R_F and R_G (Figure 1) to be less than approximately 300Ω. The combined impedance $R_F \parallel R_G$ interacts with the inverting input capacitance, placing an additional pole in the feedback network, and thus a zero in the forward response. Assuming a 2pF total parasitic on the inverting node, holding $R_F \parallel R_G < 300\Omega$ will keep this pole above 250MHz. By itself, this constraint implies that the feedback resistor R_F can increase to several kΩ at high gains. This is acceptable as long as the pole formed by R_F and any parasitic capacitance appearing in parallel is kept out of the frequency range of interest.

BANDWIDTH VS GAIN: NON-INVERTING OPERATION

Voltage feedback op amps exhibit decreasing closed-loop bandwidth as the signal gain is increased. In theory, this relationship is described by the Gain Bandwidth Product (GBP) shown in the specifications. Ideally, dividing GBP by the non-inverting signal gain (also called the Noise Gain, or NG) will predict the closed-loop bandwidth. In practice, this only holds true when the phase margin approaches 90°, as it does in high gain configurations. At low gains (increased feedback factor), most amplifiers will exhibit a wider bandwidth and lower phase margin. The OPA2652 is compensated to give a flat response in a non-inverting gain of 1 (Figure 1). This results in a typical gain of +1 bandwidth of 700MHz, far exceeding that predicted by dividing the 200MHz GBP by NG = 1. Increasing the gain will cause the phase margin to approach 90° and the bandwidth to more closely approach the predicted value of (GBP/NG). At a gain of +5, the 45MHz bandwidth shown in the Typical Specifications is close to that predicted using this simple formula.

INVERTING AMPLIFIER OPERATION

Since the OPA2652 is a general purpose, wideband voltage feedback op amp, all of the familiar op amp application circuits are available to the designer. Inverting operation is one of the more common requirements and offers several performance benefits. Figure 2 shows a typical inverting configuration.

In the inverting configuration, three key design consideration must be noted. The first is that the gain resistor (R_G) becomes part of the signal channel input impedance. If input impedance matching is desired (which is beneficial whenever the signal is coupled through a cable, twisted pair, long PC board trace or other transmission line conductor), R_G may be set equal to the required termination value and R_F adjusted to give the desired gain. This is the simplest approach and results in optimum bandwidth and noise performance. However, at low inverting gains, the resultant feedback resistor value can present a significant load to the amplifier output. For an inverting gain of –1, setting R_G to 50Ω for input matching eliminates the need for R_M but requires a 50Ω feedback resistor. This has the interesting advantage that the noise gain becomes equal to 2 for a 50Ω source impedance—the same as the non-inverting circuits considered above. However, the amplifier output will now see the 50Ω feedback resistor in parallel with the external load. In general, the feedback resistor should be limited to the 200Ω to 1.5kΩ range. In this case, it is preferable to increase both the R_F and R_G values as shown in Figure 2, and then achieve the input matching impedance with a third resistor (R_M) to ground. The total input impedance becomes the parallel combination of R_G and R_M.

The second major consideration, touched on in the previous paragraph, is that the signal source impedance becomes part of the noise gain equation and influences the bandwidth. For the example in Figure 2, the R_M value combines in parallel with the external 50Ω source impedance, yielding an effective driving impedance of 50Ω || 57.6Ω = 26.8Ω. This impedance is added in series with R_G for calculating the noise gain (NG). The resultant NG is 1.94 for Figure 2, (an ideal 0Ω source would cause NG = 2.00).

The third important consideration in inverting amplifier design is setting the bias current cancellation resistor on the non-inverting input (R_B). If this resistor is set equal to the total DC resistance looking out of the inverting node, the output DC error, due to the input bias currents, will be reduced to (Input Offset Current) • R_F. If the 50Ω source impedance is DC-coupled in Figure 2, the total resistance to ground on the inverting input will be 429Ω. Combining this in parallel with the feedback resistor gives 208Ω, which is close to the R_B = 205Ω used in Figure 2. To reduce the additional high frequency noise introduced by this resistor, it is sometimes bypassed with a capacitor. As long as R_B <300Ω, the capacitor is not required since its total noise contribution will be much less than that of the op amp's input noise voltage.

OUTPUT CURRENT AND VOLTAGE

The OPA2652 specifications in the spec table, though familiar in the industry, consider voltage and current limits separately. In many applications, it is the voltage • current, or V-I product, which is more relevant to circuit operation. Refer to the "Output Voltage and Current Limitations" plot in the Typical Performance Curves. The X and Y axes of this graph show the zero-voltage output current limit and the zero-current output voltage limit, respectively. The four quadrants give a more detailed view of the OPA2652's output drive capabilities, noting that the graph is bounded by a "Safe Operating Area" of 1W maximum internal power dissipation (500mW for each channel). Superimposing resistor load lines onto the plot shows that the OPA2652 can drive ±2.2V into 50Ω or ±2.5V into 100Ω without exceeding the output capabilities, or the 1W dissipation boundary line.

To maintain maximum output stage linearity, no output short-circuit protection is provided. This will not normally be a problem since most applications include a series matching resistor at the output that will limit the internal power dissipation if the output side of this resistor is shorted to ground. However, shorting the output pin directly to the adjacent positive power supply pin will, in most cases, destroy the amplifier. Including a small series resistor (5Ω) in the power supply line will protect against this. Always place the 0.1µF decoupling capacitor directly on the supply pins.

DRIVING CAPACITIVE LOADS

One of the most demanding and yet very common load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an A/D converter—including additional external capacitance which may be recommended to improve A/D linearity. A high speed amplifier like the OPA2652 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is

placed directly on the output pin. When the amplifier's open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness, pulse response fidelity and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The Typical Performance Curves show the recommended R_S versus capacitive load and the resulting frequency response at the load. Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA2652. Long PC board traces, unmatched cables, and connections to multiple devices can easily exceed this value. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA2652 output pin (see Board Layout Guidelines).

DISTORTION PERFORMANCE

The OPA2652 provides good distortion performance into a 100Ω load on ±5V supplies. Increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network; in the non-inverting configuration (Figure 1) this is sum of R_F + R_G, while in the inverting configuration, it is just R_F. Also, providing an additional supply decoupling capacitor (0.1µF) between the supply pins (for bipolar operation) improves the 2nd-order distortion slightly (3dB to 6dB).

It is also true that increasing the output voltage swing increases harmonic distortion.

NOISE PERFORMANCE

The OPA2652 input-referred voltage noise (8nV/√Hz), and the two input-referred current noise terms (1.4pA/√Hz), combine to give low output noise under a wide variety of operating conditions. Figure 8 shows the op amp noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

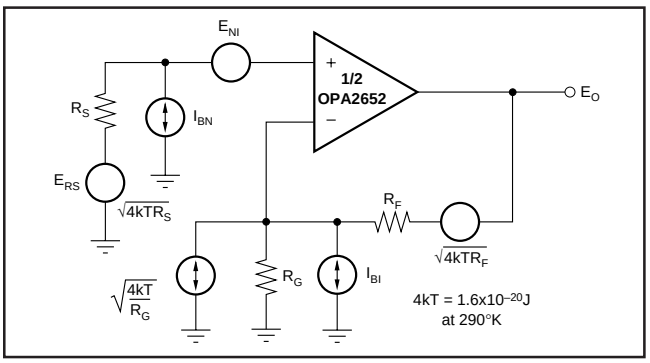


FIGURE 8. Op Amp Noise Analysis Model.

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 1 shows the general form for the output noise voltage using the terms shown in Figure 10.

Equation 1:

$$E_N = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}}$$

Dividing this expression by the noise gain ($NG = 1+R_F/R_G$) will give the equivalent input-referred spot noise voltage at the non-inverting input, as shown in Equation 2.

Equation 2:

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)NG^2 + \left(I_{BI}R_F\right)^2 + 4kTR_FNG}$$

Evaluating these two equations for the OPA2652 circuit and component values shown in Figure 1 will give a total output spot noise voltage of 17nV/√Hz and a total equivalent input spot noise voltage of 8.4nV/√Hz. This is including the noise added by the bias current cancellation resistor (205Ω) on the non-inverting input. This total input-referred spot noise voltage is only slightly higher than the 8nV/√Hz specification for the op amp voltage noise alone. This will be the case as long as the impedances appearing at each op amp input are limited to the previously recommend maximum value of 300Ω. Keeping both ($R_F \parallel R_G$) and the non-inverting input source impedance less than 300Ω will satisfy both noise and frequency response flatness considerations. Since the resistor-induced noise is relatively negligible, additional capacitive decoupling across the bias current cancellation resistor (R_B) for the inverting op amp configuration of Figure 2 is not required.

DC ACCURACY AND OFFSET CONTROL

The balanced input stage of a wideband voltage feedback op amp allows good output DC accuracy in a wide variety of applications. Although the high speed input stage does require relatively high input bias current (typically 4µA out of each input terminal), the close matching between them may be used to significantly reduce the output DC error caused by this current. This is done by matching the DC source resistances appearing at the two inputs. This reduces the output DC error due to the input bias currents to the offset current times the feedback resistor. Evaluating the configuration of Figure 1, using worst-case +25°C input offset voltage and current specifications, gives a worst-case output offset voltage equal to:

$$\pm(NG \bullet V_{OS(MAX)}) \pm (R_F \bullet I_{OS(MAX)})$$
$$= \pm(1.94 \bullet 7.0mV) \pm (402\Omega \bullet 1.0\mu A)$$
$$= \pm 14.0mV$$

(NG = non-inverting signal gain)

A fine scale output offset null, or DC operating point adjustment, is often required. Numerous techniques are available for introducing DC offset control into an op amp

circuit. Most of these techniques add a DC current through the feedback resistor. In selecting an offset trim method, one key consideration is the impact on the desired signal path frequency response. If the signal path is intended to be non-inverting, the offset control is best applied as an inverting summing signal to avoid interaction with the signal source. If the signal path is intended to be inverting, applying the offset control to the non-inverting input may be considered. However, the DC offset voltage on the summing junction will set up a DC current back into the source which must be considered. Applying an offset adjustment to the inverting op amp input can change the noise gain and frequency response flatness. For a DC-coupled inverting amplifier, Figure 9 shows one example of an offset adjustment technique that has minimal impact on the signal frequency response. In this case, the DC offset current is brought into the inverting input node through resistor values that are much larger than the signal path resistors. This will insure that the adjustment circuit has minimal effect on the loop gain and hence the frequency response.

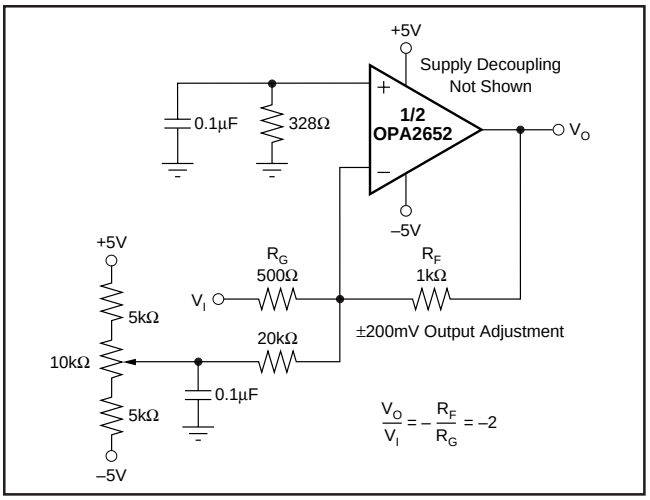


FIGURE 9. DC-Coupled, Inverting Gain of –2, with Offset Adjustment.

THERMAL ANALYSIS

Heatsinking or forced airflow may be required under extreme operating conditions. Maximum desired junction temperature will set the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed 175°C.

Operating junction temperature (T_J) is given by $T_A + P_D \bullet \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} will depend on the required output signal and load but would, for a grounded resistive load, be at a maximum when the output is fixed at a voltage equal to 1/2 of either supply voltage (for equal bipolar supplies). Under this condition, $P_{DL} = V_S^2/(4 \bullet R_L)$ where R_L includes feedback network loading.

Note that it is the power in the output stage, and not into the load, that determines internal power dissipation.

As an example, compute the maximum T_J using an OPA2652E (SOT23-8 package) in the circuit of Figure 1 operating at the maximum specified ambient temperature of +85°C and with both outputs driving $2.5V_{DC}$ into a grounded 100Ω load.

$P_D = 10V \bullet 15.5mA + 2\ [5^2/(4 \bullet (100\Omega \parallel 804\Omega))] = 296mW$

Maximum $T_J = +85°C + (0.30W \bullet 150°C/W) = 130°C$.

This absolute worst-case condition meets the specified maximum junction temperature. Actual P_{DL} will almost always be less than that considered here. Carefully consider maximum T_J in your application.

BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high frequency amplifier like the OPA2652 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

a) **Minimize parasitic capacitance** to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability: on the non-inverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) **Minimize the distance** (<0.25") from the power supply pins to high frequency 0.1µF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power supply connections should always be decoupled with these capacitors. An optional supply decoupling capacitor (0.1µF) across the two power supplies (for bipolar operation) will improve 2nd harmonic distortion performance. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

c) **Careful selection and placement of external components will preserve the high frequency performance of the OPA2652.** Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film or carbon composition axially-leaded resistors can also provide good high frequency performance. Again, keep their leads and PC board traces as short as possible. Never use wirewound type resistors in a high frequency application. Since the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if

any, as close as possible to the output pin. Other network components, such as non-inverting input termination resistors, should also be placed close to the package. Where double-side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal film or surface-mount resistors have approximately 0.2pF in shunt with the resistor. For resistor values >1.5kΩ, this parasitic capacitance can add a pole and/or zero below 500MHz that can effect circuit operation. Keep resistor values as low as possible consistent with load driving considerations. The 402Ω feedback used in the typical performance specifications is a good starting point for design. Note that a 25Ω feedback resistor, rather than a direct short, is suggested for the unity gain follower application. This effectively isolates the inverting input capacitance from the output pin that would otherwise cause additional peaking in the gain of +1 frequency response.

d) **Connections to other wideband devices** on the board may be made with short direct traces or through on-board transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of Recommended R_S vs Capacitive Load. Low parasitic capacitive loads (<5pF) may not need an R_S since the OPA2652 is nominally compensated to operate with a 2pF parasitic load. Higher parasitic capacitive loads without an R_S are allowed as the signal gain increases (increasing the unloaded phase margin) If a long trace is required, and the 6dB signal loss intrinsic to a doubly terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary on board, and in fact, a higher impedance environment will improve distortion as shown in the distortion versus load plots. With a characteristic board trace impedance defined (based on board material and trace dimensions), a matching series resistor into the trace from the output of the OPA2652 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device; this total effective impedance should be set to match the trace impedance. The high output voltage and current capability of the OPA2652 allows multiple destination devices to be handled as separate transmission lines, each with their own series and shunt terminations. If the 6dB attenuation of a doubly terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of Recommended R_S vs Capacitive Load. This will not preserve signal integrity as well as a doubly terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e) **Socketing a high speed part like the OPA2652 is not recommended.** The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA2652 onto the board.

INPUT AND ESD PROTECTION

The OPA2652 is built using a very high speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the "Absolute Maximum Ratings" table. All device pins are protected with internal ESD protection diodes to the power supplies as shown in Figure 10.

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (e.g., in systems with ±15V supply parts driving into the OPA2652), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response.

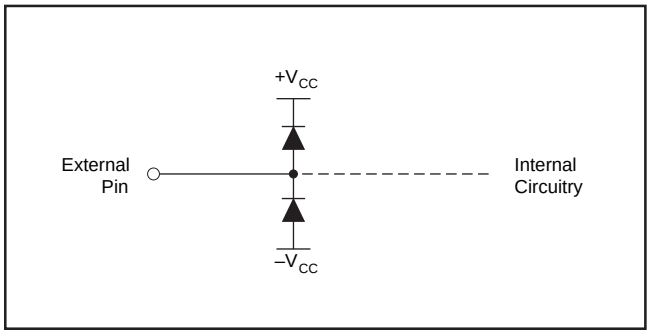


FIGURE 10. Internal ESD Protection.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
OPA2652E/250	ACTIVE	SOT23	DCN	8	250	TBD	CU SNPB	Level-2-235C-1 YEAR
OPA2652E/3K	ACTIVE	SOT23	DCN	8	3000	TBD	CU SNPB	Level-2-235C-1 YEAR
OPA2652U	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU	Level-2-260C-1 YEAR
OPA2652U-1	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2652U-1/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA2652U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU	Level-2-260C-1 YEAR
OPA2652U/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

IMPORTANT NOTICE

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265