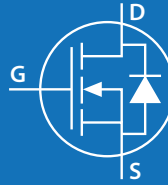


EPC2214 – Automotive 80 V (D-S) Enhancement Mode Power Transistor

 $V_{DS}, 80\text{ V}$
 $R_{DS(on)}, 20\text{ m}\Omega$
 $I_D, 10\text{ A}$

AEC-Q101



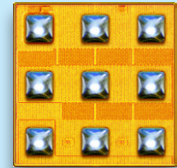
Revised April 25, 2025

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR} . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Application Notes:

- Easy-to-use and reliable gate
- Gate Drive ON = 5-5.25 V typical, OFF = 0 V (negative voltage not needed)
- Top of FET is electrically connected to source

Questions:



Die Size: 1.35 x 1.35 mm

EPC2214 eGaN® FETs are supplied only in passivated die form with solder bumps.

Maximum Ratings			
PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	80	V
I_D	Continuous ($T_A = 25^\circ\text{C}$)	10	A
	Pulsed (25°C , $T_{PULSE} = 10\ \mu\text{s}$)	60	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-55 to 150	$^\circ\text{C}$
T_{STG}	Storage Temperature	-55 to 150	

Thermal Characteristics			
PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2.7	$^\circ\text{C}/\text{W}$
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	7.5	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	81	

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details

Static Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	$V_{GS} = 0\text{ V}$, $I_D = 0.2\text{ mA}$	80			V
I_{DSS}	Drain-Source Leakage	$V_{GS} = 0\text{ V}$, $V_{DS} = 64\text{ V}$		0.003	0.15	mA
I_{GSS}	Gate-to-Source Forward Leakage	$V_{GS} = 5\text{ V}$		0.003	1.1	mA
	Gate-to-Source Forward Leakage [#]	$V_{GS} = 5\text{ V}$, $T_J = 125^\circ\text{C}$		0.01	2.5	mA
	Gate-to-Source Reverse Leakage	$V_{GS} = -4\text{ V}$		0.003	0.15	mA
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 2\text{ mA}$	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	$V_{GS} = 5\text{ V}$, $I_D = 6\text{ A}$		15	20	m Ω
V_{SD}	Source-Drain Forward Voltage [#]	$V_{GS} = 0\text{ V}$, $I_S = 0.5\text{ A}$		1.9		V

[#] Defined by design. Not subject to production test.

All measurements were done with substrate connected to source.

Applications

- Lidar/pulsed power applications
- DC-DC conversion
- Wireless power transfer

Benefits

- Ultra high efficiency
- Ultra low $R_{DS(on)}$
- Ultra low Q_G
- Ultra small footprint

Scan QR code or click link below for more information including reliability reports, device models, demo boards!



<https://l.ead.me/EPC2214>

Dynamic Characteristics* (T_J = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C _{ISS}	Input Capacitance	V _{GS} = 0 V, V _{DS} = 40 V		198	238	pF
C _{RSS}	Reverse Transfer Capacitance			1.8		
C _{OSS}	Output Capacitance			129	194	
C _{OSS(ER)}	Effective Output Capacitance, Energy Related (Note 2)	V _{GS} = 0 V, V _{DS} = 0 to 40 V		171		pF
C _{OSS(TR)}	Effective Output Capacitance, Time Related (Note 3)			211		
R _G	Gate Resistance			0.65		Ω
Q _G	Total Gate Charge	V _{GS} = 5 V, V _{DS} = 40 V, I _D = 6 A		1.8	2.2	nC
Q _{GS}	Gate to Source Charge	V _{DS} = 40 V, I _D = 6 A		0.5		
Q _{GD}	Gate to Drain Charge			0.3		
Q _{G(TH)}	Gate Charge at Threshold			0.4		
Q _{OSS}	Output Charge	V _{GS} = 0 V, V _{DS} = 40 V		8	12	
Q _{RR}	Source-Drain Recovery Charge			0		

Defined by design. Not subject to production test.
 All measurements were done with substrate connected to source.
 Note 2: C_{OSS(ER)} is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.
 Note 3: C_{OSS(TR)} is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Figure 1: Typical Output Characteristics at 25°C

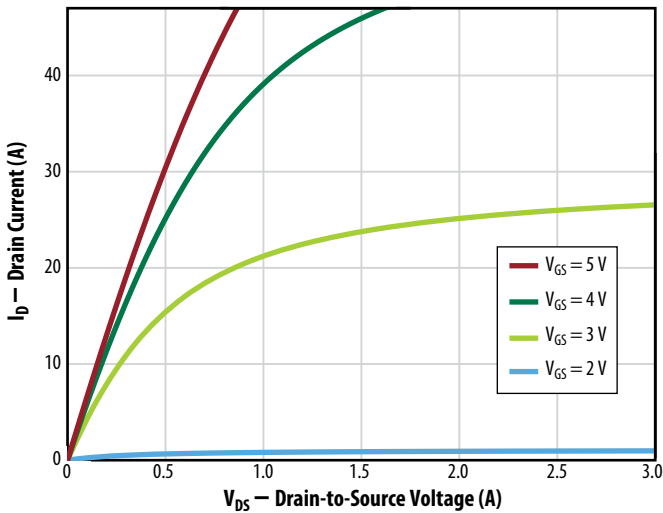


Figure 2: Typical Transfer Characteristics

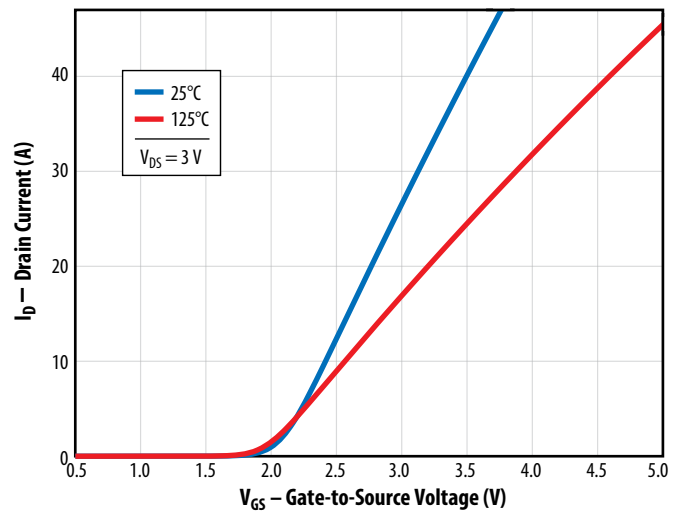


Figure 3: Typical R_{DS(on)} vs. V_{GS} for Various Drain Currents

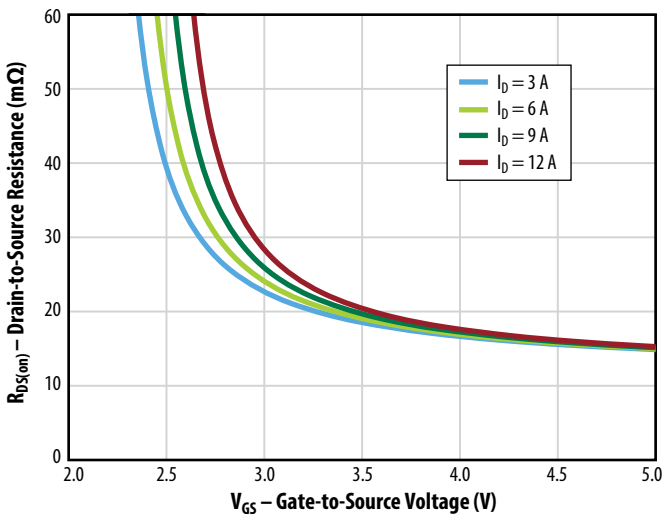


Figure 4: Typical R_{DS(on)} vs. V_{GS} for Various Temperatures

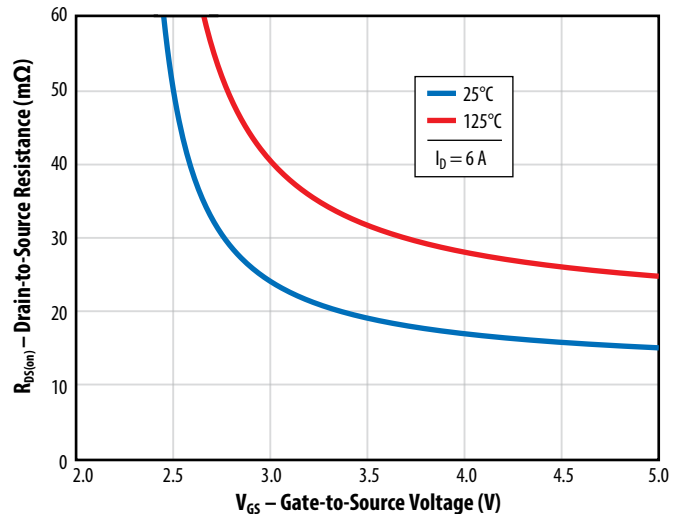


Figure 5a: Typical Capacitance (Linear Scale)

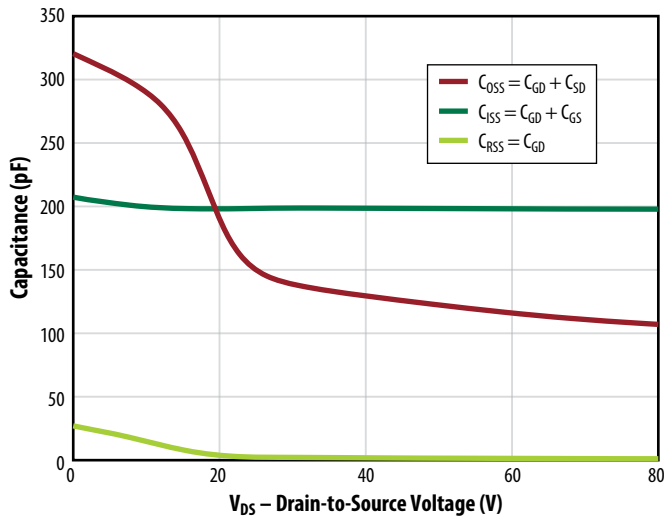


Figure 5b: Typical Capacitance (Log Scale)

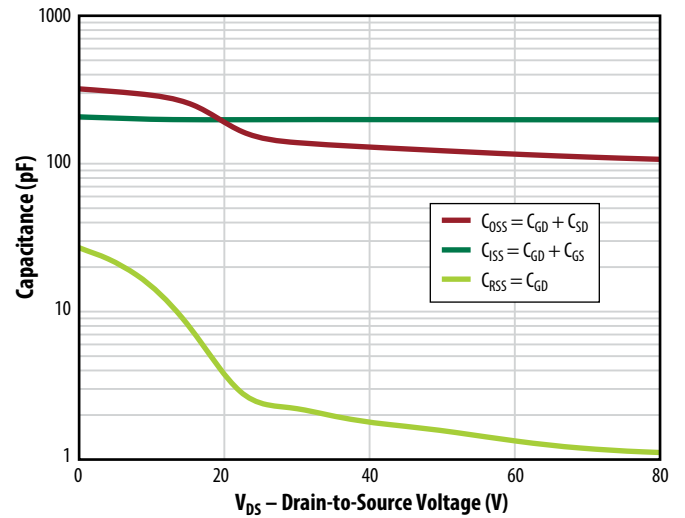


Figure 6: Typical Output Charge and C_{OSS} Stored Energy

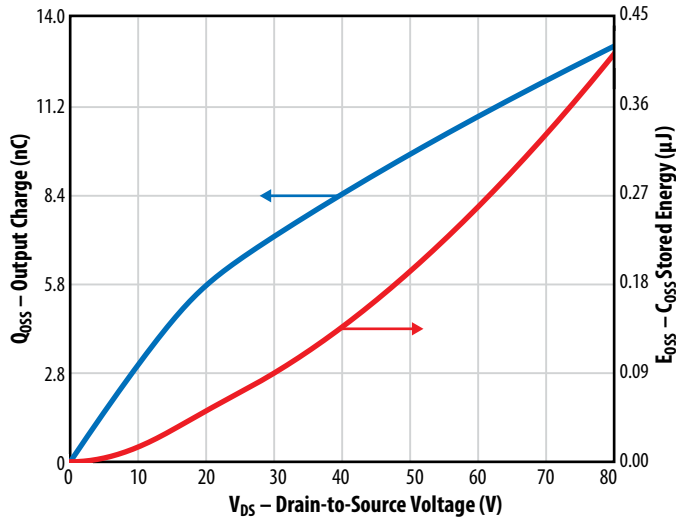


Figure 7: Typical Gate Charge

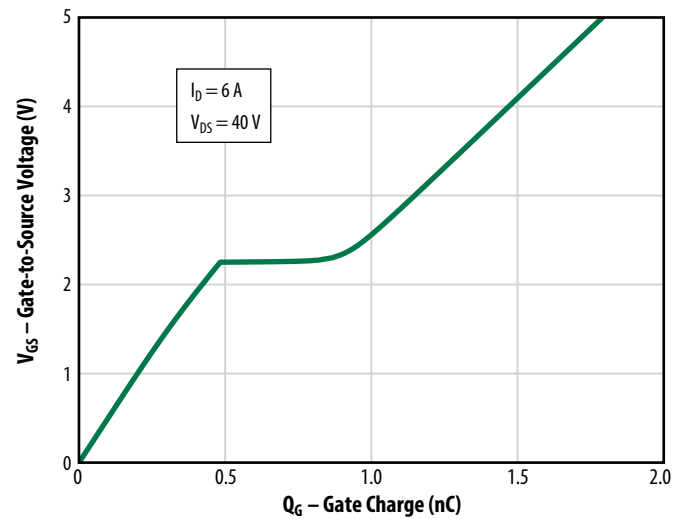
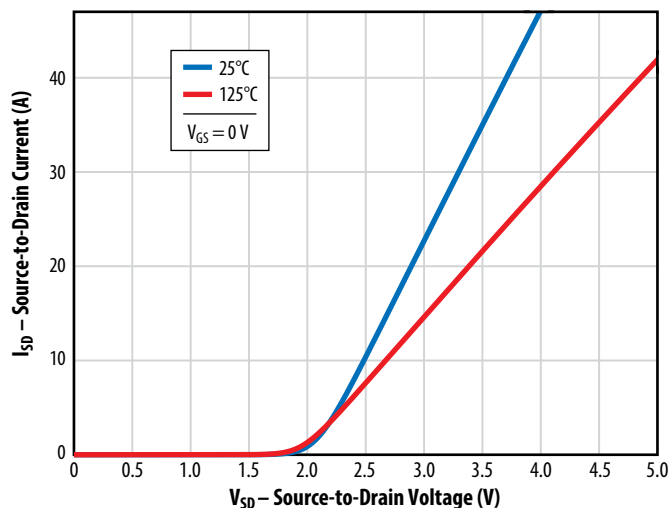


Figure 8: Typical Reverse Drain-Source Characteristics



Note: Negative gate drive voltage increases the reverse drain-source voltage. EPC recommends 0V for OFF.

Figure 9: Typical Normalized On-State Resistance vs. Temp.

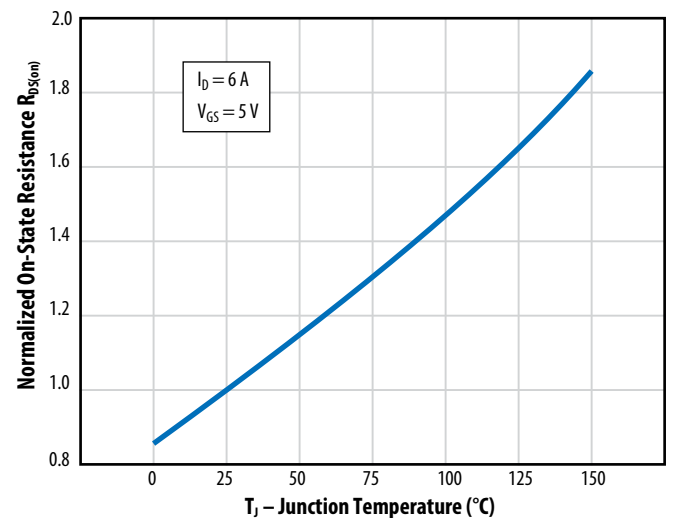


Figure 10: Typical Normalized Threshold Voltage vs. Temp.

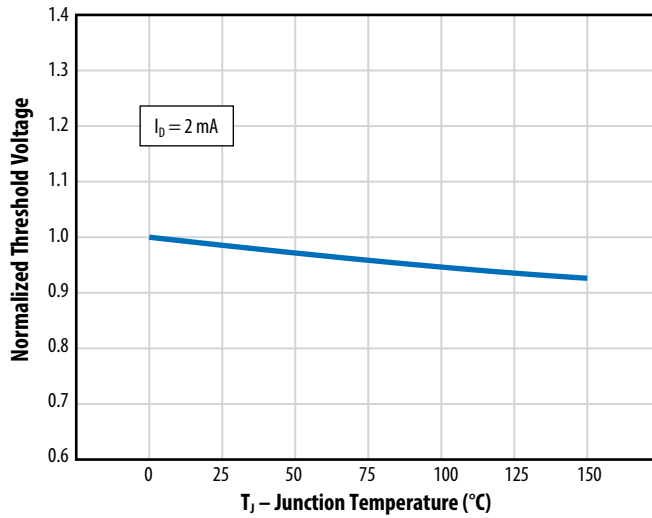


Figure 11: Typical Transient Thermal Response Curves

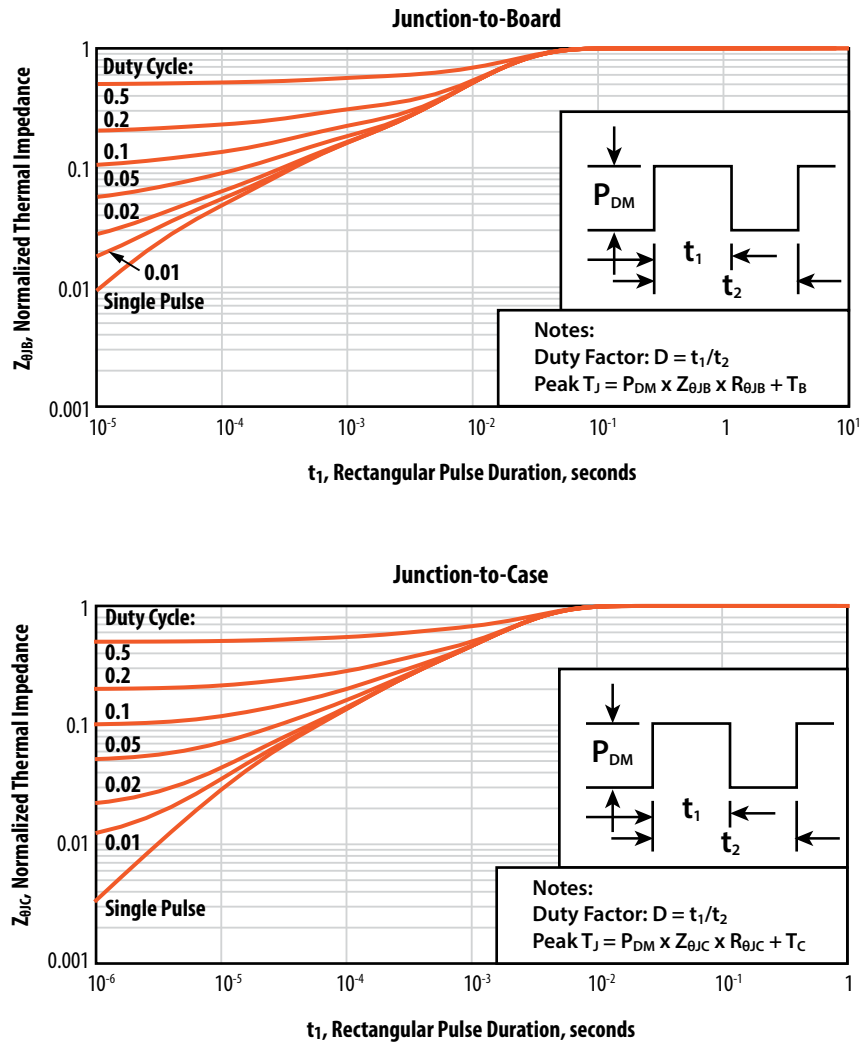
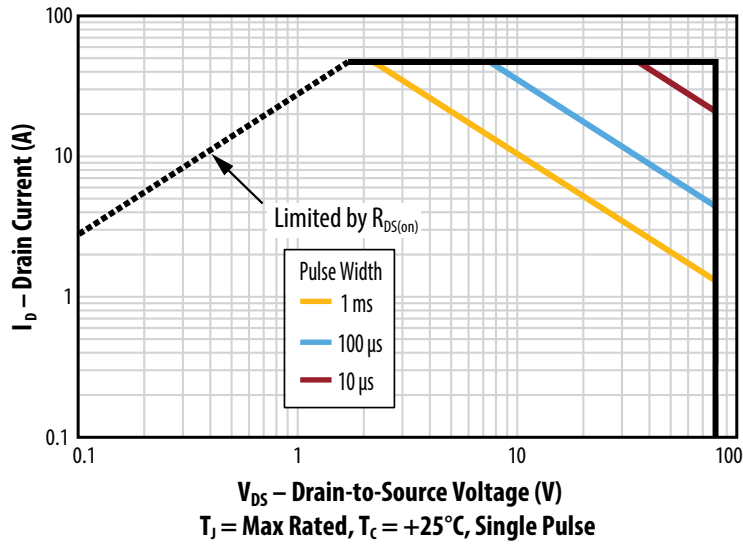
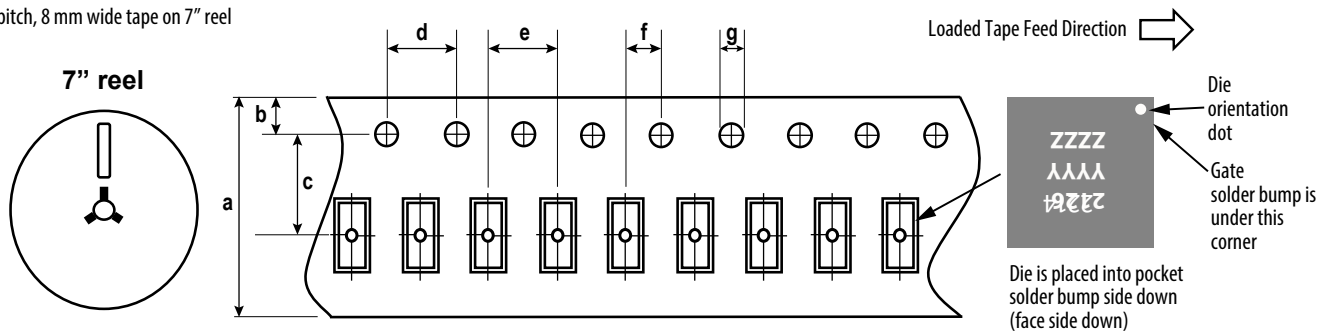


Figure 12: Safe Operating Area



TAPE AND REEL CONFIGURATION

4 mm pitch, 8 mm wide tape on 7" reel

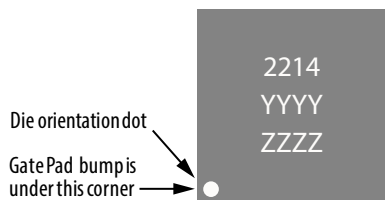


EPC2214 (Note 1)	Dimension (mm)		
	Target	MIN	MAX
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (Note 2)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

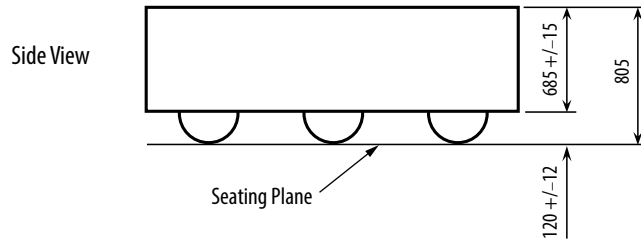
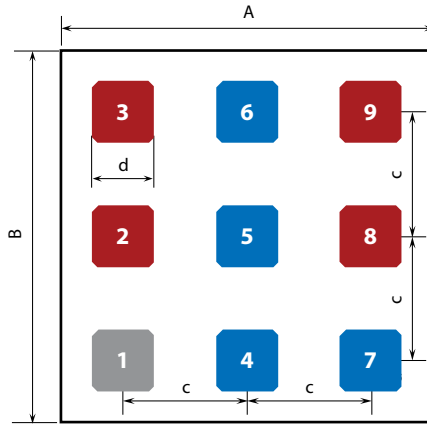
DIE MARKINGS



Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2214	2214	YYYY	ZZZZ

DIE OUTLINE

Pad View



DIM	Micrometers		
	MIN	Nominal	MAX
A	1320	1350	1380
B	1320	1350	1380
c		450	
d		225	

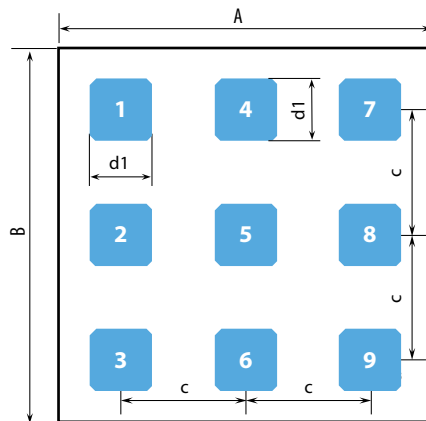
Pad 1 is Gate;

Pads 4, 5, 6, 7 are Drain;

Pads 2, 3, 8, 9 are Source.

RECOMMENDED LAND PATTERN

(measurements in μm)



DIM	Micrometers
A	1350
B	1350
c	450
d1	205

The land pattern is solder mask defined.

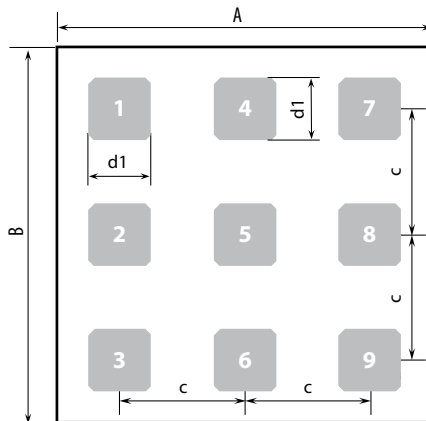
Pad 1 is Gate;

Pads 4, 5, 6, 7 are Drain;

Pads 2, 3, 8, 9 are Source.

RECOMMENDED STENCIL DRAWING

(measurements in μm)



DIM	Micrometers
A	1350
B	1350
c	450
d1	225

Recommended stencil should be 4 mil (100 μm) thick, must be laser cut, openings per drawing.

The corner has a radius of R60.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Additional assembly resources available at

<https://epc-co.com/epc/design-support>

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