

NTMFS4H02N

Power MOSFET

25 V, 193 A, Single N-Channel, SO-8FL

Features

- Optimized Design to Minimize Conduction and Switching Losses
- Optimized Package to Minimize Parasitic Inductances
- Optimized material for improved thermal performance
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- High Performance DC-DC Converters
- System Voltage Rails
- Netcom, Telecom
- Servers & Point of Load

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Units
Drain-to-Source Voltage	V_{DS}	25	V
Gate-to-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JA}$ ($T_A = 25^\circ\text{C}$, Note 1)	I_D	37	A
Power Dissipation $R_{\theta JA}$ ($T_A = 25^\circ\text{C}$, Note 1)	P_D	3.13	W
Continuous Drain Current $R_{\theta JC}$ ($T_C = 25^\circ\text{C}$, Note 1)	I_D	193	A
Power Dissipation $R_{\theta JC}$ ($T_C = 25^\circ\text{C}$, Note 1)	P_D	83	W
Pulsed Drain Current ($t_p = 10 \mu\text{s}$)	I_{DM}	412	A
Single Pulse Drain-to-Source Avalanche Energy (Note 1) ($I_L = 47 \text{ A}_{pk}$, $L = 0.3 \text{ mH}$)	E_{AS}	331	mJ
Drain to Source dV/dt	dV/dt	7	V/ns
Maximum Junction Temperature	$T_{J(max)}$	150	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-55 to 150	$^\circ\text{C}$
Lead Temperature Soldering Reflow (SMD Styles Only), Pb-Free Versions (Note 2)	T_{SLD}	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Values based on copper area of 645 mm^2 (or 1 in^2) of 2 oz copper thickness and FR4 PCB substrate.
2. For more information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERM/D.
3. This is the absolute maximum rating. Parts are 100% UIS tested at $T_J = 25^\circ\text{C}$, $V_{GS} = 10 \text{ V}$, $I_L = 31 \text{ A}$, $E_{AS} = 144 \text{ mJ}$.

THERMAL CHARACTERISTICS

Parameter	Symbol	Max	Units
Thermal Resistance, Junction-to-Ambient (Note 1 and 4) Junction-to-Case (Note 1 and 4)	$R_{\theta JA}$ $R_{\theta JC}$	40.0 1.5	$^\circ\text{C/W}$

4. Thermal Resistance $R_{\theta JA}$ and $R_{\theta JC}$ as defined in JESD51-3.



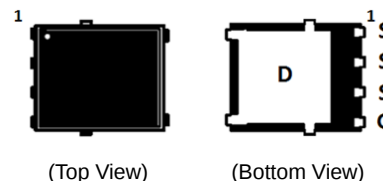
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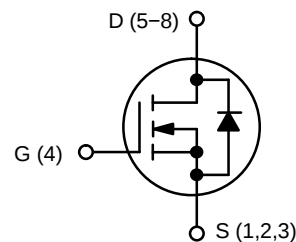
V_{GS}	MAX $R_{DS(on)}$	TYP Q_{GTOT}
4.5 V	2.2 m Ω	18 nC
10 V	1.4 m Ω	38.5 nC

PIN CONNECTIONS

SO8-FL (5 x 6 mm)



N-CHANNEL MOSFET



ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	25			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			18.5		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}$	$T_J = 25^\circ\text{C}$		1	μA
			$T_J = 125^\circ\text{C}$		20	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	1.2		2.1	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			3.7		mV/ $^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 30\text{ A}$		1.1	1.4	m Ω
		$V_{GS} = 4.5\text{ V}, I_D = 30\text{ A}$		1.7	2.2	
Forward Transconductance	g_{FS}	$V_{DS} = 12\text{ V}, I_D = 15\text{ A}$		84		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 12\text{ V}$		2651		pF
Output Capacitance	C_{OSS}			1814		
Reverse Transfer Capacitance	C_{RSS}			103		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 12\text{ V}; I_D = 30\text{ A}$		18		nC
Threshold Gate Charge	$Q_{G(TH)}$			2.7		
Gate-to-Source Charge	Q_{GS}			7.2		
Gate-to-Drain Charge	Q_{GD}			4.2		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 12\text{ V}; I_D = 30\text{ A}$		38.5		nC
Gate Resistance	R_G	$T_A = 25^\circ\text{C}$		1.0	2	Ω

SWITCHING CHARACTERISTICS, $V_{GS} = 4.5\text{ V}$ (Note 5)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DD} = 12\text{ V}, I_D = 15\text{ A}, R_G = 3.0\text{ }\Omega$		13.1		ns
Rise Time	t_r			20		
Turn-Off Delay Time	$t_{d(OFF)}$			22.2		
Fall Time	t_f			9.1		

SWITCHING CHARACTERISTICS, $V_{GS} = 10\text{ V}$ (Note 5)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DD} = 12\text{ V}, I_D = 15\text{ A}, R_G = 3.0\text{ }\Omega$		9.5		ns
Rise Time	t_r			18.5		
Turn-Off Delay Time	$t_{d(OFF)}$			30.3		
Fall Time	t_f			5		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 10\text{ A}$	$T_J = 25^\circ\text{C}$		0.75	1.1	V
			$T_J = 125^\circ\text{C}$		0.56		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = 30\text{ A}$		46.3		ns	
Charge Time	t_a			23.9			
Discharge Time	t_b			22.4			
Reverse Recovery Charge	Q_{RR}			51		nC	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

6. Switching characteristics are independent of operating junction temperatures.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
PACKAGE PARASITIC VALUES						
Source Inductance	L_S	$T_A = 25^\circ\text{C}$		0.57		nH
Drain Inductance	L_D			0.13		nH
Gate Inductance	L_G			1.37		nH

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

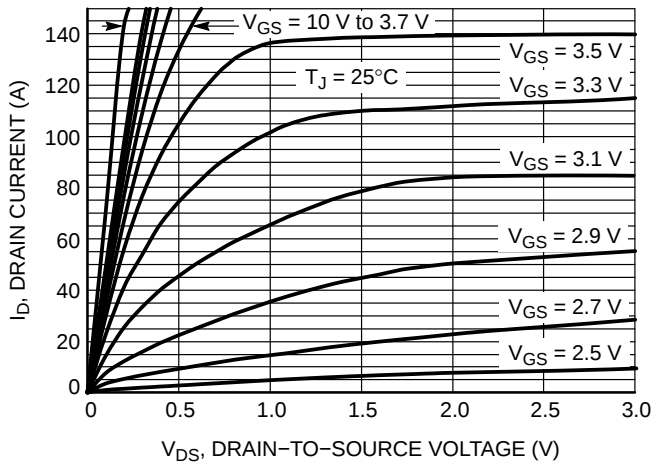


Figure 1. On-Region Characteristics

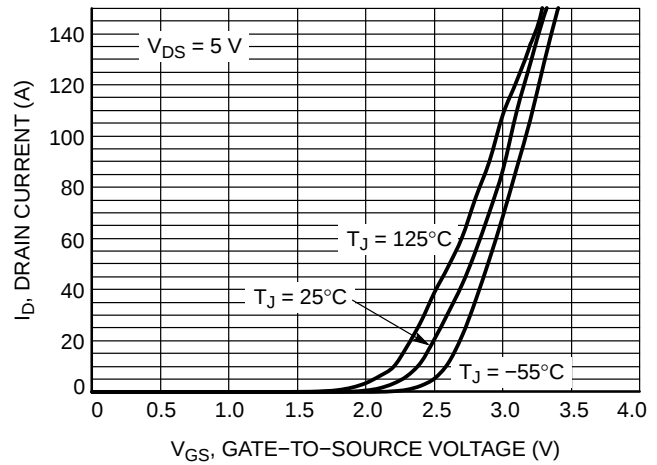


Figure 2. Transfer Characteristics

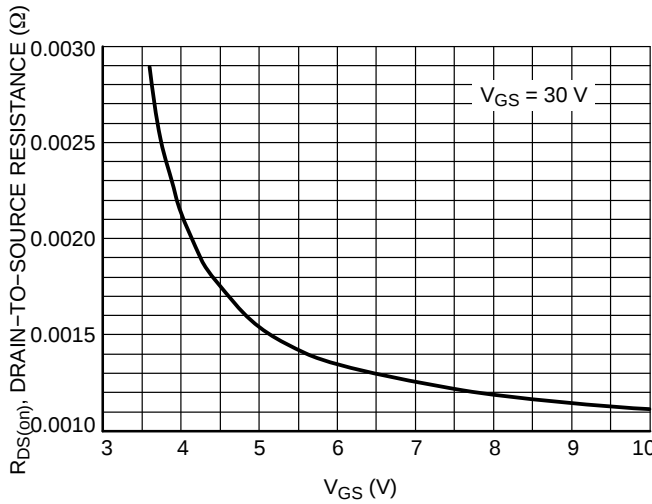


Figure 3. On-Resistance vs. V_{GS}

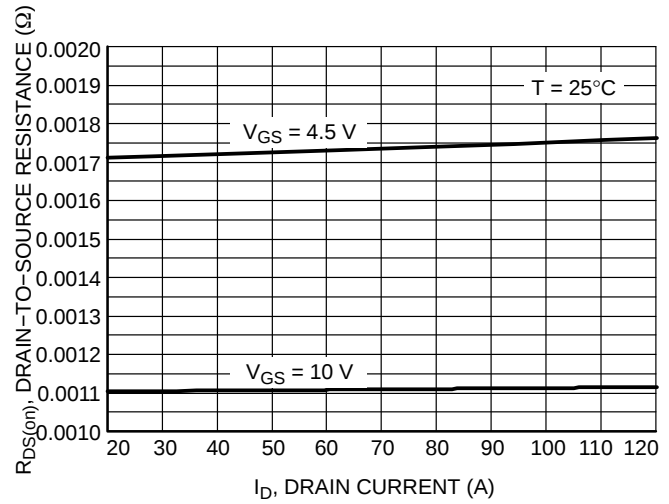


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

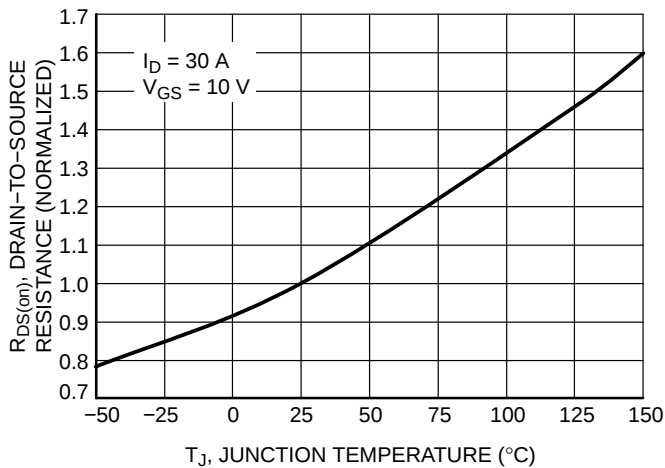


Figure 5. On-Resistance Variation with Temperature

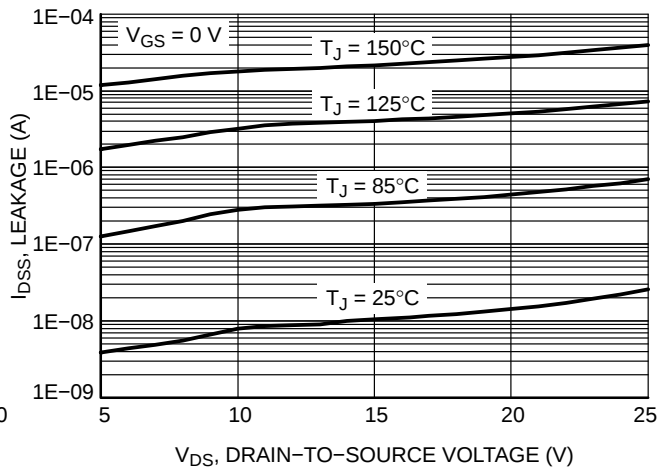


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

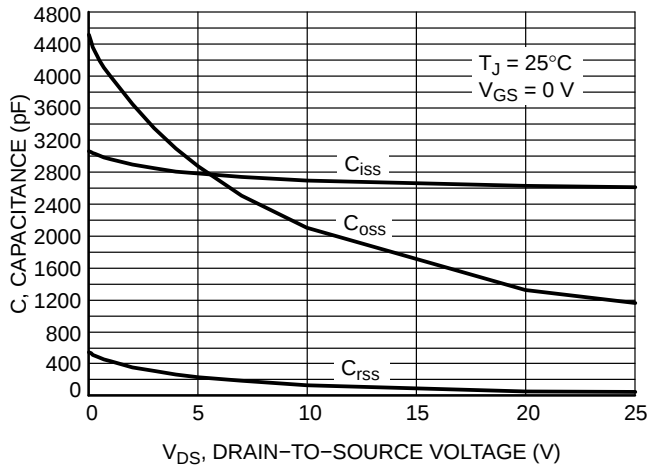


Figure 7. Capacitance Variation

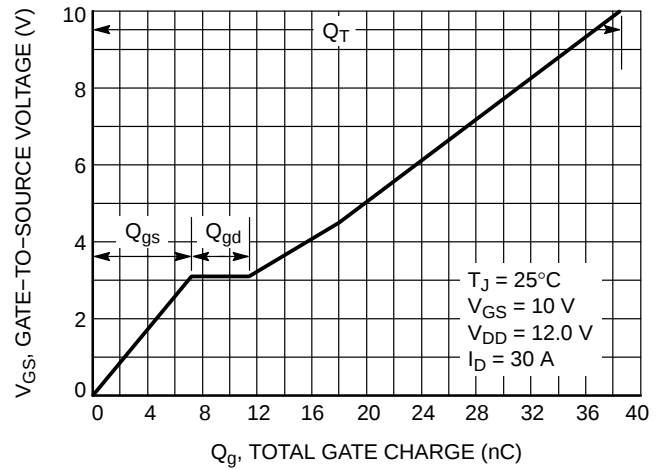


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

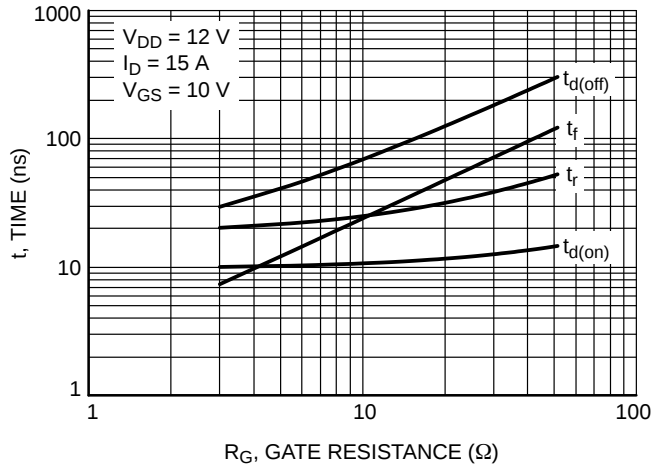


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

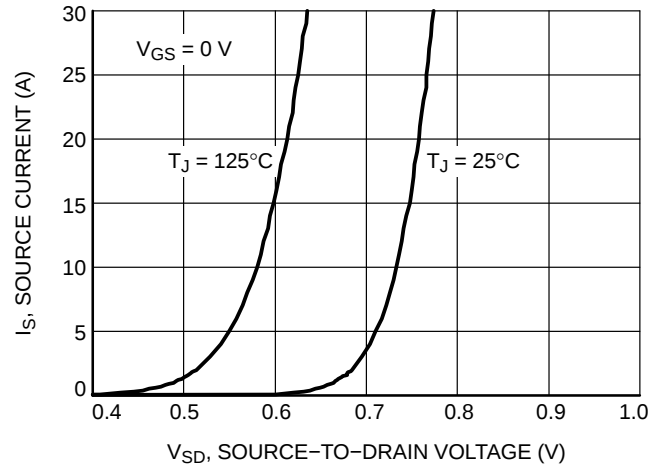


Figure 10. Diode Forward Voltage vs. Current

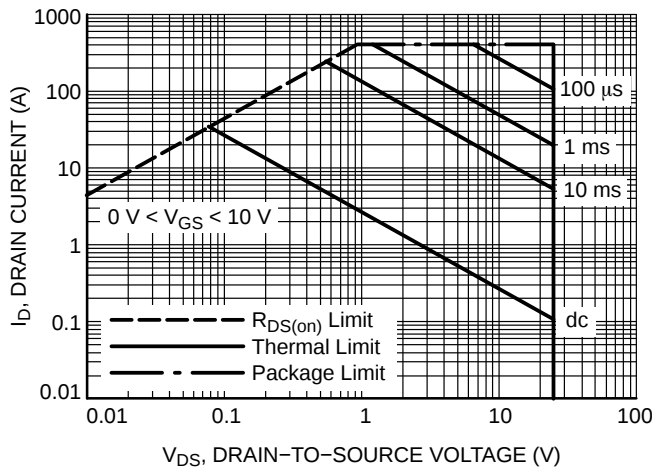


Figure 11. Maximum Rated Forward Biased Safe Operating Area

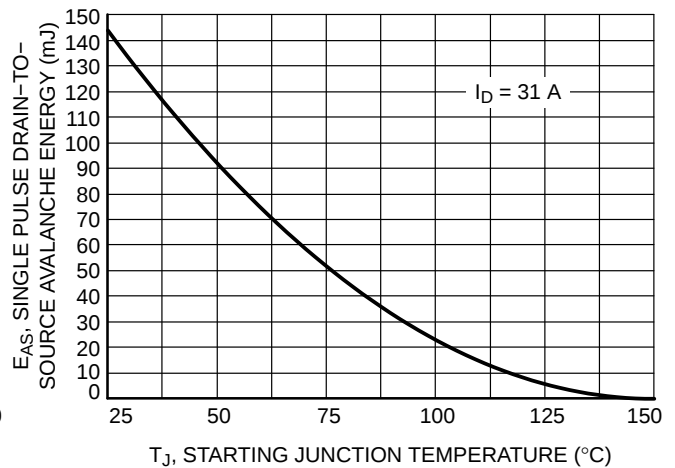


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

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TYPICAL CHARACTERISTICS

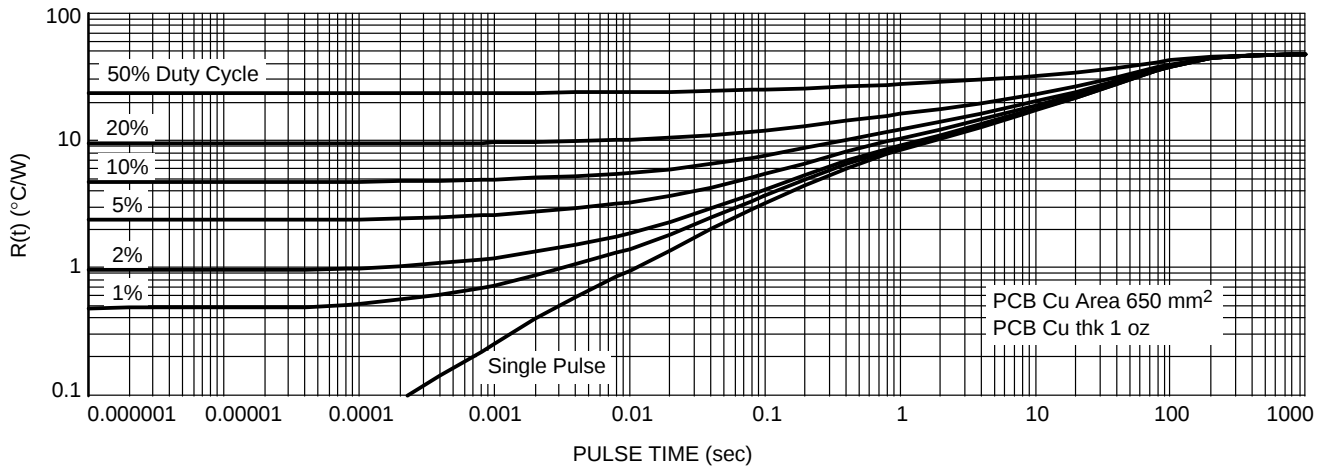


Figure 13. Thermal Characteristics

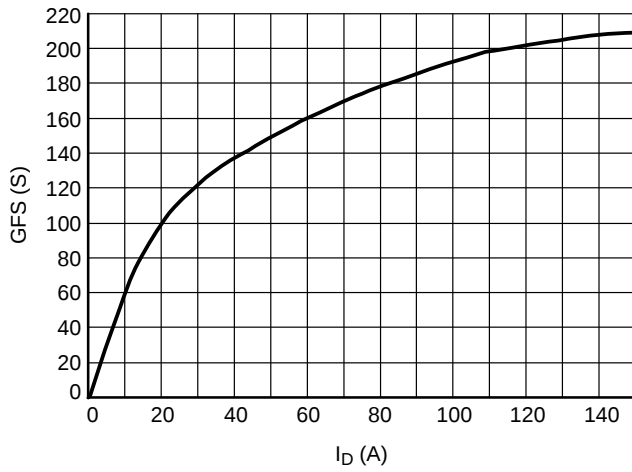


Figure 14. GFS vs. I_D

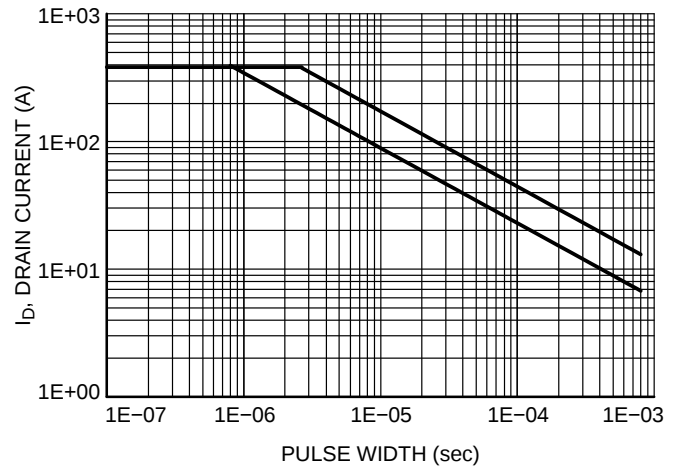


Figure 15. Avalanche Characteristics

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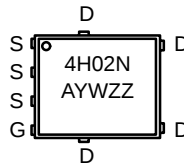
ORDERING INFORMATION

Device	Package	Shipping†
NTMFS4H02NT1G	SO8-FL (Pb-Free)	1500 / Tape & Reel
NTMFS4H02NT3G	SO8-FL (Pb-Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



MARKING DIAGRAM

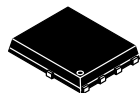


A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

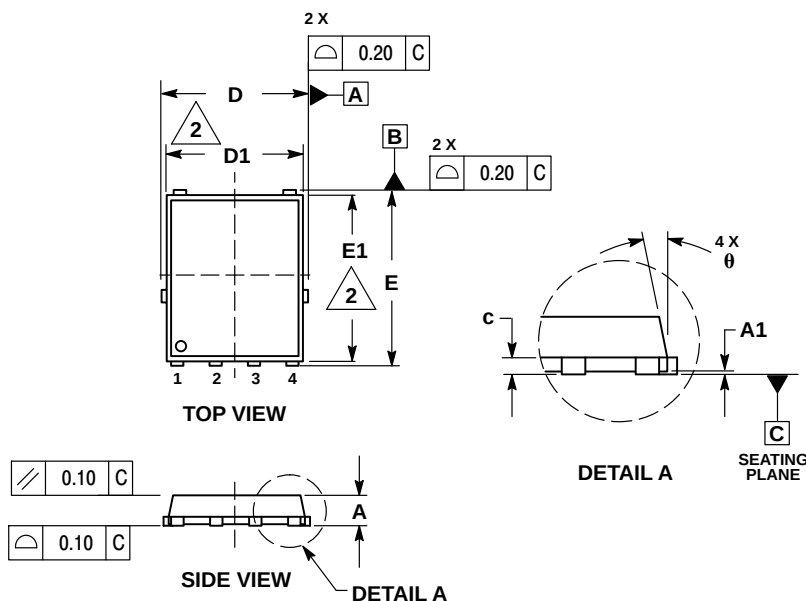
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SCALE 2:1

DFN5 5x6, 1.27P
(SO-8FL)
CASE 488AA
ISSUE N

DATE 25 JUN 2018



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

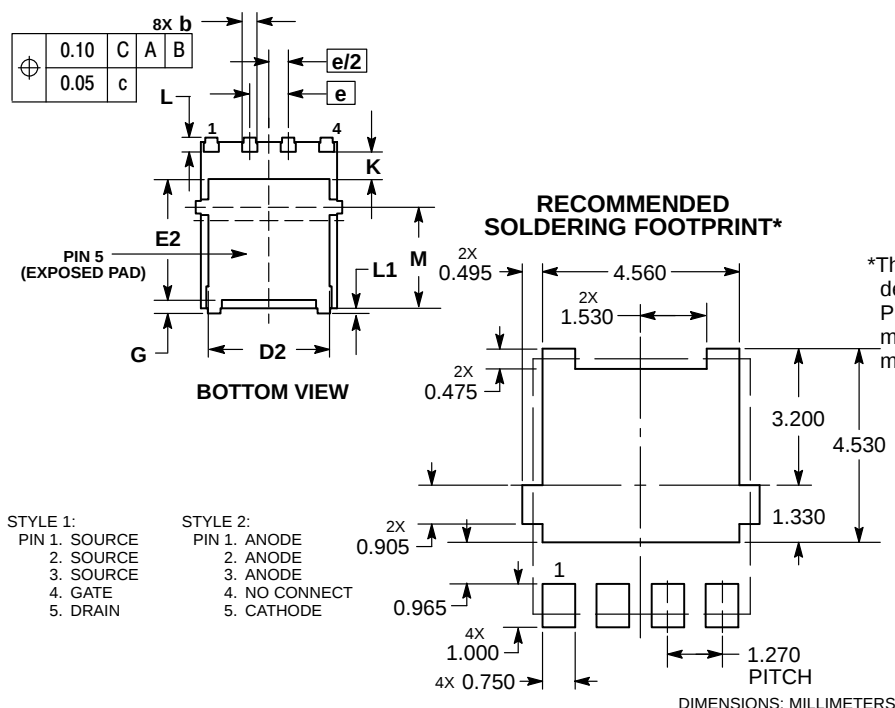
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
theta	0°	---	12°

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN

STYLE 2:
PIN 1. ANODE
2. ANODE
3. ANODE
4. NO CONNECT
5. CATHODE

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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