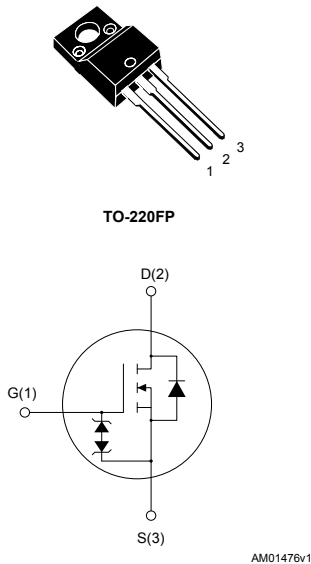


N-channel 600 V, 110 mΩ typ., 24 A MDmesh DM2 Power MOSFET in a TO-220FP package


Product status link
[STF33N60DM2](#)
Product summary

Order code	STF33N60DM2
Marking	33N60DM2
Package	TO-220FP
Packing	Tube

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STF33N60DM2	600 V	130 mΩ	24 A

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

- Switching applications

Description

This high-voltage N-channel Power MOSFET is part of the MDmesh DM2 fast-recovery diode series. It offers very low recovery charge (Q_{rr}) and time (t_{rr}) combined with low $R_{DS(on)}$, rendering it suitable for the most demanding high-efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate-source voltage (static)	± 25	V
	Gate-source voltage (dynamic AC, $f > 1$ Hz)	± 30	
I_D	Drain current (continuous) at $T_C = 25$ °C	24	A
	Drain current (continuous) at $T_C = 100$ °C	15.5	
$I_{DM}^{(1)}$	Drain current (pulsed)	96	A
P_{TOT}	Total power dissipation at $T_C = 25$ °C	35	W
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1$ s; $T_C = 25$ °C)	2.5	kV
$dv/dt^{(2)}$	Peak diode recovery voltage slope	100	V/ns
$di/dt^{(2)}$	Peak diode recovery current slope	1000	A/ μ s
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	100	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 24$ A, $V_{DS} (peak) < V_{(BR)DSS}$. $V_{DD} = 400$ V.
3. $V_{DD} \leq 480$ V.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	3.6	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	62.5	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max.)	5.5	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25$ °C, $I_D = I_{AR}$, $V_{DD} = 50$ V)	570	mJ

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	600	-	-	V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$	-	-	1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$, $T_C = 125\text{ °C}^{(1)}$	-	-	100	
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$	-	-	± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 12\text{ A}$	-	110	130	m Ω

1. Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	1870	-	pF
C_{oss}	Output capacitance		-	87	-	pF
C_{rss}	Reverse transfer capacitance		-	2	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{ to }480\text{ V}$	-	157	-	pF
R_g	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	4.5	-	Ω
Q_g	Total gate charge	$V_{DD} = 480\text{ V}$, $I_D = 24\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see the Figure 14. Test circuit for gate charge behavior)	-	43	-	nC
Q_{gs}	Gate-source charge		-	9.8	-	nC
Q_{gd}	Gate-drain charge		-	21	-	nC

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 12\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	17	-	ns
t_r	Rise time		-	8	-	ns
$t_{d(off)}$	Turn-off delay time	(see the Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	62	-	ns
t_f	Fall time		-	9	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-	-	24	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-	-	96	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 24 \text{ A}$, $V_{GS} = 0 \text{ V}$	-	-	1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 24 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$,	-	120	-	ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60 \text{ V}$	-	0.53	-	μC
I_{RRM}	Reverse recovery current	(see the Figure 15. Test circuit for inductive load switching and diode recovery times)	-	8.8	-	A
t_{rr}	Reverse recovery time	$I_{SD} = 24 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$,	-	316	-	ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60 \text{ V}$, $T_J = 150 \text{ }^\circ\text{C}$	-	2.85	-	μC
I_{RRM}	Reverse recovery current	(see the Figure 15. Test circuit for inductive load switching and diode recovery times)	-	18	-	A

1. Pulse width is limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

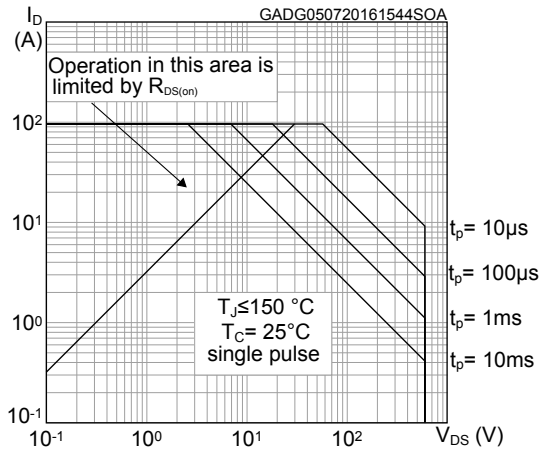
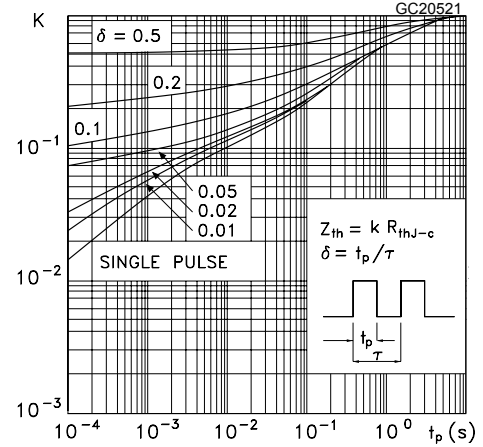
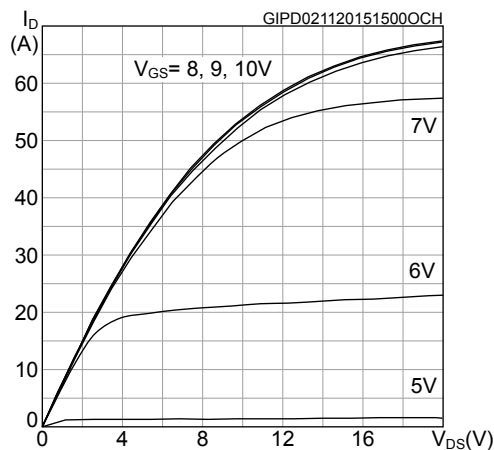
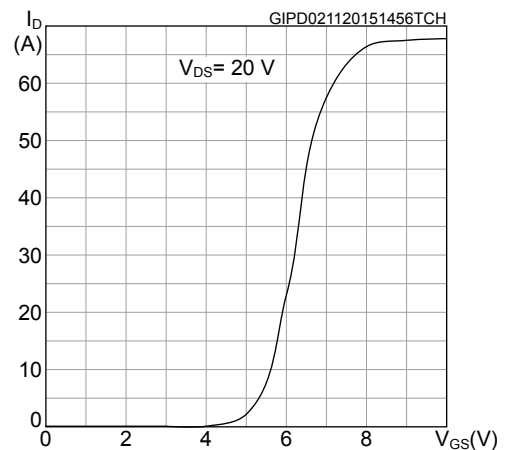
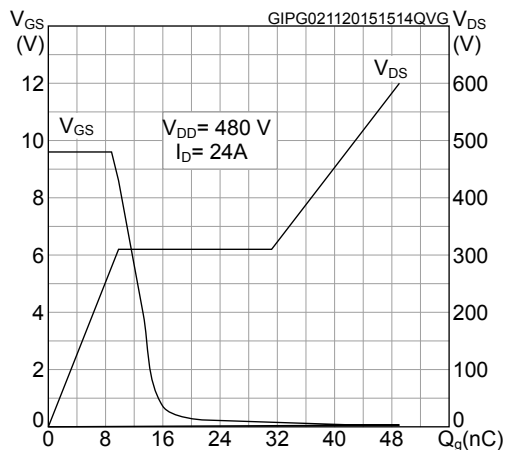
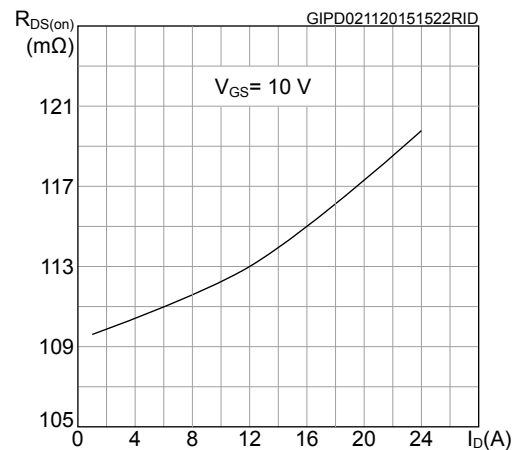
Figure 1. Safe operating area

Figure 2. Normalized transient thermal impedance

Figure 3. Typical output characteristics

Figure 4. Typical transfer characteristics

Figure 5. Typical gate charge characteristics

Figure 6. Typical drain-source on-resistance


Figure 7. Typical capacitance characteristics

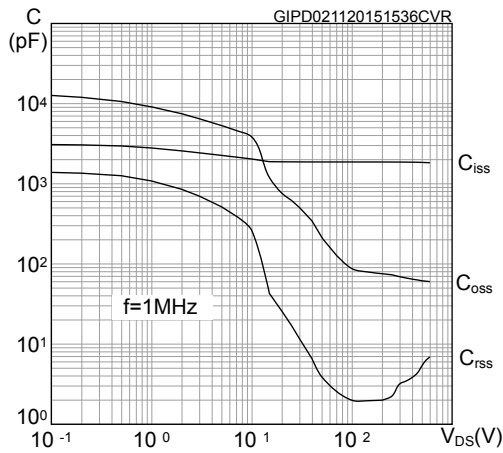


Figure 8. Typical output capacitance stored energy

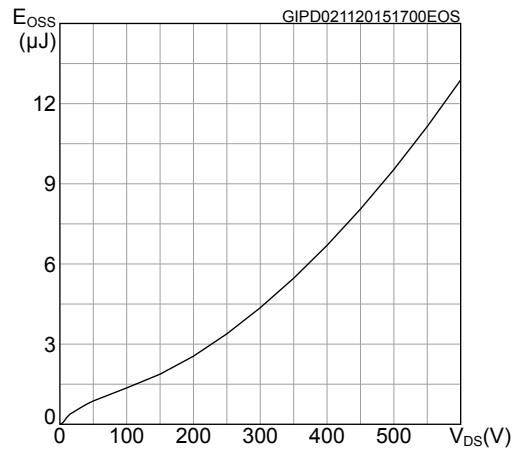


Figure 9. Normalized gate threshold vs temperature

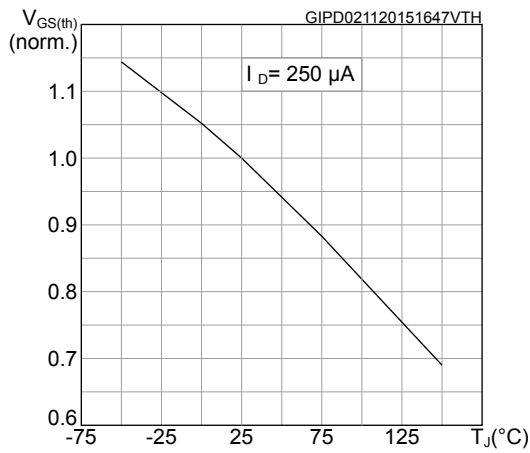


Figure 10. Normalized on-resistance vs temperature

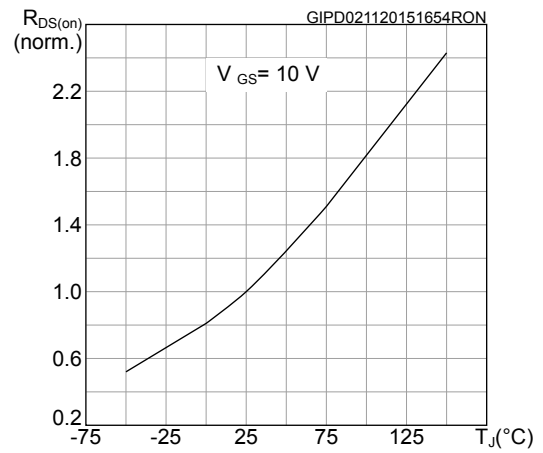


Figure 11. Normalized breakdown voltage vs temperature

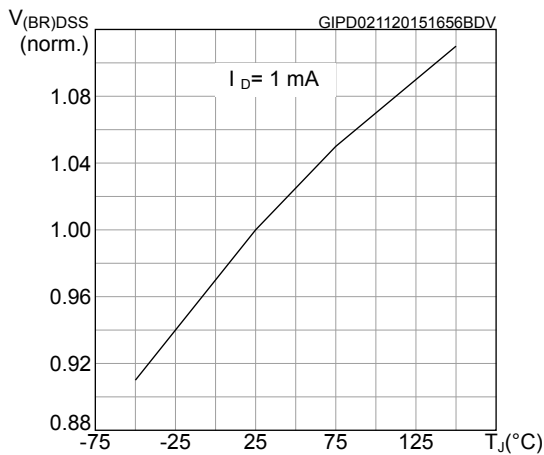
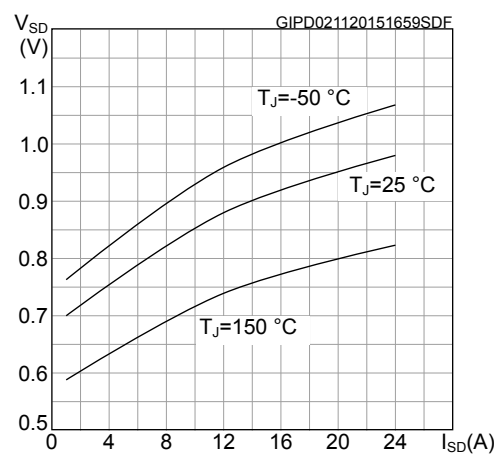


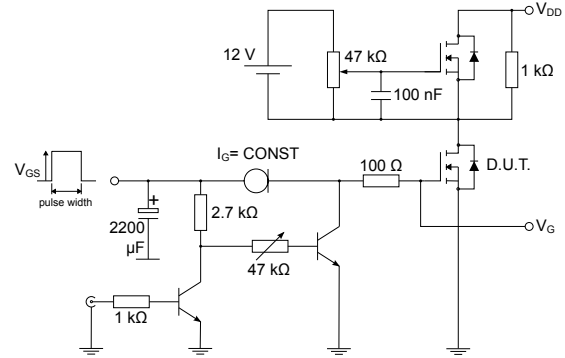
Figure 12. Typical reverse diode forward characteristics



3 Test circuits

Figure 13. Test circuit for resistive load switching times


AM01468v1

Figure 14. Test circuit for gate charge behavior


AM01469v1

Figure 15. Test circuit for inductive load switching and diode recovery times


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Figure 16. Unclamped inductive load test circuit


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Figure 17. Unclamped inductive waveform


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Figure 18. Switching time waveform

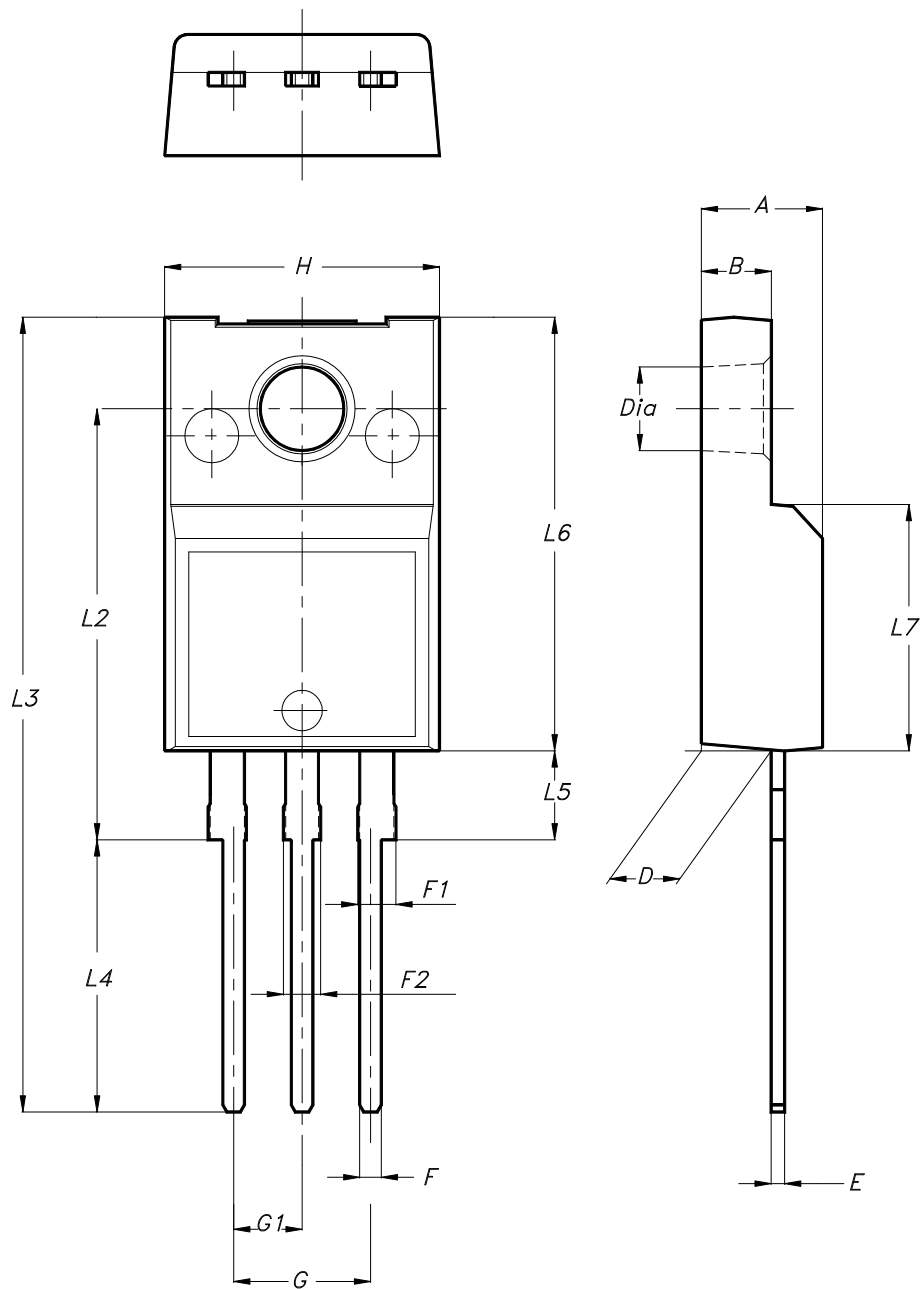

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4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220FP type B package information

Figure 19. TO-220FP type B package outline



7012510_B_rev.14

Table 8. TO-220FP type B package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.20
G1	2.40		2.70
H	10.00		10.40
L2		16.00	
L3	28.60		30.60
L4	9.80		10.60
L5	2.90		3.60
L6	15.90		16.40
L7	9.00		9.30
Dia	3.00		3.20

Revision history

Table 9. Document revision history

Date	Version	Changes
04-Sep-2014	1	First release.
05-Jul-2016	2	Document status promoted from preliminary to production data. Updated title and features in cover page. Updated <i>Section 1: "Electrical ratings"</i> and <i>Section 2: "Electrical characteristics"</i> . Added <i>Section 2.1: "Electrical characteristics (curves)"</i> . Minor text changes.
16-Apr-2026	3	Updated Section 4: Package information . Minor text changes.

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