

MOS FIELD EFFECT TRANSISTOR

μ PA2727T1A

SWITCHING

N-CHANNEL POWER MOSFET

DESCRIPTION

The μ PA2727T1A is N-channel MOSFET designed for DC/DC converter applications.

FEATURES

- Low on-state resistance
 $R_{DS(on)1} = 9.6 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 8 \text{ A)}$
 $R_{DS(on)2} = 15 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 8 \text{ A)}$
- Low Q_{GD}
 $Q_{GD} = 3.5 \text{ nC TYP. (} V_{DD} = 15 \text{ V, } I_D = 16 \text{ A)}$
- Built-in gate protection diode
- Thin type surface mount package with heat spreader (8-pin HVSON)
- RoHS Compliant

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, All terminals are connected.)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	30	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 20	V
Drain Current (DC)	$I_{D(DC)}$	± 16	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	± 96	A
Total Power Dissipation ^{Note2}	P_{T1}	1.5	W
Total Power Dissipation (PW = 10 sec) ^{Note2}	P_{T2}	4.6	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	$-55 \text{ to } +150$	$^\circ\text{C}$
Single Avalanche Current ^{Note3}	I_{AS}	16	A
Single Avalanche Energy ^{Note3}	E_{AS}	26	mJ

THERMAL RESISTANCE

Channel to Ambient Thermal Resistance ^{Note2}	$R_{th(ch-A)}$	83.3	$^\circ\text{C/W}$
Channel to Case (Drain) Thermal Resistance	$R_{th(ch-C)}$	2.0	$^\circ\text{C/W}$

Notes 1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

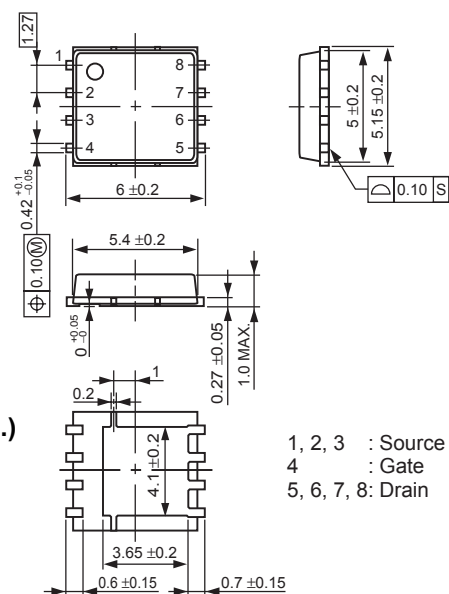
2. Mounted on a glass epoxy board of 25.4 mm x 25.4 mm x 0.8 mm

3. Starting $T_{ch} = 25^\circ\text{C}$, $V_{DD} = 15 \text{ V}$, $R_G = 25 \Omega$, $V_{GS} = 20 \rightarrow 0 \text{ V}$, $L = 100 \mu\text{H}$

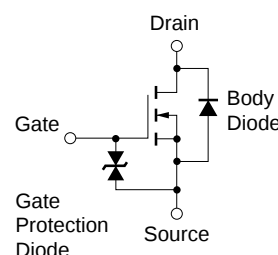
Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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PACKAGE DRAWING (Unit: mm)



EQUIVALENT CIRCUIT

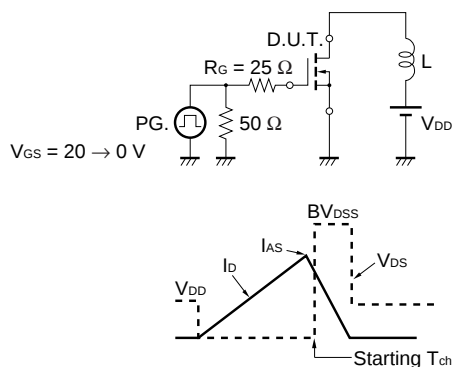


<R> ELECTRICAL CHARACTERISTICS (T_A = 25°C, All terminals are connected.)

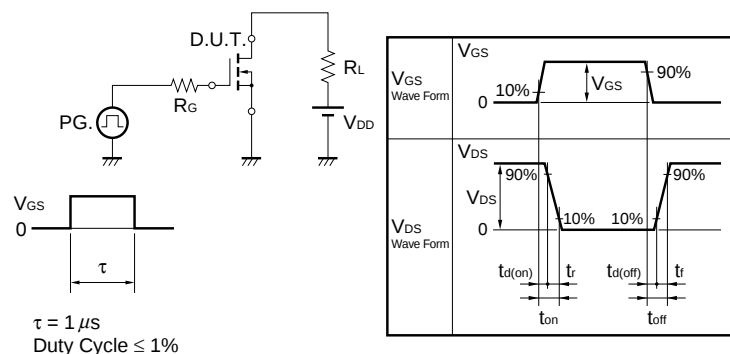
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			10	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±16 V, V _{DS} = 0 V			±10	μA
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5		2.5	V
Forward Transfer Admittance ^{Note}	y _{fs}	V _{DS} = 10 V, I _D = 8 A	6			S
Drain to Source On-state Resistance ^{Note}	R _{DS(on)1}	V _{GS} = 10 V, I _D = 8 A		7.6	9.6	mΩ
	R _{DS(on)2}	V _{GS} = 4.5 V, I _D = 8 A		11	15	mΩ
Input Capacitance	C _{iss}	V _{DS} = 15 V,		1170		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V,		250		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		90		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 15 V, I _D = 8 A,		13		ns
Rise Time	t _r	V _{GS} = 10 V,		3.6		ns
Turn-off Delay Time	t _{d(off)}	R _G = 10 Ω		41		ns
Fall Time	t _f			8		ns
Total Gate Charge	Q _G	V _{DD} = 15 V,		11		nC
Gate to Source Charge	Q _{GS}	V _{GS} = 5 V,		3.8		nC
Gate to Drain Charge	Q _{GD}	I _D = 16 A		3.5		nC
Body Diode Forward Voltage ^{Note}	V _{F(S-D)}	I _F = 16 A, V _{GS} = 0 V		0.83		V
Reverse Recovery Time	t _{rr}	I _F = 16 A, V _{GS} = 0 V,		27		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		23		nC
Gate Resistance	R _G	f = 1 MHz		2.2		Ω

Note Pulsed

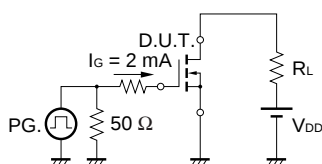
TEST CIRCUIT 1 AVALANCHE CAPABILITY



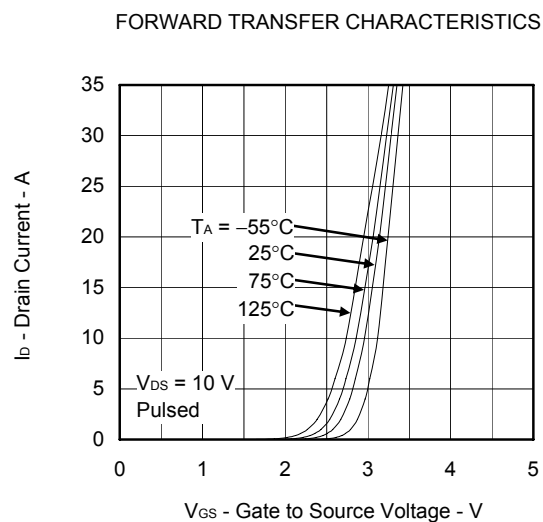
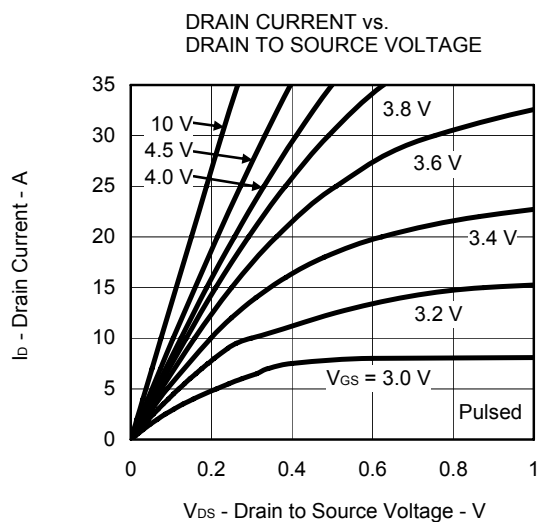
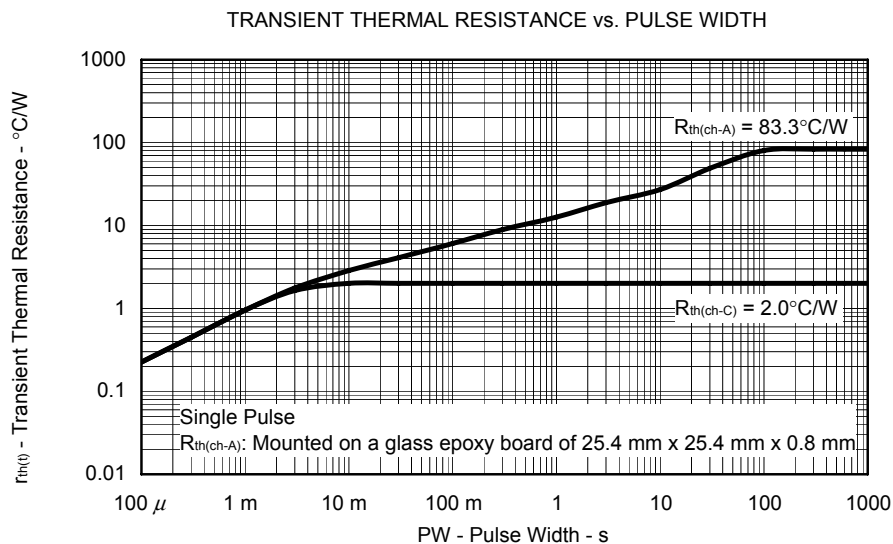
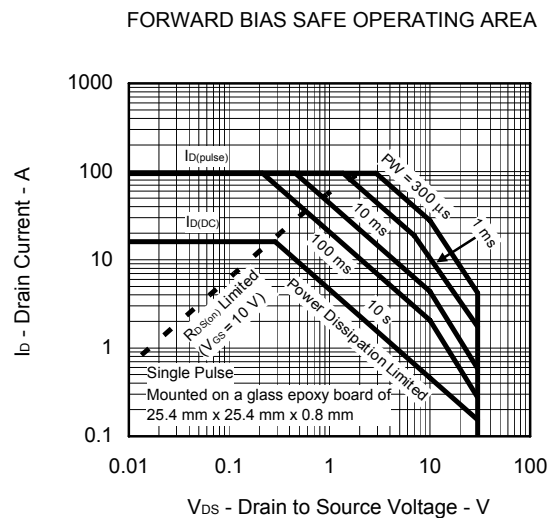
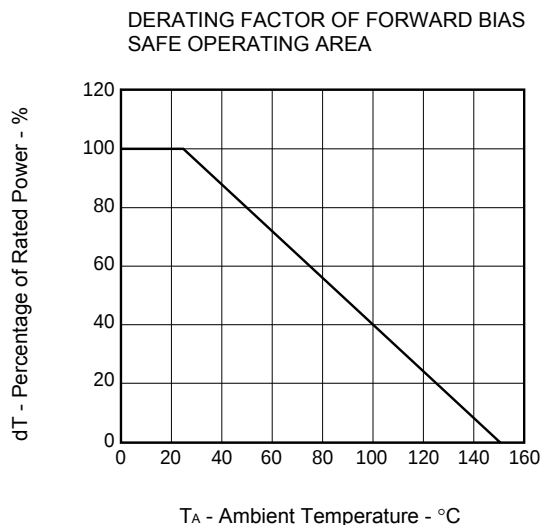
TEST CIRCUIT 2 SWITCHING TIME



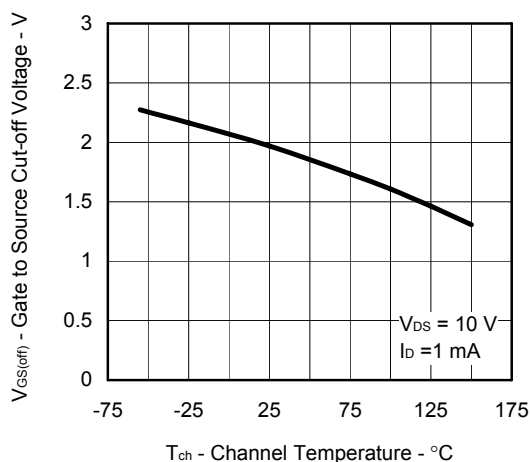
TEST CIRCUIT 3 GATE CHARGE



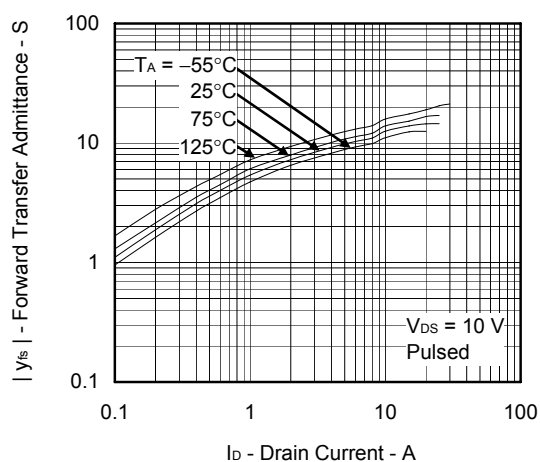
<R> TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)



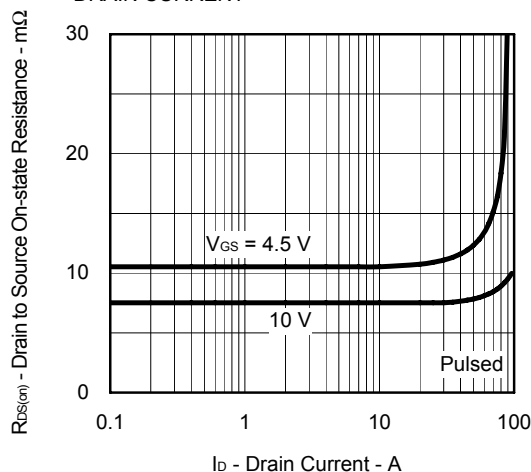
GATE TO SOURCE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



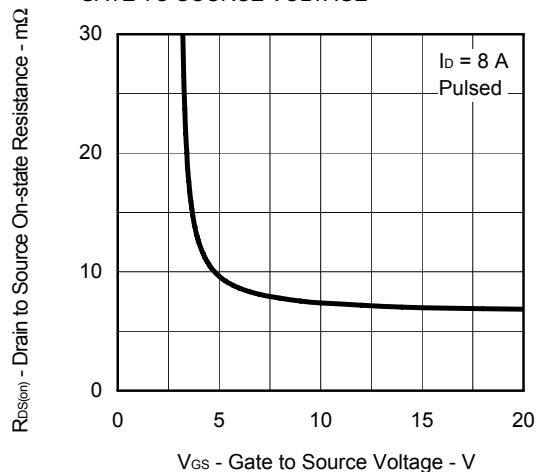
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



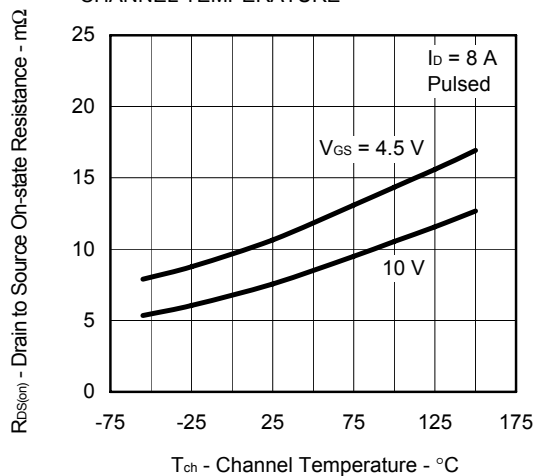
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



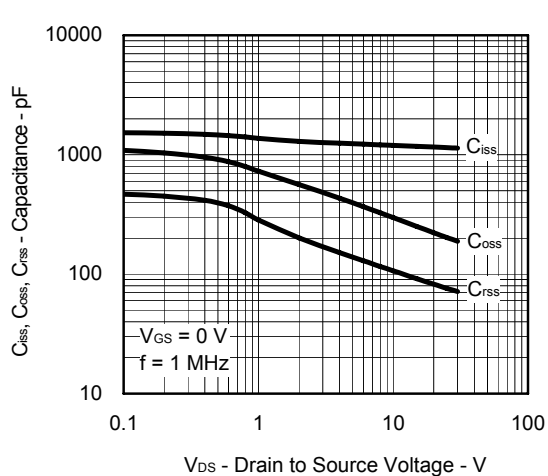
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



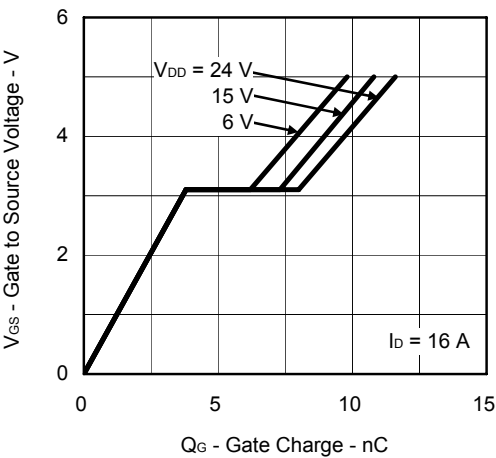
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
CHANNEL TEMPERATURE



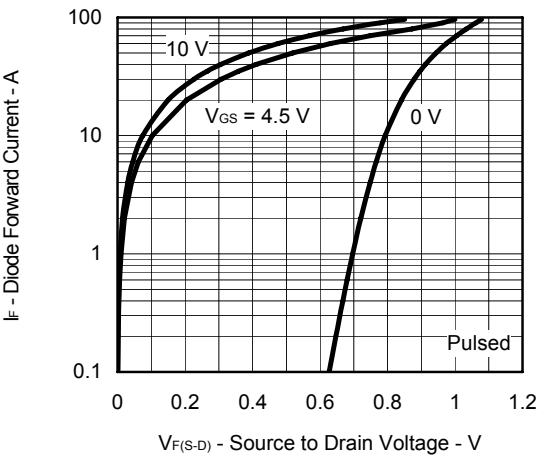
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
μ PA2727T1A-E1-AZ ^{Note}	Sn-Bi	Tape 3000 p/reel	8-pin HVSON 0.10 g TYP.
μ PA2727T1A-E2-AZ ^{Note}			
μ PA2727T1A-E1-AY ^{Note}	Pure Sn		
μ PA2727T1A-E2-AY ^{Note}			

Note Pb-free (This product does not contain Pb in the external electrode.)

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