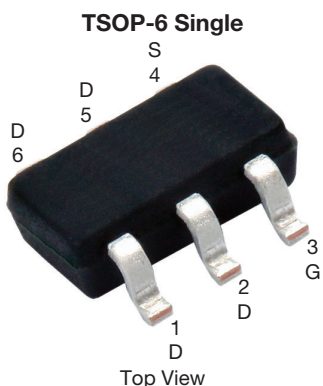


N-Channel 150 V (D-S) MOSFET



FEATURES

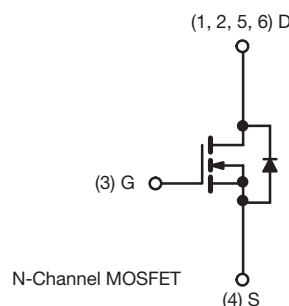
- TrenchFET® power MOSFET
- PWM optimized for fast switching in small footprint
- 100 % R_g tested
- Material categorization:
for definitions of compliance please see
www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Primary side switch for low power DC/DC converters



PRODUCT SUMMARY	
V _{DS} (V)	150
R _{DS(on)} max. (Ω) at V _{GS} = 10 V	0.375
R _{DS(on)} max. (Ω) at V _{GS} = 6 V	0.400
Q _g typ. (nC)	5.4
I _D (A)	1.5
Configuration	Single

ORDERING INFORMATION	
Package	TSOP-6
Lead (Pb)-free	Si3440DV-T1-E3
Lead (Pb)-free and halogen-free	Si3440DV-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	V _{DS}	150	V	
Gate-source voltage	V _{GS}	± 20	V	
Continuous drain current (T _J = 175 °C) ^a	T _A = 25 °C	1.2	A	
	T _A = 85 °C	0.8		
Pulsed drain current	I _{DM}	6		
Single avalanche current	I _{AS}	4		
Single avalanche energy (duty cycle ≤ 1 %)	E _{AS}	0.8	mJ	
Continuous source current (diode conduction) ^a	I _S	1	A	
Maximum power dissipation ^a	T _A = 25 °C	1.14	W	
	T _A = 85 °C	0.59		
Operating junction and storage temperature range	T _J , T _{stg}	-55 to +150	°C	

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT	
Maximum junction-to-ambient ^a	R _{thJA}	45	62.5	°C/W	
		90	110		
Maximum junction-to-foot (drain)	R _{thJF}	25	30		

Notes

a. Surface mounted on 1" x 1" FR4 board



SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Gate threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	-	4	V
Gate-body leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 150\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	1	μA
		$V_{DS} = 150\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 85\text{ }^{\circ}\text{C}$	-	-	5	
On-state drain current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}$, $V_{GS} = 10\text{ V}$	4	-	-	A
Drain-source on-state resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 1.5\text{ A}$	-	0.310	0.375	Ω
		$V_{GS} = 6\text{ V}$, $I_D = 1.4\text{ A}$	-	0.330	0.400	
Forward transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}$, $I_D = 1.5\text{ A}$	-	4.1	-	S
Diode forward voltage ^a	V_{SD}	$I_S = 1.7\text{ A}$, $V_{GS} = 0\text{ V}$	-	0.8	1.2	V
Dynamic ^b						
Total gate charge	Q_g	$V_{DS} = 75\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 1.5\text{ A}$	-	5.4	8	nC
Gate-source charge	Q_{gs}		-	1.1	-	
Gate-drain charge	Q_{gd}		-	1.9	-	
Gate resistance	R_g	$f = 1\text{ MHz}$	4	9	15	Ω
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 75\text{ V}$, $R_L = 75\text{ }\Omega$ $I_D \cong 1\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 6\text{ }\Omega$	-	8	15	ns
Rise time	t_r		-	10	15	
Turn-off delay time	$t_{d(off)}$		-	20	30	
Fall time	t_f		-	15	25	
Source-drain reverse recovery time	t_{rr}	$I_F = 1.7\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}$	-	40	60	

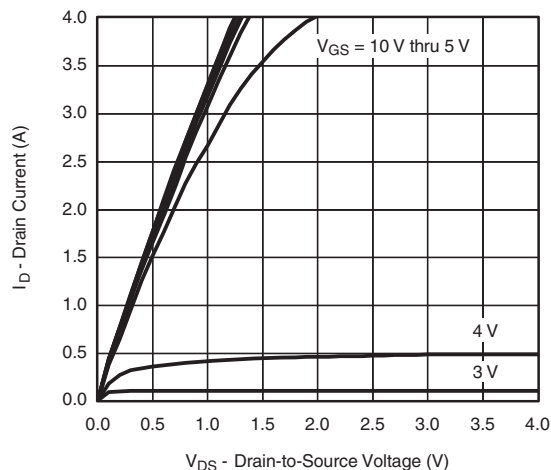
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing

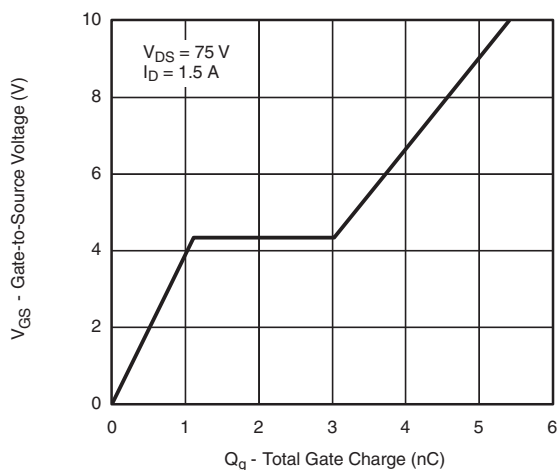
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



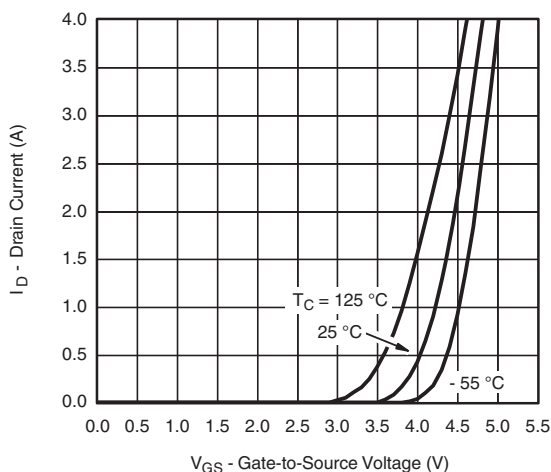
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



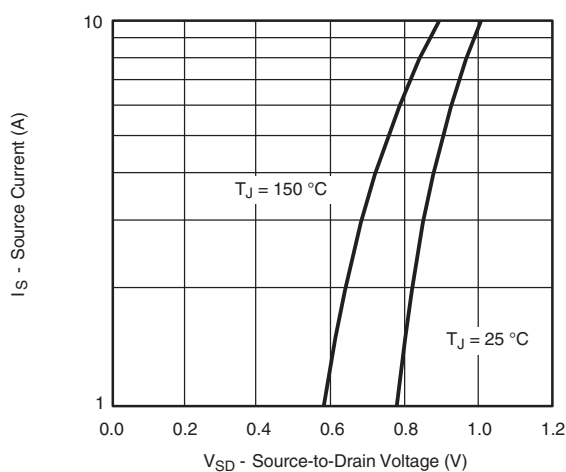
Output Characteristics



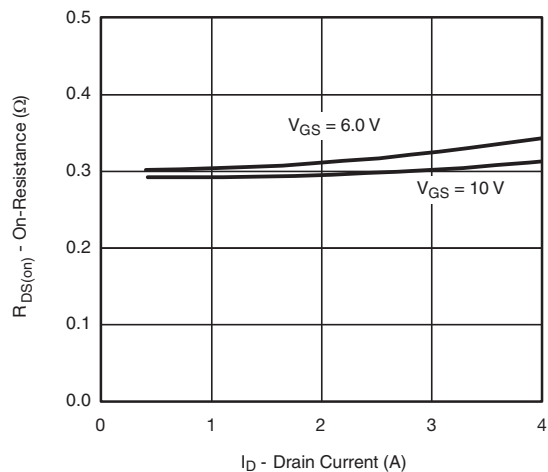
Gate Charge



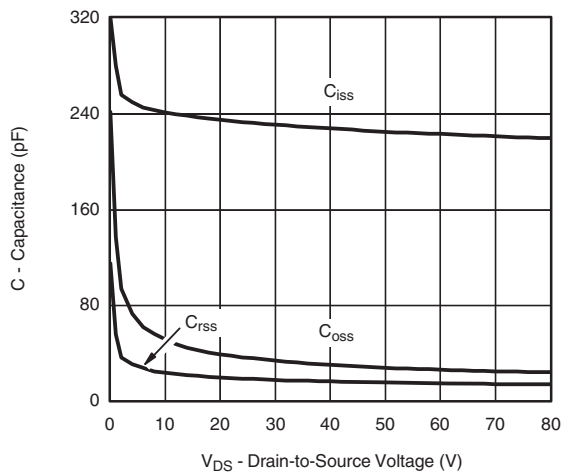
Transfer Characteristics



Source-Drain Diode Forward Voltage



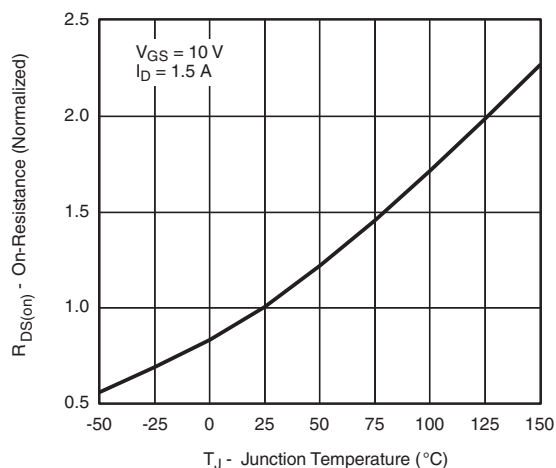
On-Resistance vs. Drain Current



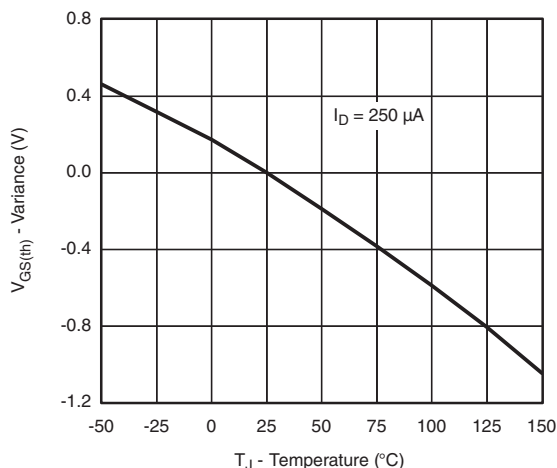
Capacitance



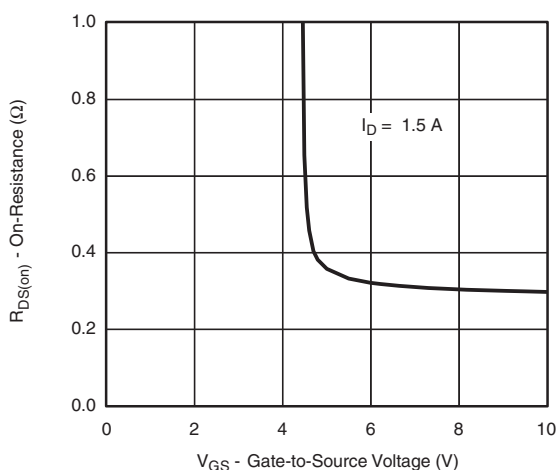
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



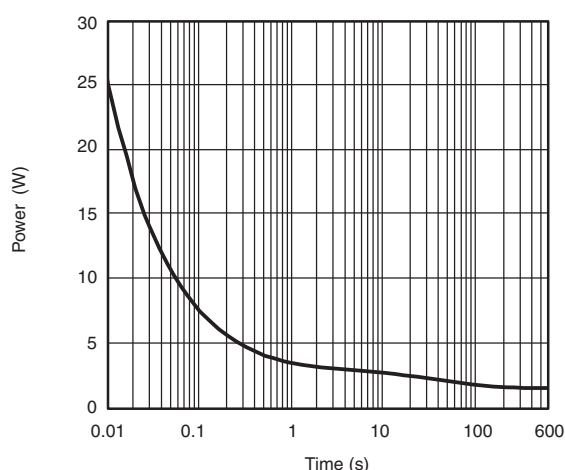
On-Resistance vs. Junction Temperature



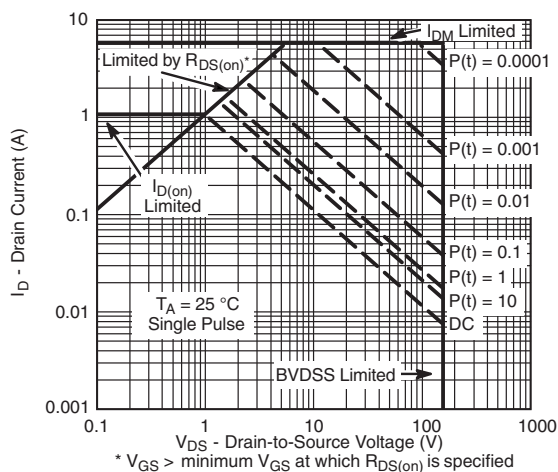
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



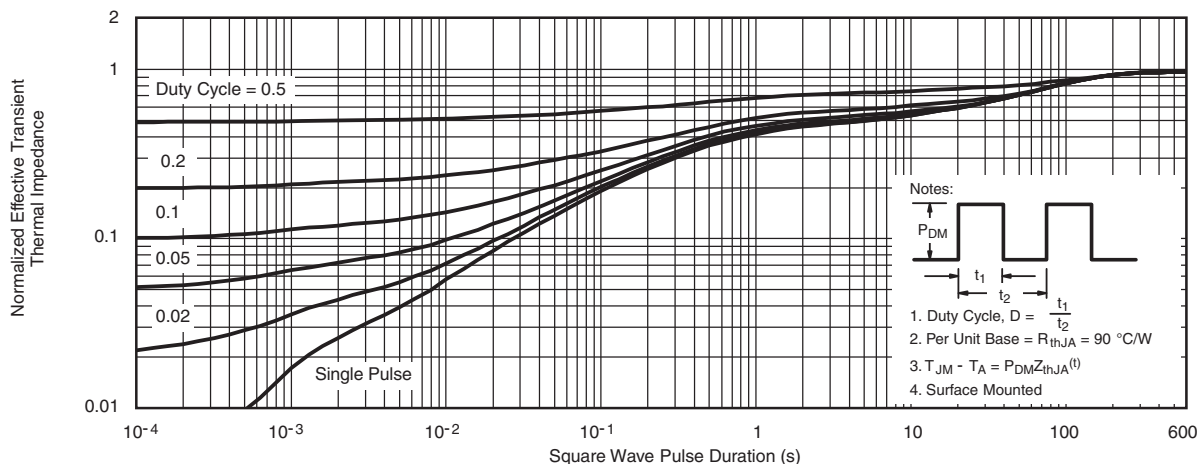
Single Pulse Power



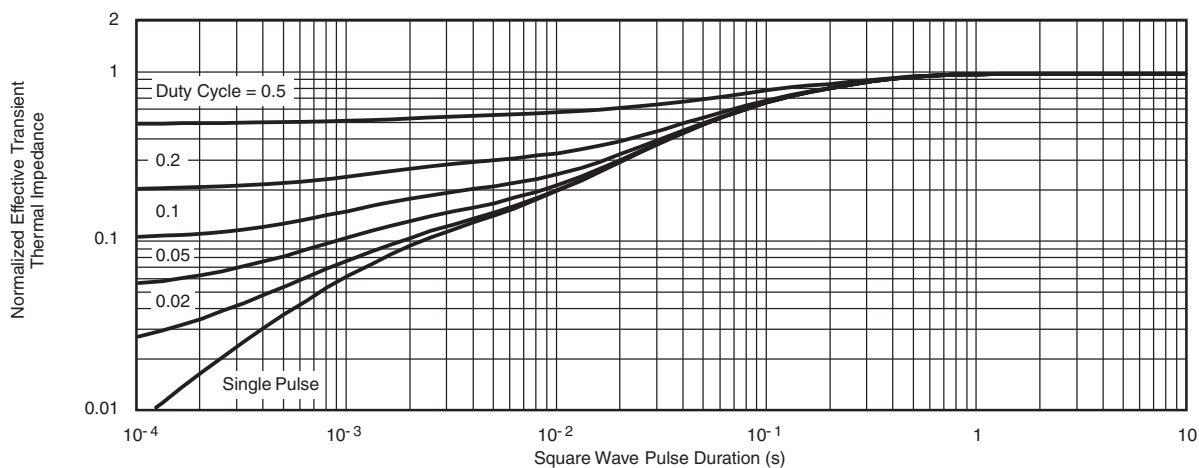
Safe Operating Area



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

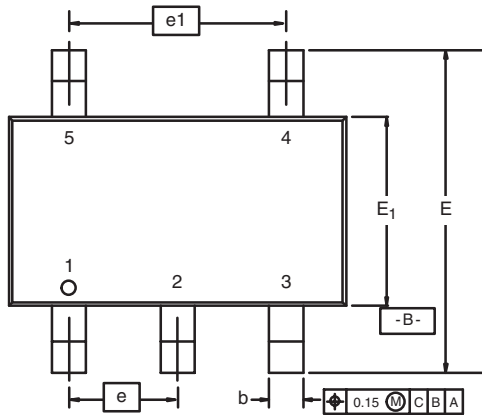


Normalized Thermal Transient Impedance, Junction-to-Foot

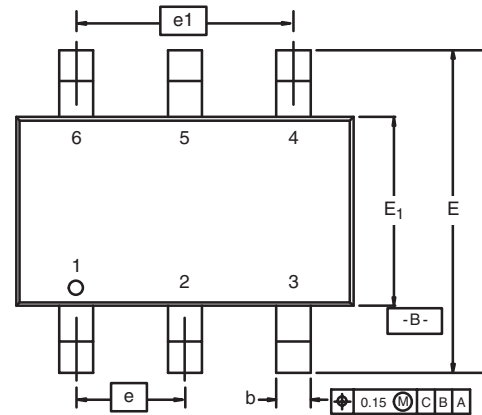
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?72380.

TSOP: 5/6-LEAD

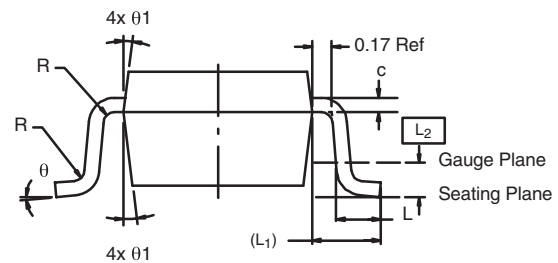
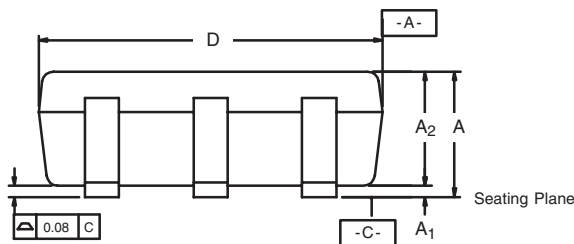
JEDEC Part Number: MO-193C



5-LEAD TSOP

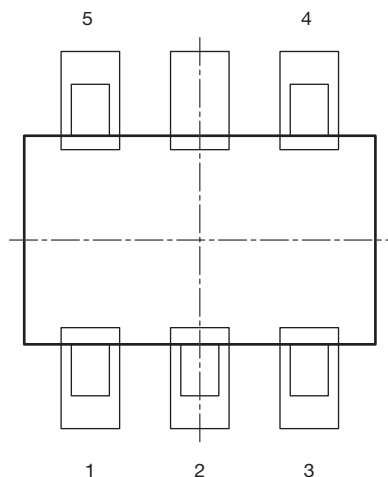


6-LEAD TSOP

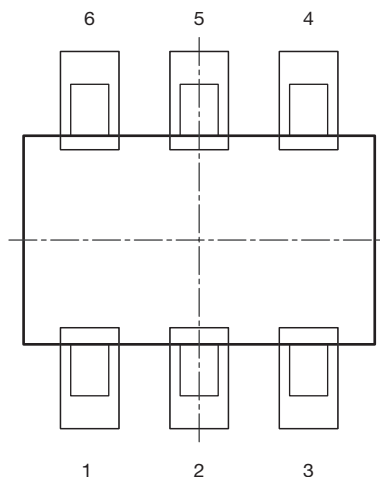


Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.91	-	1.10	0.036	-	0.043
A ₁	0.01	-	0.10	0.0004	-	0.004
A ₂	0.90	-	1.00	0.035	0.038	0.039
b	0.30	0.32	0.45	0.012	0.013	0.018
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	2.70	2.85	2.98	0.106	0.112	0.117
E ₁	1.55	1.65	1.70	0.061	0.065	0.067
e	0.95 BSC			0.0374 BSC		
e ₁	1.80	1.90	2.00	0.071	0.075	0.079
L	0.32	-	0.50	0.012	-	0.020
L ₁	0.60 Ref			0.024 Ref		
L ₂	0.25 BSC			0.010 BSC		
R	0.10	-	-	0.004	-	-
θ	0°	4°	8°	0°	4°	8°
θ ₁	7° Nom			7° Nom		
ECN: C-06593-Rev. I, 18-Dec-06						
DWG: 5540						

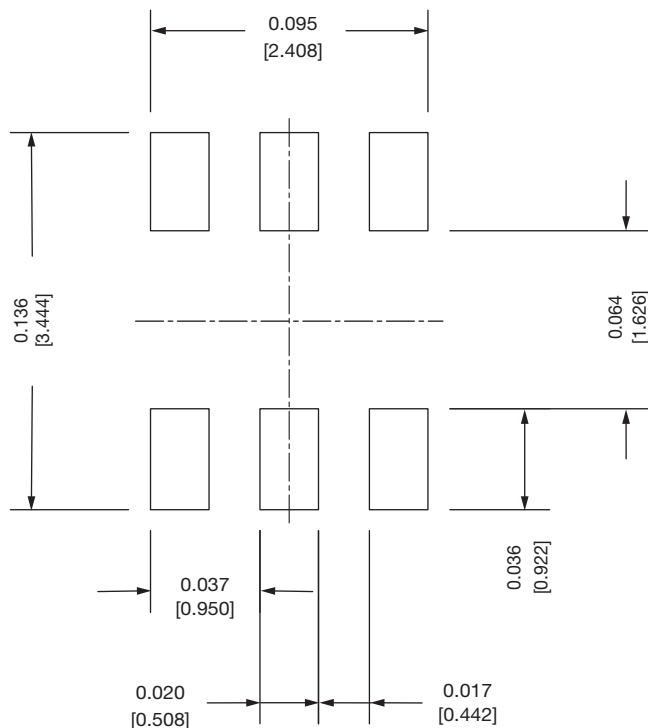
Recommended Land Pattern For TSOP-5L / TSOP-6L



TSOP 5L



TSOP 6L


Note

- All dimensions are in inches (millimeter)

ECN: C22-0860-Rev. B, 24-Oct-2022
DWG: 3010



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