

MOSFET – N-Channel, POWERTRENCH®

40 V, 14 A, 9.7 mΩ

FDMC8327L

General Description

This N-Channel MOSFET is produced using onsemi's advanced POWERTRENCH process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

Features

- Max $R_{DS(on)}$ = 9.7 mΩ at V_{GS} = 10 V, I_D = 12 A
- Max $R_{DS(on)}$ = 12.5 mΩ at V_{GS} = 4.5 V, I_D = 10 A
- Low Profile – 0.8 mm Max in Power 33
- 100% UIL Test
- This Device is Pb-Free, Halide Free and RoHS Compliant

Applications

- DC-DC Conversion

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

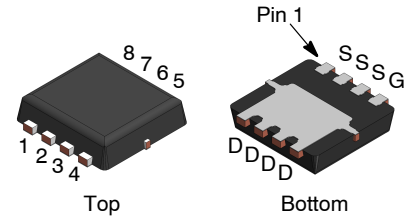
Symbol	Parameter	Value	Unit
V_{DS}	Drain to Source Voltage	40	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current – Continuous (Package Limited) $T_C = 25^\circ\text{C}$ – Continuous (Silicon Limited) $T_C = 25^\circ\text{C}$ – Continuous (Note 1a) $T_A = 25^\circ\text{C}$ – Pulsed	14 43 12 60	A
E_{AS}	Single Pulse Avalanche Energy (Note 3)	25	mJ
P_D	Power Dissipation Power Dissipation (Note 1a)	$T_C = 25^\circ\text{C}$ $T_A = 25^\circ\text{C}$ 30 2.3	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

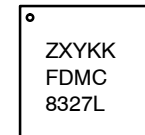
Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	4.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

V_{DS}	$R_{DS(on)}$ MAX	I_D MAX
40 V	9.7 mΩ @ 10 V	14 A
	12.5 mΩ @ 4.5 V	



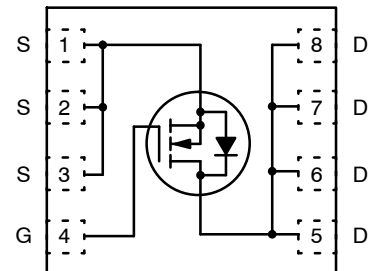
WDFN8 3.3x3.3, 0.65P
CASE 511DR

MARKING DIAGRAM



Z = Assembly Plant Code
XY = 2-Digit Date Code (Year and Week)
KK = 2-Digits Lot Run Traceability Code
FDMC8327L = Specific Device Code

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

FDMC8327L

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	40	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C	–	22	–	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 32 V, V _{GS} = 0 V	–	–	1	μA
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V	–	–	±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	1.0	1.7	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C	–	–5	–	mV/°C
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 12 A	–	7.4	9.7	mΩ
		V _{GS} = 4.5 V, I _D = 10 A	–	9.4	12.5	
		V _{GS} = 10 V, I _D = 12 A, T _J = 125°C	–	11	14.5	
g _{FS}	Forward Transconductance	V _{DD} = 5 V, I _D = 12 A	–	52	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 20 V, V _{GS} = 0 V, f = 1 MHz	–	1235	1850	pF
C _{oss}	Output Capacitance		–	347	520	pF
C _{rss}	Reverse Transfer Capacitance		–	21	35	pF
R _g	Gate Resistance		0.1	0.6	1.3	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 20 V, I _D = 12 A, V _{GS} = 10 V, R _{GEN} = 6 Ω	–	8.4	17	ns
t _r	Rise Time		–	2.2	10	ns
t _{d(off)}	Turn-Off Delay Time		–	20	32	ns
t _f	Fall Time		–	2.2	10	ns
Q _{g(TOT)}	Total Gate Charge	V _{GS} = 0 V to 10 V, V _{DD} = 20 V, I _D = 12 A	–	18.5	26	nC
		V _{GS} = 0 V to 5 V, V _{DD} = 20 V, I _D = 12 A	–	9.7	14	
Q _{gs}	Gate to Source Charge	V _{DD} = 20 V, I _D = 12 A	–	3.3	–	nC
Q _{gd}	Gate to Drain “Miller” Charge		–	2.6	–	nC

DRAIN-SOURCE DIODE CHARACTERISTICS

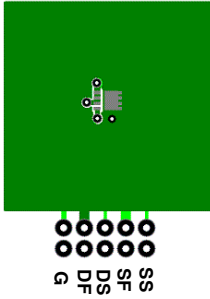
V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = 1.8 A (Note 2)	–	0.7	1.2	V
		V _{GS} = 0 V, I _S = 12 A (Note 2)	–	0.8	1.3	
t _{rr}	Reverse Recovery Time	I _F = 12 A, di/dt = 100 A/s	–	32	51	ns
Q _{rr}	Reverse Recovery Charge		–	10	20	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

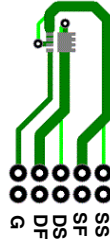
FDMC8327L

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 53°C/W when mounted
on a 1 in² pad of 2 oz copper



b) 125°C/W when mounted
on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μ s, Duty Cycle < 2.0%.
3. Starting $T_J = 25^\circ\text{C}$; N-ch: $L = 0.3 \text{ mH}$, $I_{AS} = 13 \text{ A}$, $V_{DD} = 36 \text{ V}$, $V_{GS} = 10 \text{ V}$.

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

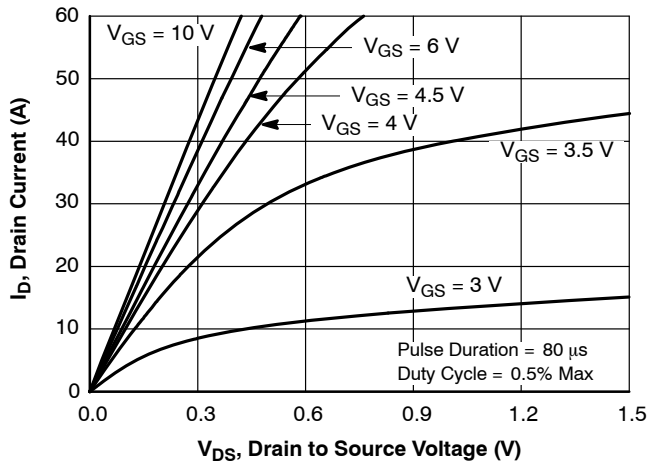


Figure 1. On Region Characteristics

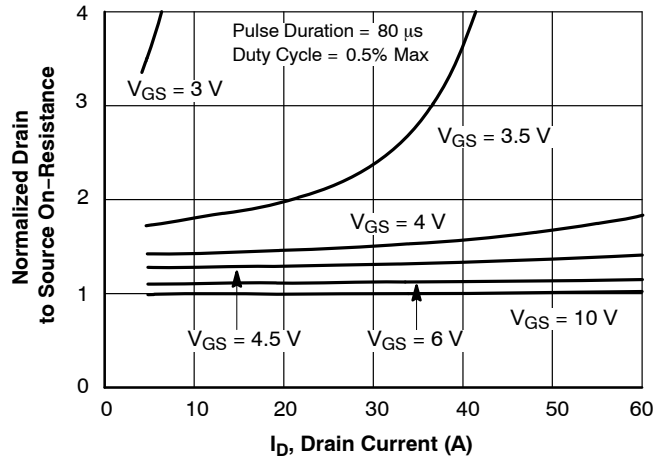


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

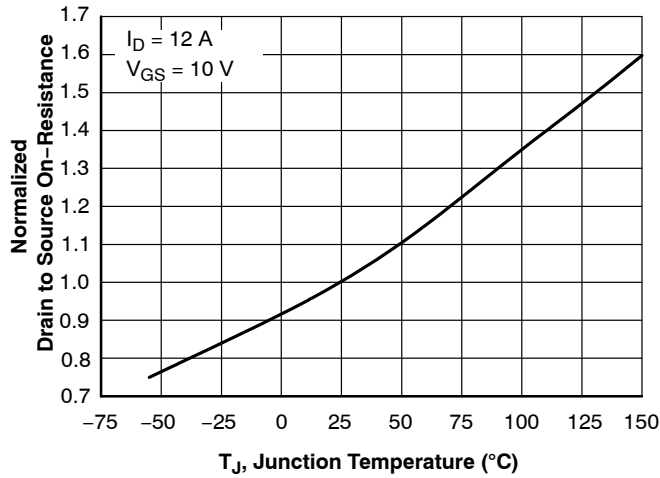


Figure 3. Normalized On Resistance vs. Junction Temperature

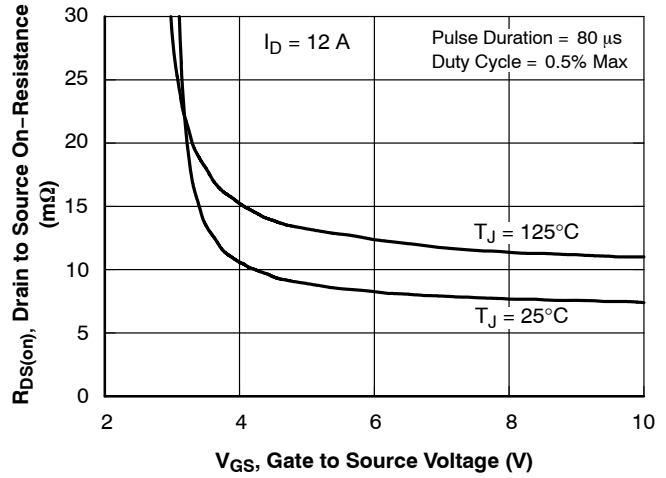


Figure 4. On-Resistance vs. Gate to Source Voltage

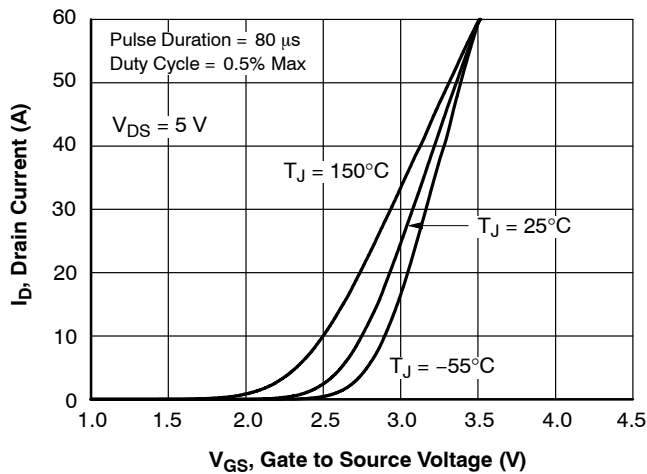


Figure 5. Transfer Characteristics

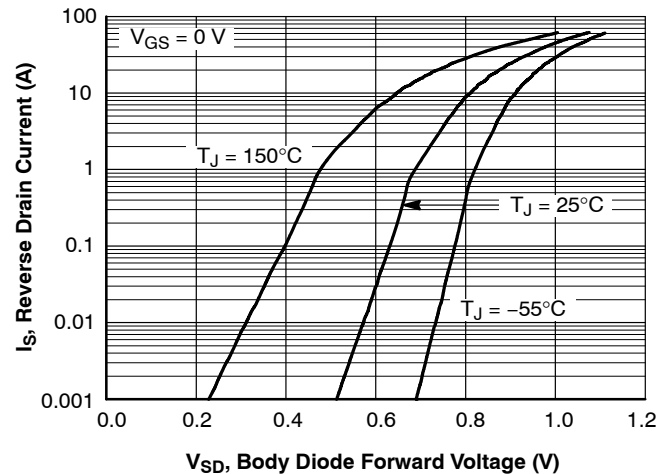


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

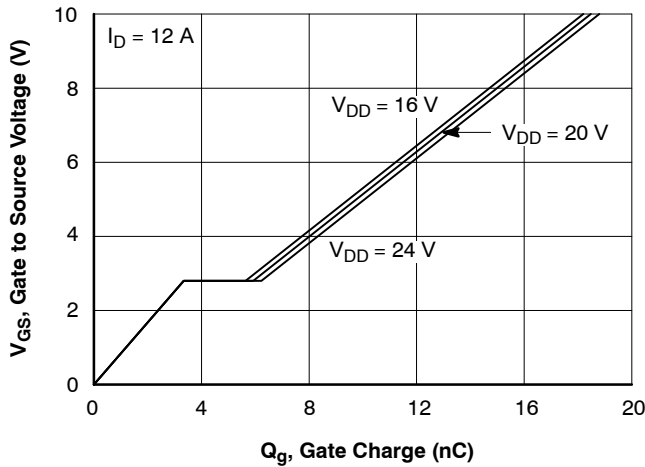


Figure 7. Gate Charge Characteristics

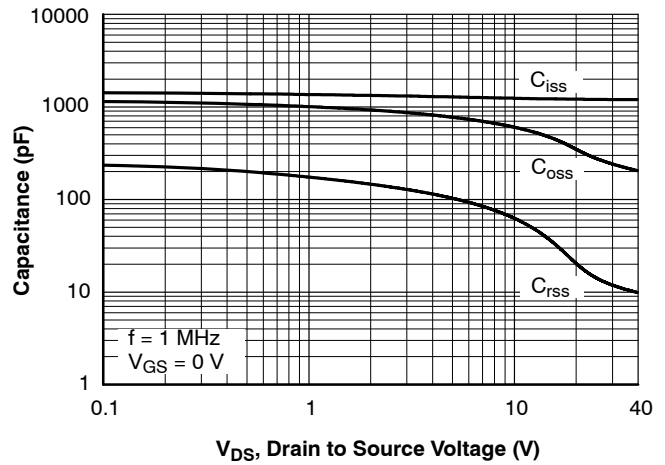


Figure 8. Capacitance vs. Drain to Source Voltage

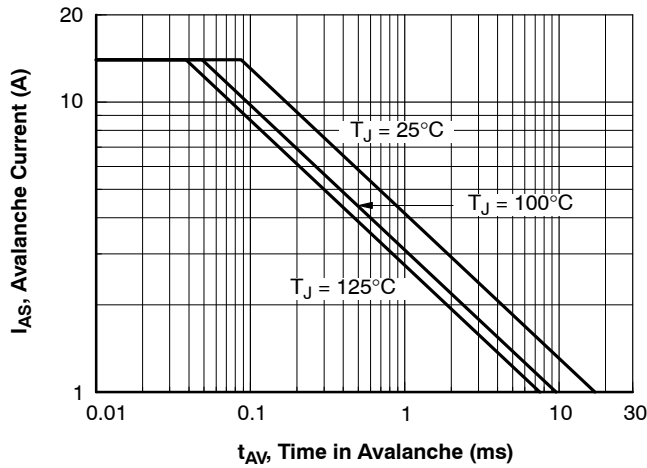


Figure 9. Unclamped Inductive Switching Capability

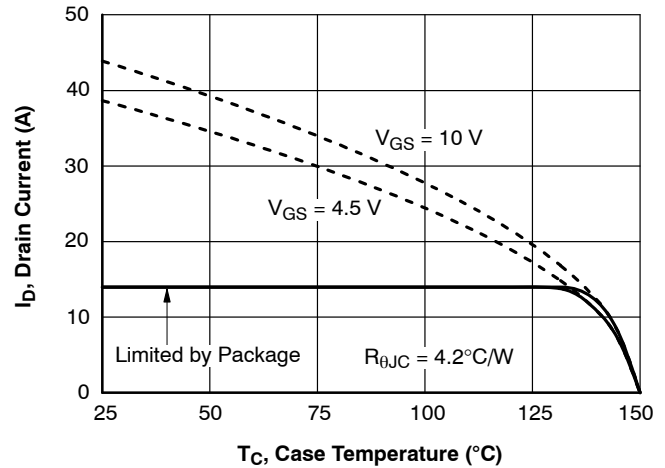


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

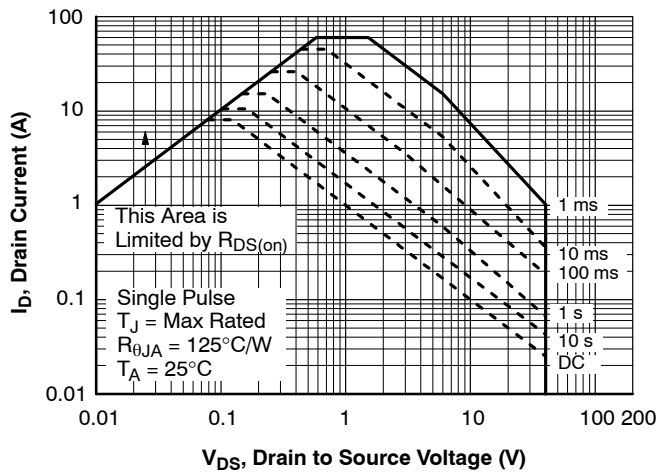


Figure 11. Forward Bias Safe Operating Area

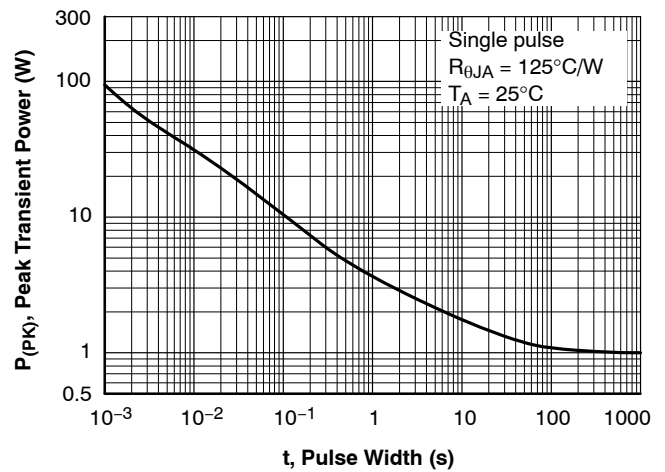


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

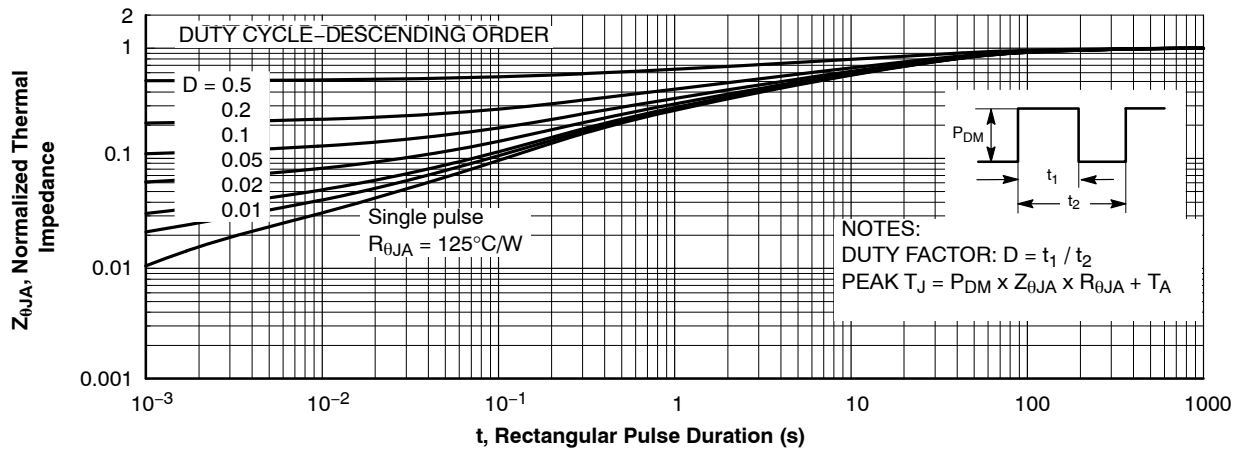
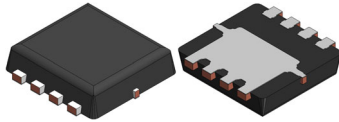


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

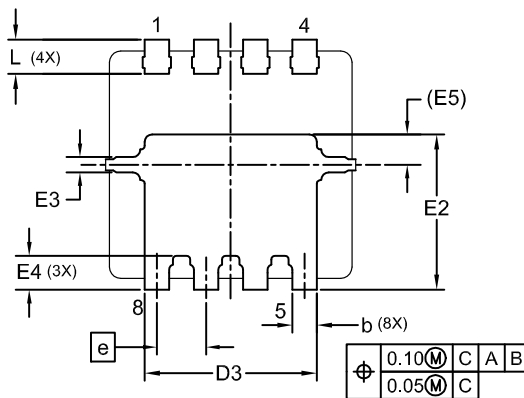
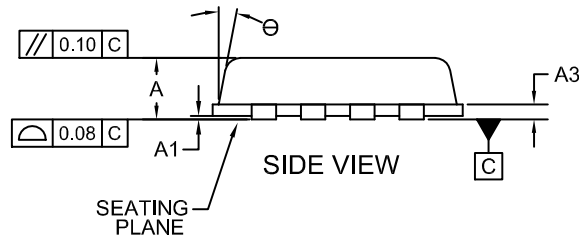
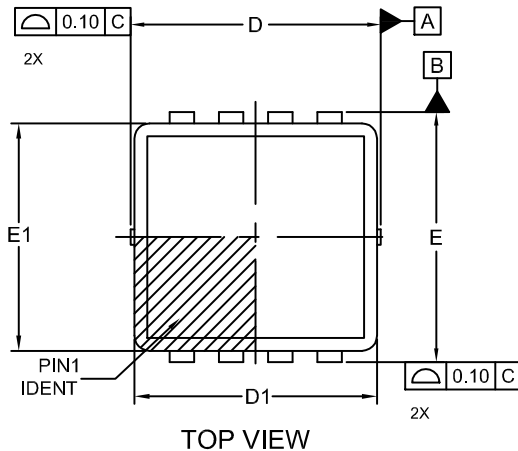
PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package Type	Reel Size	Tape Width	Shipping [†]
FDMC8327L	FDMC8327L	WDFN8 3.3x3.3, 0.65P (Pb-Free)	13"	12 mm	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

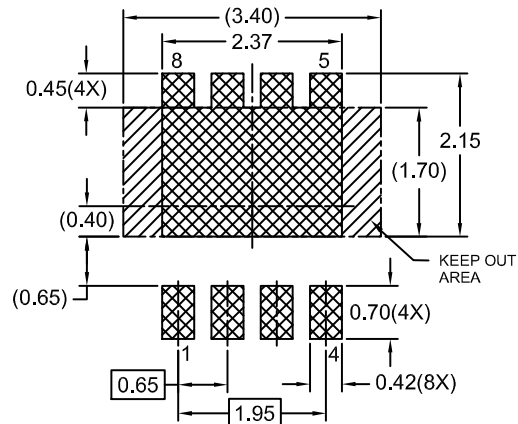

WDFN8 3.3x3.3, 0.65P
CASE 511DR
ISSUE B

DATE 02 FEB 2022

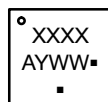

NOTES:

- A. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
B. SEATING PLANE IS DEFINED BY TERMINAL TIPS ONLY
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH PROTRUSIONS NOR GATE BURRS. MOLD FLASH PROTRUSION OR GATE BURR DOES NOT EXCEED 0.150MM.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.15	0.20	0.25
b	0.27	0.32	0.37
D	3.20	3.30	3.40
D1	3.10	3.20	3.30
D3	2.17	2.27	2.37
E	3.20	3.30	3.40
E1	2.90	3.00	3.10
E2	1.95	2.05	2.15
E3	0.15	0.20	0.25
E4	0.30	0.40	0.50
E5	0.40 REF		
e	0.65 BSC		
L	0.30	0.40	0.50
Θ	0°	-	12°


RECOMMENDED LAND PATTERN

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*


XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	WDFN8 3.3x3.3, 0.65P	PAGE 1 OF 1

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