# TLV7081 Nano-Power, 4-Bump WCSP, Small-Size Comparator

## 1 Features

- Wide Supply Voltage Range: 1.7 V to 5.5 V
- Quiescent Supply Current of 370 nA
- Low Propagation Delay of 4 µs
- Open-Drain Output
- Independent Input Voltage Range up to 5.6 V
- Internal Hysteresis: 10 mV
- Temperature Range: –40°C to +125°C
- Package:
  – 0.7 mm × 0.7 mm WCSP (4)

## 2 Applications

- Smartphones
- Notebook PCs and Tablets
- Optical Modules
- Digital Cameras
- Relays and Circuit Breakers
- Portable Medical Devices
- Door and Window Sensors
- Video Game Controllers

## 3 Description

The TLV7081 is a single-channel, nano-power comparator that operates down to 1.7 V. The comparator is available in an ultra-small, WCSP package measuring 0.7 mm × 0.7 mm, making the TLV7081 applicable for space-critical designs like smartphones and other portable or battery-powered applications.

The TLV7081 features a wide input-voltage range that is independent of supply voltage. Having an input range that is independent of supply voltage allows the TLV7081 to be directly connected to sources that are active even if the TLV7081 is not powered.

The TLV7081 has an open-drain output stage that can be pulled beyond V+, making it appropriate for level translators and bipolar to single-ended converters.

**Device Information (1)**

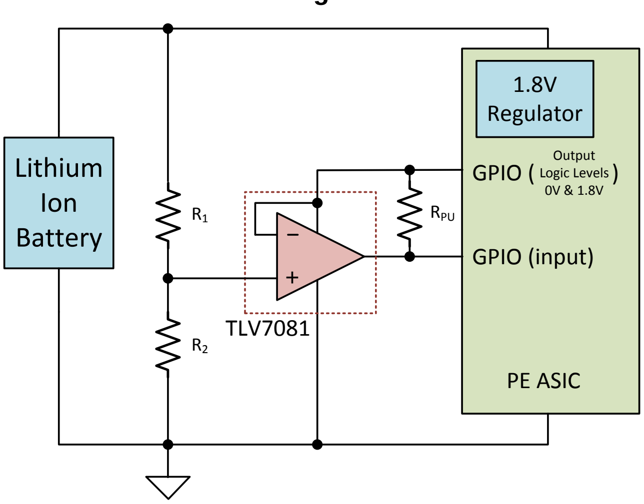
| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| TLV7081 | WCSP (4) | 0.7 mm × 0.7 mm |

**Small-Size, Low-Power Comparator Family**

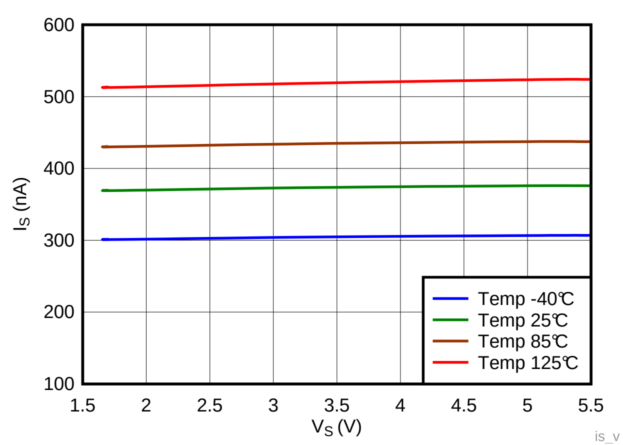
| FAMILY | $I_Q$ PER CHAN | $t_{PD}$ | Output Type | Package |
|---|---|---|---|---|
| TLV7081 | 370 nA | 4 µs | Open-Drain | WCSP |
| TLV7031 | 335 nA | 3 µs | Push-Pull | X2SON |
| TLV7041 | 335 nA | 3 µs | Open-Drain | X2SON |
| TLV7011 | 5 µA | 260 ns | Push-Pull | X2SON |
| TLV7021 | 5 µA | 260 ns | Open-Drain | X2SON |

(1) For all available packages, see the package option addendum at the end of the datasheet.

**UnderVoltage Detection**




**$I_S$ vs. Supply Voltage**



# Table of Contents



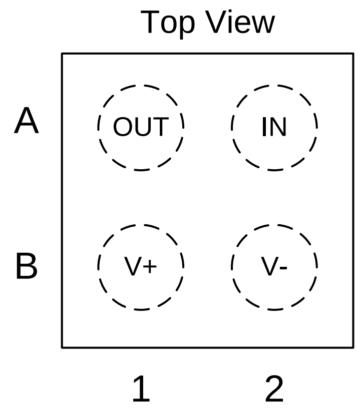
## 4 Revision History

**Changes from Original (December 2017) to Revision A** — **Page**

- Changed Advance Information to Production Data ... 1
- Added note to the *Timing Diagrams* section ... 6

# 5 Pin Configuration and Functions

**YKA Package**
**4-Bump DSBGA**
**Top View**




**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | Number | | |
| OUT | A1 | O | Comparator output: OUT is open-drain. |
| V+ | B1 | P | Positive (highest) power supply; functions as an external reference voltage |
| V– | B2 | P | Negative (lowest) power supply |
| IN | A2 | I | Comparator input: IN is the noninverting input |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

| | MIN | MAX | UNIT |
|---|---|---|---|
| Supply voltage $V_S$ = (V+) - (V-) | – 0.3 | 6 | V |
| Input (IN) to (V–)[2] | – 0.3 | 6 | V |
| Current into input (IN) | | ±10 | mA |
| Output (OUT) to (V–) | – 0.3 | 6 | V |
| Output short-circuit duration[3] | | 10 | s |
| Junction temperature, $T_J$ | | 150 | °C |
| Storage temperature, $T_{stg}$ | – 65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input signals that can swing more than 0.3 V below (V–) must be current-limited to 10 mA or less.
(3) Short-circuit to ground, one comparator per package.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | ±1500 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101[2] | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | MIN | MAX | UNIT |
|---|---|---|---|
| Supply voltage $V_S$ = (V+) - (V-) | 1.7 | 5.5 | V |
| Open-Drain PULL-UP voltage $V_{PULL-UP}$ | | 5.5 | V |
| Ambient temperature, $T_A$ | –40 | 125 | °C |

## 6.4 Thermal Information

| THERMAL METRIC[1] | | TLV7081 YKA (DSBGA) 4 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 207 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 1.8 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 73.2 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 1 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 73.3 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 6.5 Electrical Characteristics

Over the operating temperature range of $T_A$ = –40°C to +125°C, $V_S$ = 3.3 V, and $V_{PULL\text{-}UP}$ = V+ (unless otherwise noted). Typical values are at $T_A$ = 25°C. Voltage at input pin (IN) is referenced to (V-).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IO}$ | Input Offset Voltage | $V_S$ = 1.8 V and 3.3 V, $T_A$ = –40°C to +125°C | –10 | ±1 | 10 | mV |
| $dV_{IO}/dT$ | Input Offset Voltage Drift | $T_A$ = –40°C to +125°C | | ±3 | | µV/℃ |
| $V_{HYS}$ | Input Hysteresis Voltage | | | 10 | | mV |
| $V_{IN}$ | Input Voltage Range (1) | | 0 | | 5.6 | V |
| $I_{BIAS}$ | Input bias current | IN = 5.6 V, positive value means current entering pin (IN) | | 3 | | pA |
| $I_{LEAK}$ | Input leakage current | IN = 5.6 V, $V_S$ = 0 V, positive value means current entering pin (IN) | | 4 | | pA |
| $C_I$ | Input Capacitance | | | 1.9 | | pF |
| $V_{OL}$ | Low-Level Output Voltage | Sinking 200 µA, measured relative to (V-) | | | 0.1 | V |
| | | Sinking 2 mA, measured relative to (V-) | | | 0.4 | V |
| $I_{O\text{-}SC}$ | Short-circuit sink current | $V_S$ = 5 V | | 45 | | mA |
| $I_{O\text{-}LKG}$ | Output Leakage Current | IN = (V+) + 0.1V (output high), $V_{PULL\text{-}UP}$ = (V+) | | 130 | | pA |
| PSRR | Power Supply Rejection Ratio | $V_S$ = 1.8 V to 5 V | | 75 | | dB |
| $I_S$ | Supply Current | no load, IN = (V+) – 0.1V (output low), $T_A$ = 25°C | | 370 | 470 | nA |
| | | no load, IN = (V+) – 0.1V (output low), $T_A$ = –40°C to +125°C | | | 630 | nA |

(1) Over Operating Supply Voltage Range ($V_s$): 1.7 V to 5.5 V

## 6.6 Switching Characteristics

Typical values are at $T_A$ = 25°C, $V_S$ = 3.3 V; $C_L$ = 15 pF, (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PHL}$ | High-to-low propagation delay (1) | Input overdrive = –100 mV | | 4 | | µs |
| $t_{PLH}$ | Low-to-high propagation delay (1) | Input overdrive = +100 mV, $R_{PULL\text{-}UP}$ = 4.99 kΩ | | 4 | | µs |
| $t_F$ | Output fall time | Measured from 20% to 80% | | 7 | | ns |
| $t_{ON}$ | Start-up delay (2) | | | 1 | | ms |

(1) High-to-low and low-to-high refers to the transition at the input pin (IN).
(2) During power on, $V_S$ must exceed 1.7 V for 1 ms before the output is in a correct state.

## 6.7 Timing Diagrams

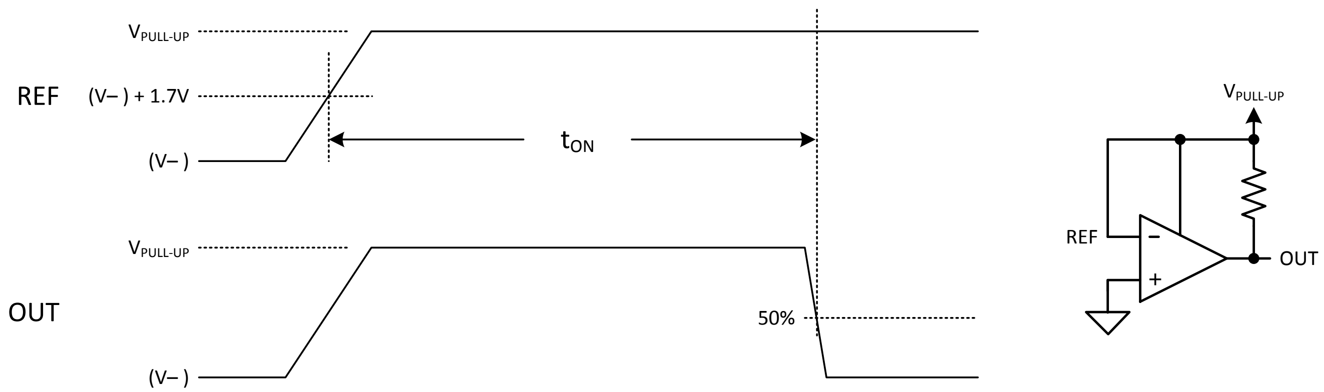



**Figure 1. Start-up Delay**

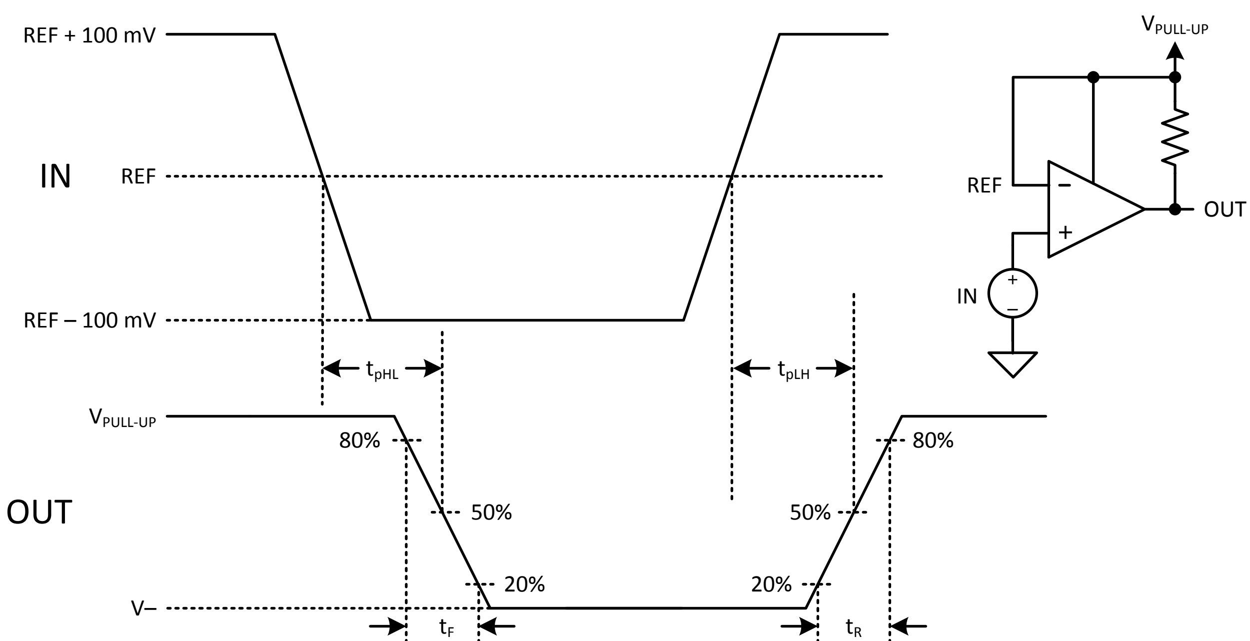



**Figure 2. Timing Diagram**

---

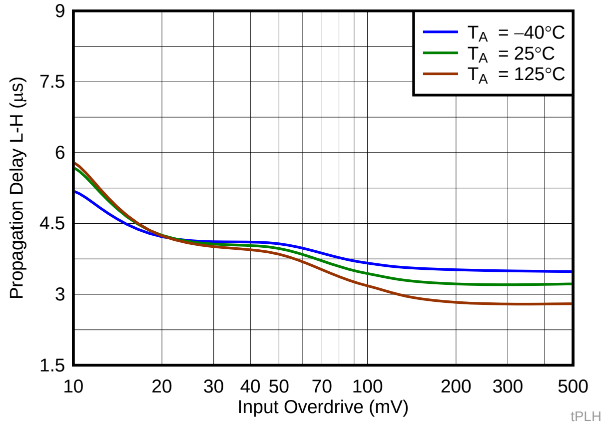
**NOTE**

The propagation delays $t_{pLH}$ and $t_{pHL}$ include the contribution of input offset and hysteresis.

---

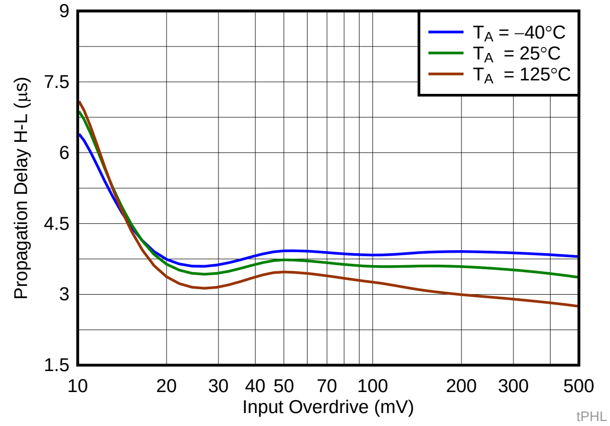
## 6.8 Typical Characteristics

$T_A$ = 25°C, $V_S$ = 3.3 V, $R_{PULL\text{-}UP}$ = 4.99 kΩ, $C_L$ = 15 pF



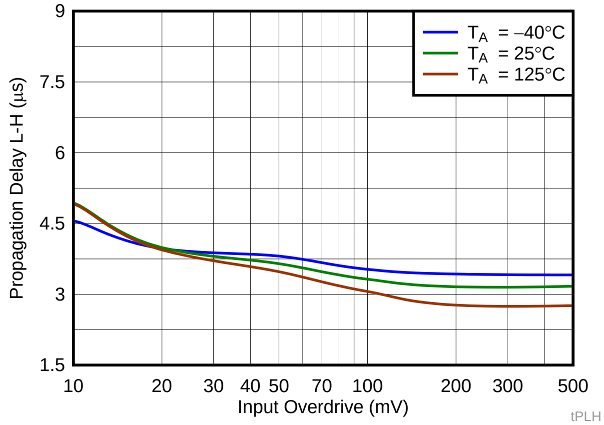

$V_S$ = 1.8 V

**Figure 3. Propagation Delay (L-H) vs. Input Overdrive**



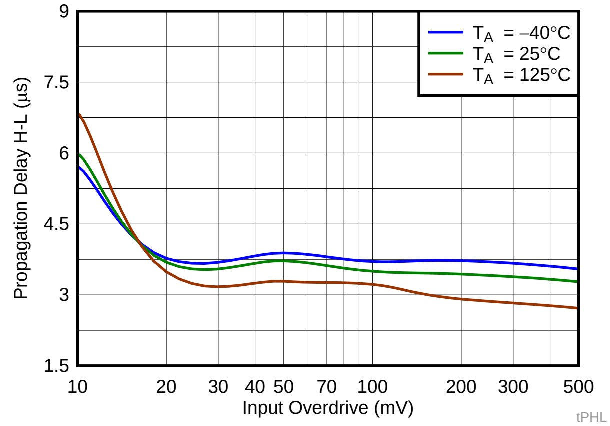

$V_S$ = 1.8 V

**Figure 4. Propagation Delay (H-L) vs. Input Overdrive**



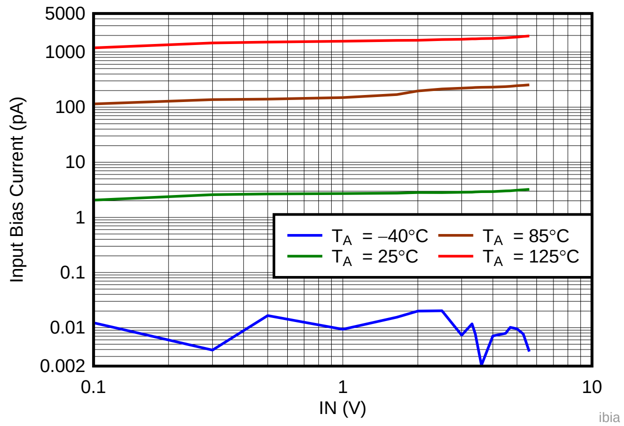

$V_S$ = 3.3 V

**Figure 5. Propagation Delay (L-H) vs. Input Overdrive**




$V_S$ = 3.3 V

**Figure 6. Propagation Delay (H-L) vs. Input Overdrive**




$V_S$ = 3.3 V

**Figure 7. Input Bias Current vs. IN**

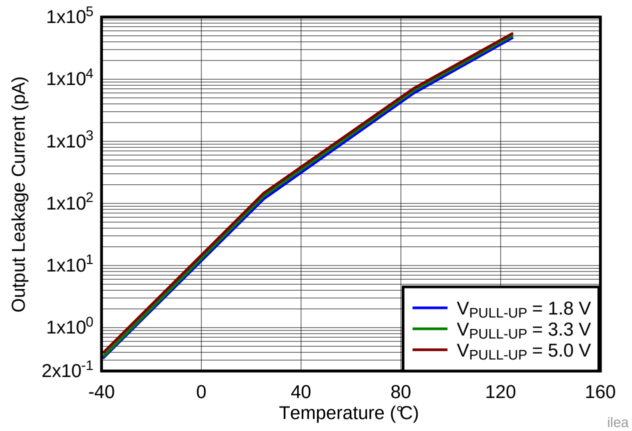
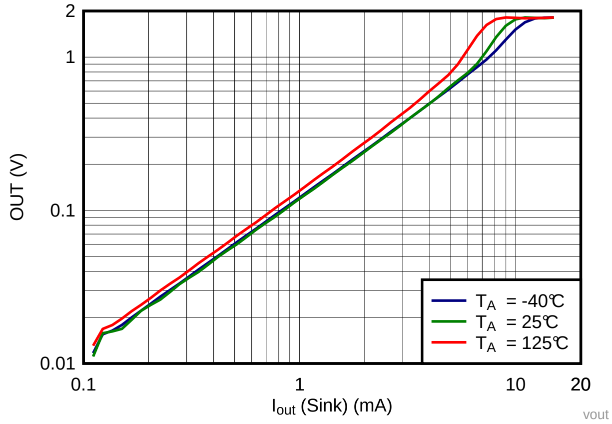



**Figure 8. Output Leakage Current vs. Temperature**

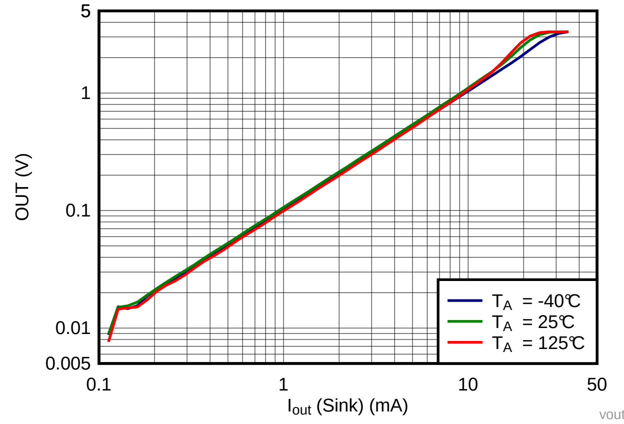
## Typical Characteristics (continued)

$T_A$ = 25°C, $V_S$ = 3.3 V, $R_{PULL-UP}$ = 4.99 kΩ, $C_L$ = 15 pF



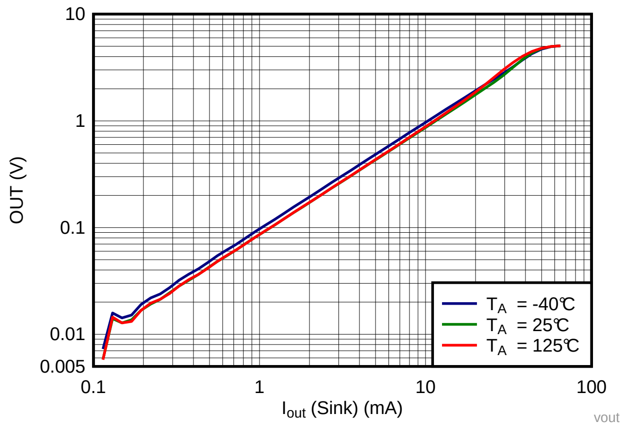

$V_S$ = 1.8 V

**Figure 9. Output Voltage Low vs. Output Sink Current**




$V_S$ = 3.3 V

**Figure 10. Output Voltage Low vs. Output Sink Current**




$V_S$ = 5 V

**Figure 11. Output Voltage Low vs. Output Sink Current**

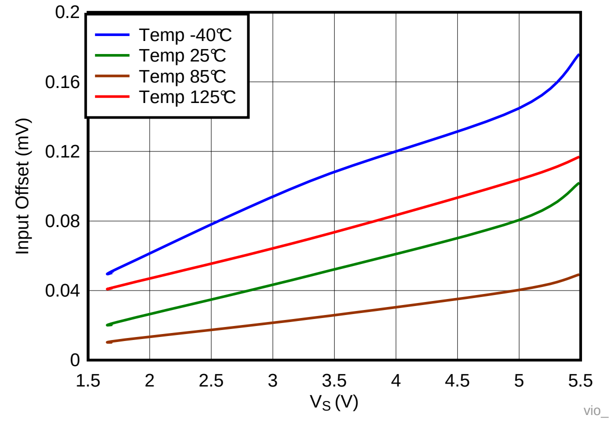



**Figure 12. Input Offset vs. $V_S$**

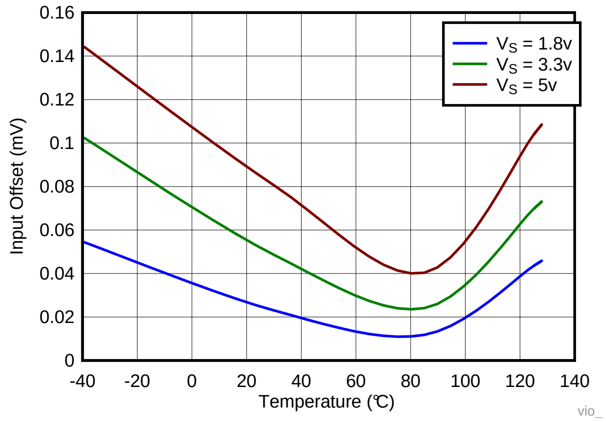



**Figure 13. Input Offset vs. Temperature**

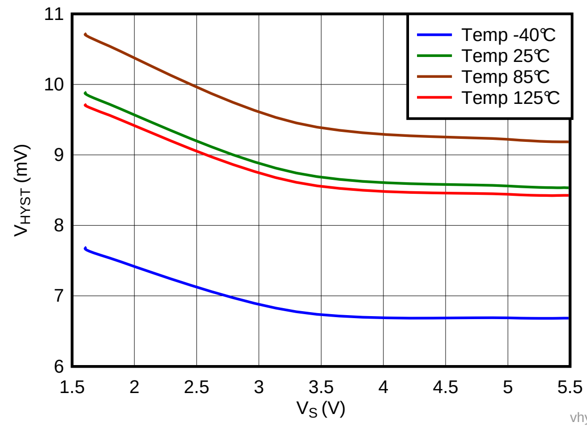



**Figure 14. Hysteresis vs $V_S$**

## Typical Characteristics (continued)

$T_A$ = 25°C, $V_S$ = 3.3 V, $R_{PULL-UP}$ = 4.99 kΩ, $C_L$ = 15 pF

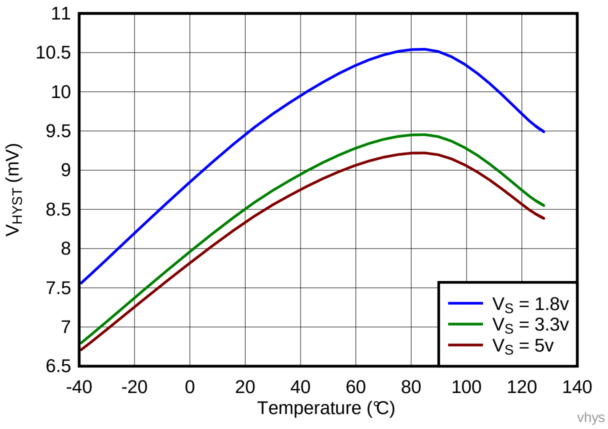
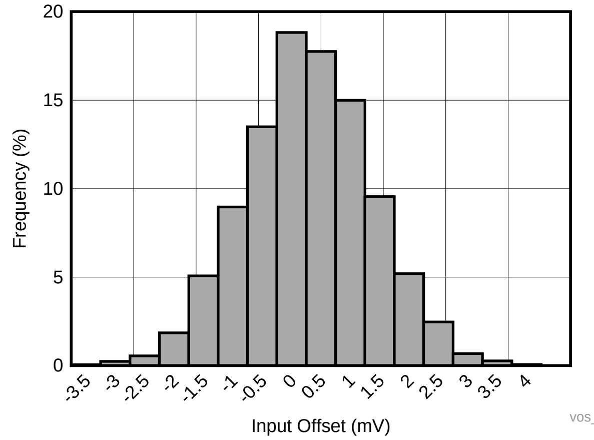
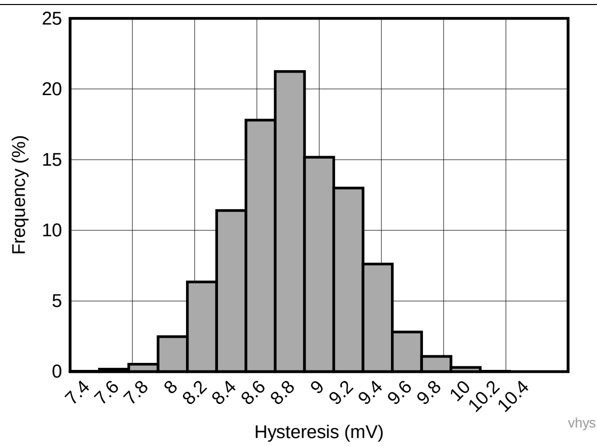



Figure 15. Hysteresis vs. Temperature



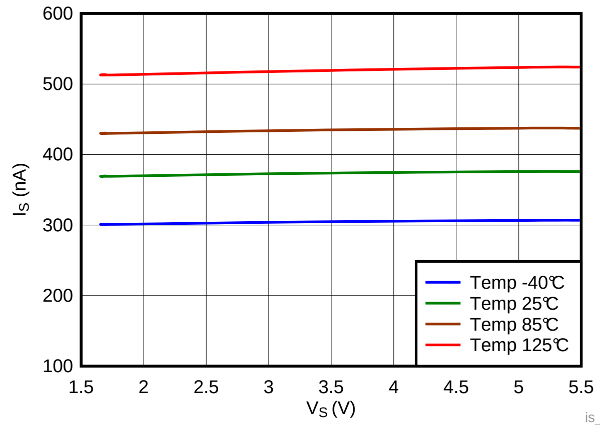

Distribution Taken from 7,990 Comparators

Figure 16. Input Offset Histogram



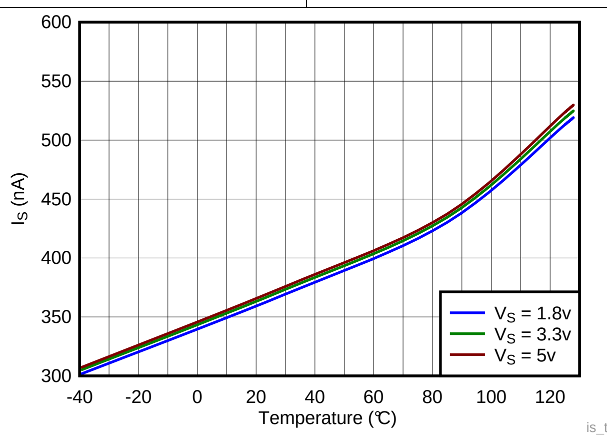

Distribution Taken from 7,990 Comparators

Figure 17. Hysteresis Histogram




IN = (V+) - 0.1V (output low), No load.

Figure 18. Supply Current vs. $V_S$




IN = (V+) - 0.1V (output low), No load.

Figure 19. Supply Current vs. Temperature

# 7 Detailed Description

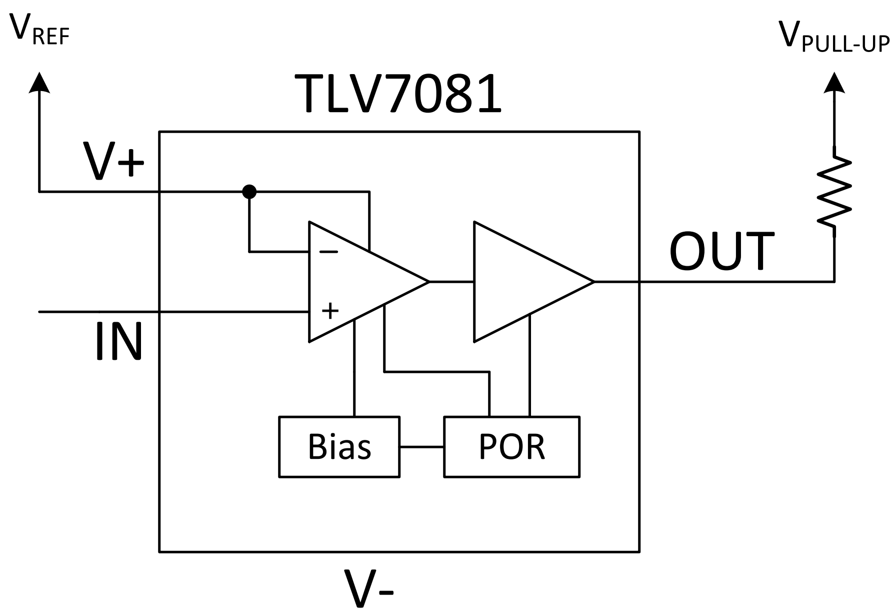
## 7.1 Overview

The TLV7081 is a single-channel, nano-power comparator that does not need a dedicated power supply connection, and can operate down to 1.7 V. The comparator is available in an ultra-small, WCSP package measuring 0.7 mm × 0.7 mm, making the TLV7081 applicable for space-critical designs like smartphones and other portable or battery-powered applications.

The TLV7081 features a wide input-voltage range that is independent of supply voltage. Having an input range that is independent of supply voltage allows the TLV7081 to be directly connected to sources that are active even if the TLV7081 is not powered.

The TLV7081 has an open-drain output stage that can be pulled beyond V+, making it appropriate for level translators and bipolar to single-ended converters.

## 7.2 Functional Block Diagram




## 7.3 Feature Description

The TLV7081 is a single-channel, nano-power comparator that operates down to 1.7 V. The inverting input is internally tied to V+ which helps to streamline applications which use supply as the reference. The non-inverting input IN extends to 5.6 V which is independent of the power supply V+ (1.7 V - 5.5 V) and it's available in an ultra-small, WCSP package measuring 0.7 mm × 0.7 mm.

## 7.4 Device Functional Modes

The TLV7081 has a power-on-reset (POR) circuit. While the power supply ($V_S$) is greater than $V_{POR}$ (typically 1V) and less than the minimum operating supply voltage, either upon ramp-up or ramp-down, the POR circuitry is activated.

The POR circuit keeps the output high impedance (logical high) while activated.

When the supply voltage is greater than, or equal to, the minimum supply voltage, the comparator output reflects the state of the input IN.

## Device Functional Modes (continued)

### 7.4.1 Inputs

The TLV7081 input extends from V- to 5.6 V which is independent of supply. The input IN can be any voltage within these limits and no phase inversion of the comparator output occurs.

The input of TLV7081 is fault tolerant. It maintains the same high input impedance when V+ is unpowered or ramping up. The input can be safely driven up to the specified maximum voltage (5.6 V) with V+ = 0 V or any value up to the maximum specified.

The input bias current is typically 3 pA for input IN voltages between 0 and 5.6 V. The comparator inputs are protected from undervoltage by internal diodes connected to V-. As the input voltage goes under V-, the protection diodes become forward biased and begin to conduct causing the input bias current to increase exponentially. Input bias current typically doubles for every 10°C temperature increase.

### 7.4.2 Internal Hysteresis

The device hysteresis transfer curve is shown in Figure 20. This curve is a function of three components: $V_{TH}$, $V_{OS}$, and $V_{HYST}$:

- $V_{TH}$ is the actual set voltage or threshold trip voltage.
- $V_{OS}$ is the internal offset voltage between IN and V+. This voltage is added to $V_{TH}$ to form the actual trip point at which the comparator must respond to change output states.
- $V_{HYST}$ is the internal hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise (10 mV typical).

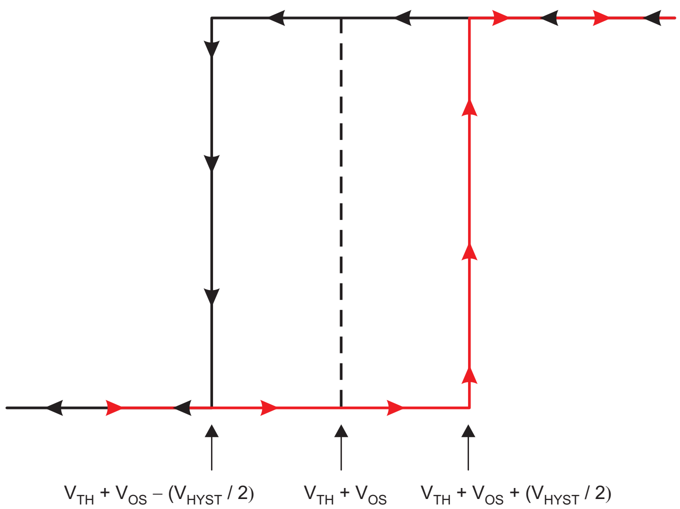



**Figure 20. Hysteresis Transfer Curve**

### 7.4.3 Output

The TLV7081 features an open-drain output stage enabling the output logic levels to be pulled up to an external source up to 5.5 V independently of the supply voltage.

# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The TLV7081 is a 4-pin, nano-power comparator with open-drain output that is well suited for monitoring battery voltages. The TLV7081's benefits include a small package footprint and a unique input stage that allows the comparator input to be driven by a voltage source even when the operating voltage for the comparator is turned-off (zero volts).

## 8.2 Typical Applications

### 8.2.1 Nano-Power Battery Monitor

The application of the TLV7081 for an under-voltage detection circuit is shown in Figure 21.

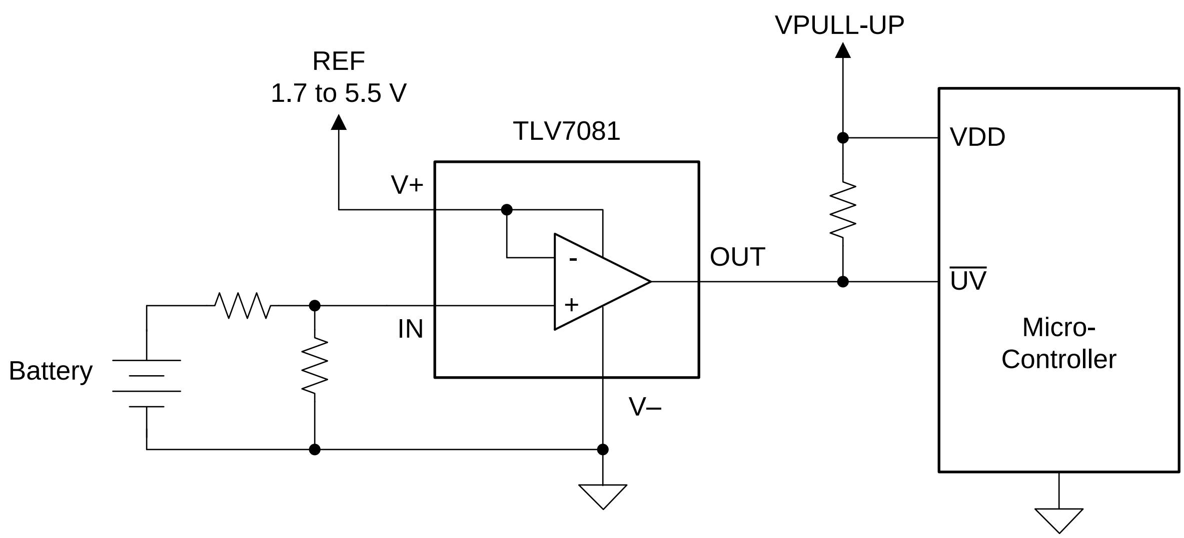





**Figure 21. Under-Voltage Detection**

#### *8.2.1.1 Design Requirements*

For this design, follow these design requirements:

- The supply voltage connected to pin (V+) serves as the reference voltage for the comparator and can be any voltage between 1.7 V and 5.5 V.
- The voltage applied to the input pin (IN) can be any voltage in the range of 0 V to 5.6 V. This voltage range is uniquely independent of the supply voltage applied to pin (V+).
- The comparator output pin (OUT) requires a pull-up resistor that sets the output-high logic level ($V_{OH}$) for the comparator. $V_{PULL-UP}$ should be connected to the supply voltage of the microcontroller which is monitoring the comparator output and serves as the level-shifting block for the logic levels in the application.

## Typical Applications (continued)

#### 8.2.1.2 Detailed Design Procedure

Instead of being powered directly from the battery, the TLV7081 is powered directly from a voltage reference that exists in the system. The input to the comparator (IN) is allowed to operate above and below the reference voltage due to the unique analog front end of the TLV7081. When the battery voltage is above the reference threshold, the output of the comparator is high and when the battery drops below the threshold of the reference, the output of the comparator goes low (see Figure 22 for details). For simplicity, the integrated hysteresis of the comparator is not shown in the timing diagram. Integrated hysteresis is helpful in avoiding glitches at the comparator output when operating in noisy environments or when the input voltage changes thresholds very slowly. An open-drain output configuration allows the output logic level of the comparator to be level-shifted to match the logic level of the receiving device.

#### 8.2.1.3 Application Curve

When the voltage applied to the input pin (IN) falls below the reference threshold (REF), the output pin (OUT) is pulled low to ground (V-). Moreover, when the input voltage rises above REF, the output of the comparator goes into a high impedance state and the OUT pin is pulled high by the pull-up resistor and $V_{PULL-UP}$ supply voltage.

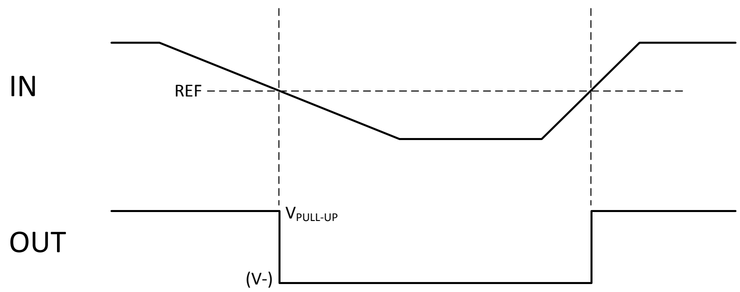



**Figure 22. Under-Voltage Timing Results**

### 8.2.2 Battery Monitoring in Portable Electronics

A recommended circuit diagram for monitoring a battery voltage in a personal electronic device is shown in Figure 23. In this diagram, the GPIO pin of an application specific integrated circuit (ASIC) serves as the supply voltage and the voltage reference for the TLV7081. Using a GPIO pin to power the TLV7081 is possible because of the low quiescent current of the TLV7081. In systems where power consumption needs to be further reduced, the GPIO pin can be used to power-cycle the TLV7081.

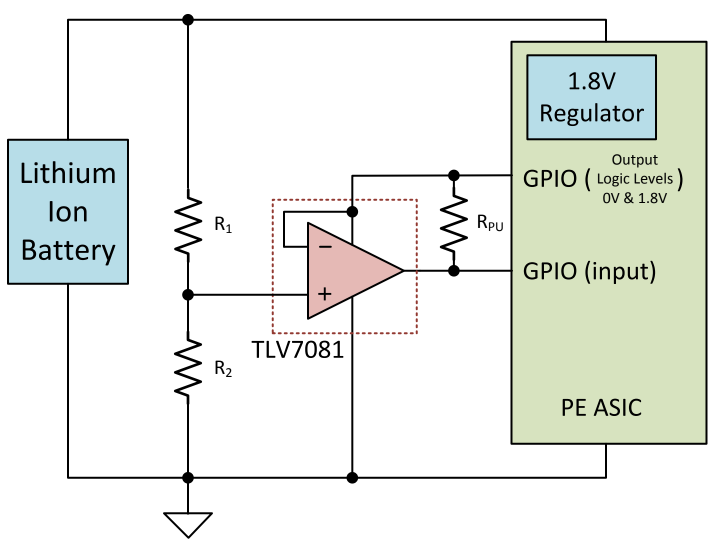



**Figure 23. Battery Monitor**

# 9 Layout

## 9.1 Layout Guidelines

A power supply bypass capacitor of 100 nF is recommended when supply output impedance is high, supply traces are long, or when excessive noise is expected on the supply lines. Bypass capacitors are also recommended when the comparator output drives a long trace or is required to drive a capacitive load. Due to the fast rising and falling edge rates and high-output sink and source capability of the TLV7081 output stages, higher than normal quiescent current can be drawn from the power supply. Under this circumstance, the system would benefit from a bypass capacitor across the supply pins.

## 9.2 Layout Example

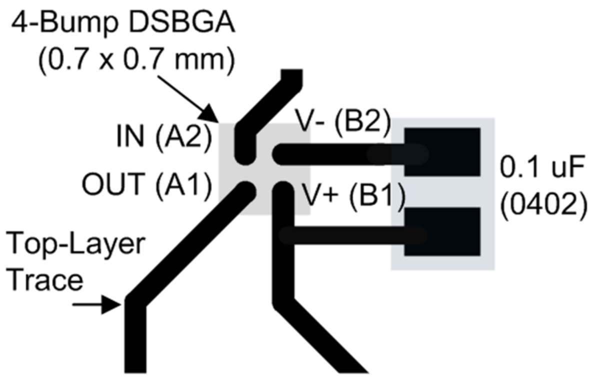



**Figure 24. Layout Example**

# 10 Device and Documentation Support

## 10.1 Documentation Support

### 10.1.1 Related Documentation

For related documentation see the following:

- TLV7081
- TLV7031
- TLV7041
- TLV7011
- TLV7021

## 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 10.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 10.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 10.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TLV7081YKAR | Active | Production | DSBGA (YKA) \| 4 | 3000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | W |
| TLV7081YKAR.A | Active | Production | DSBGA (YKA) \| 4 | 3000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -40 to 125 | W |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

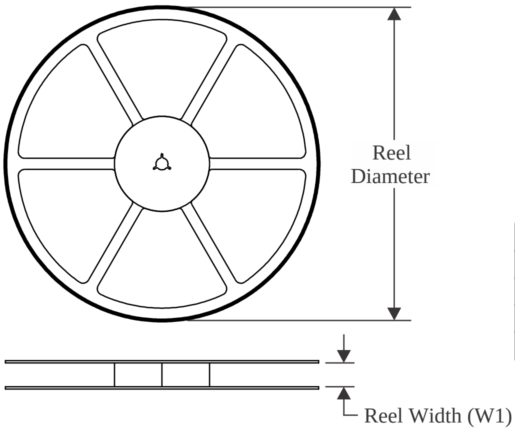
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

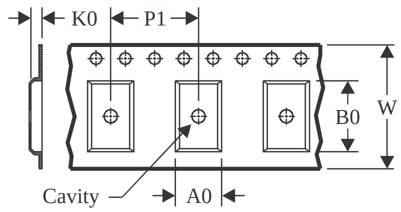
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

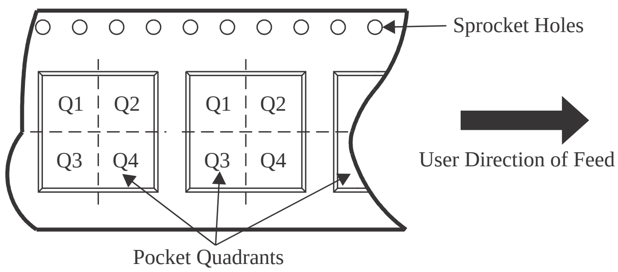



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

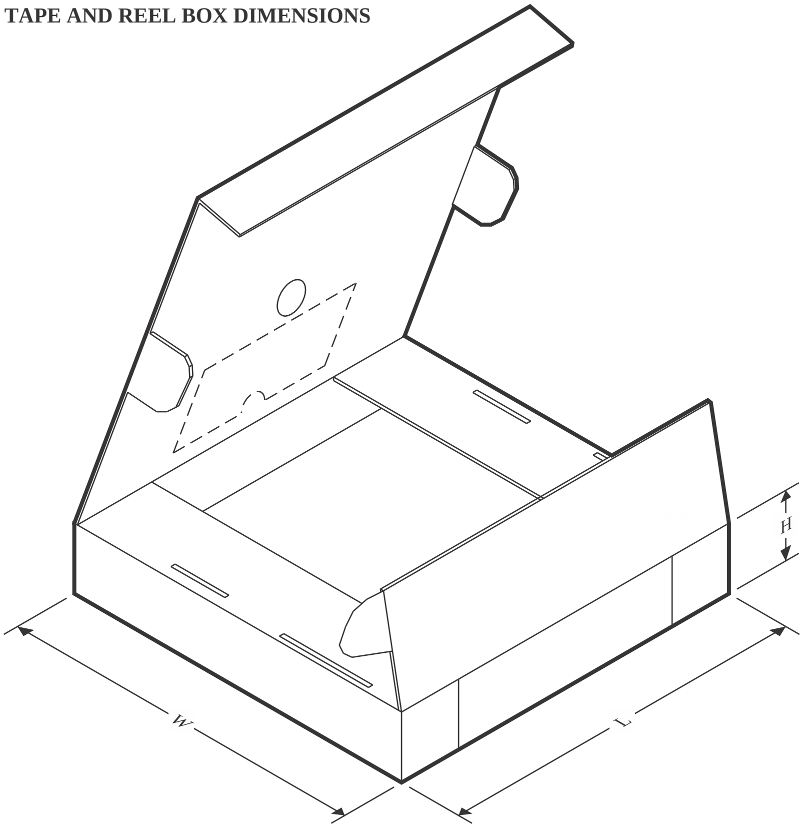
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

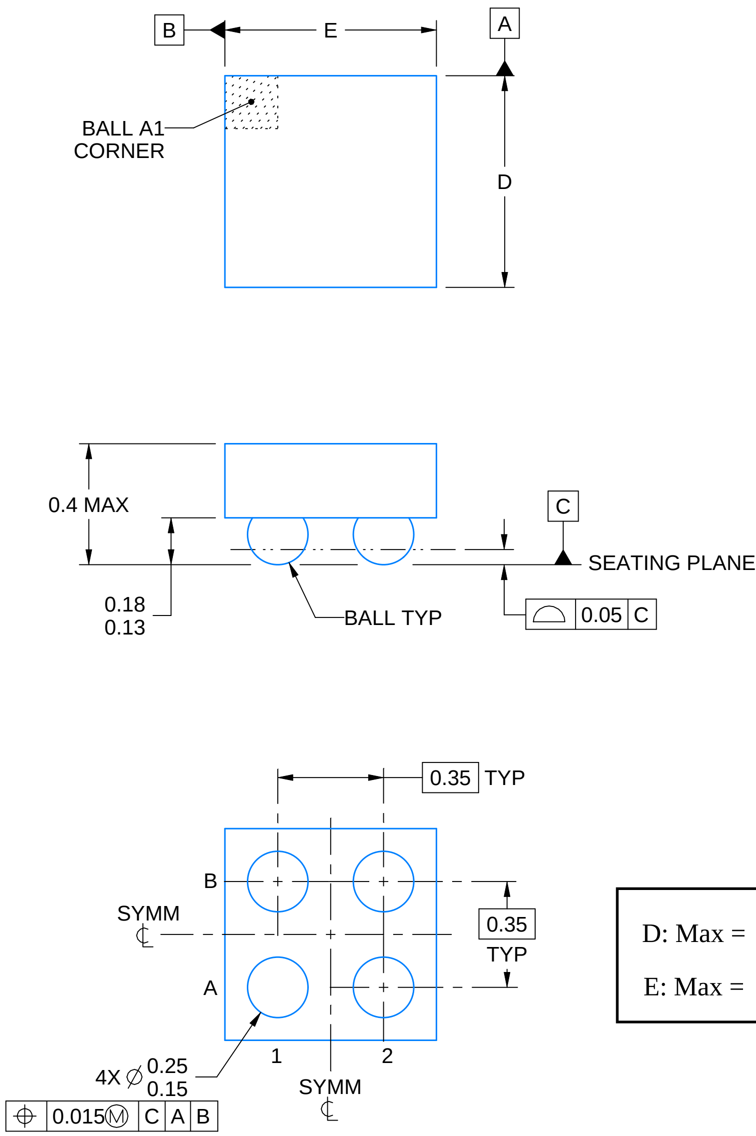
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV7081YKAR | DSBGA | YKA | 4 | 3000 | 180.0 | 8.4 | 0.8 | 0.8 | 0.47 | 4.0 | 8.0 | Q1 |
| TLV7081YKAR | DSBGA | YKA | 4 | 3000 | 180.0 | 8.4 | 0.8 | 0.8 | 0.47 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLV7081YKAR | DSBGA | YKA | 4 | 3000 | 182.0 | 182.0 | 20.0 |
| TLV7081YKAR | DSBGA | YKA | 4 | 3000 | 182.0 | 182.0 | 20.0 |

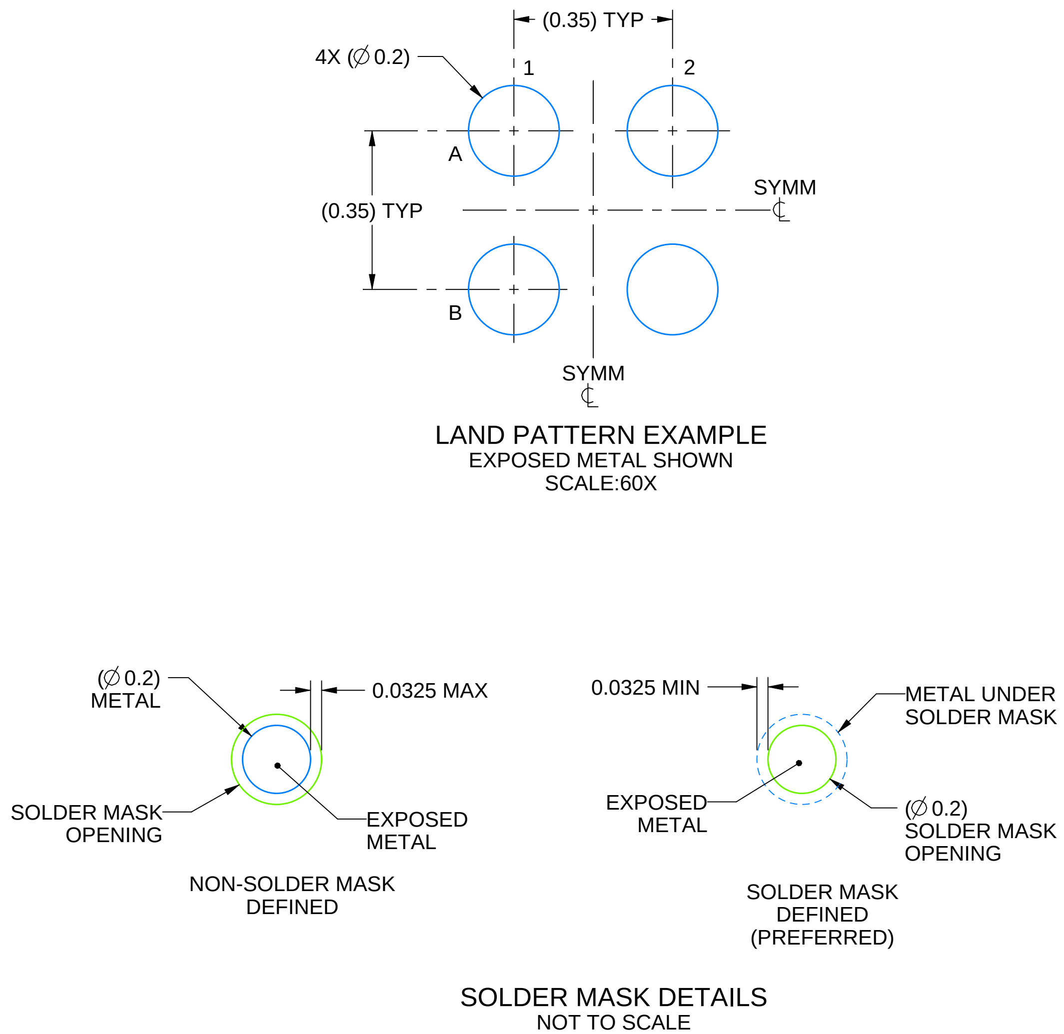



| | |
|---|---|
| D: Max = 0.73 mm, Min = 0.67 mm | |
| E: Max = 0.73 mm, Min = 0.67 mm | |

4221909/B 08/2018

NOTES:

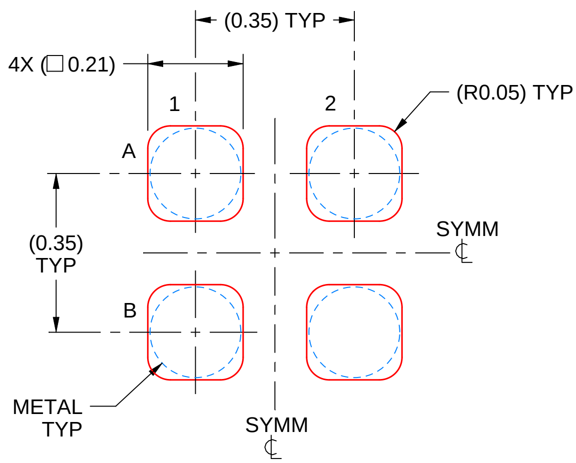
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




4221909/B 08/2018

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).




SOLDER PASTE EXAMPLE
BASED ON 0.075 mm - 0.1 mm THICK STENCIL
SCALE:60X

4221909/B 08/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.