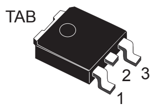
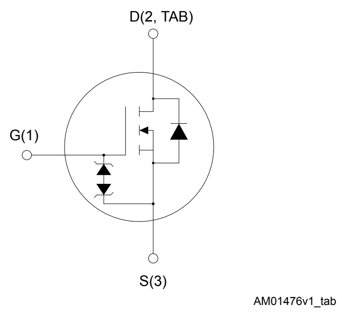
STD2N105K5

Datasheet

N-channel 1050 V, 6 Ω typ., 1.5 A MDmesh K5 Power MOSFET in a DPAK package



DPAK



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STD2N105K5	1050 V	8 Ω	1.5 A

- Ultra-low gate charge
- Very low FoM (figure of merit)
- Zener-protected
- 100% avalanche tested

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

STPOWER

Product status link
STD2N105K5

Product summary	
Order code	STD2N105K5
Marking	2N105K5
Package	DPAK
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	1.5	A
	Drain current (continuous) at T_C = 100 °C	0.95	
I_{DM} (1)	Drain current (pulsed)	6	A
P_{TOT}	Total power dissipation at T_C = 25 °C	60	W
dv/dt (2)	Peak diode recovery voltage slope	4.5	V/ns
dv/dt (3)	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. *Pulse width is limited by safe operating area.*
2. *I_{SD} ≤ 1.5 A, di/dt = 100 A/µs, V_{DS} (peak) < $V_{(BR)DSS}$.*
3. *V_{DD} ≤ 840 V.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	2.08	°C/W
R_{thJA} (1)	Thermal resistance, junction-to-ambient	50	°C/W

1. *When mounted on a standard 1-inch^2 area of FR-4 PCB with 2-oz copper.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_J max.)	0.5	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	90	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	1050			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 1050 V			1	µA
		V_{GS} = 0 V, V_{DS} = 1050 V, T_C = 125 °C (1)			50	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 0.75 A		6	8	Ω

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	115	-	pF
C_{oss}	Output capacitance		-	15	-	pF
C_{rss}	Reverse transfer capacitance		-	0.5	-	pF
$C_{o(tr)}$ (1)	Equivalent output capacitance time related	V_{DS} = 0 to 840 V, V_{GS} = 0 V	-	17	-	pF
$C_{o(er)}$ (2)	Equivalent output capacitance energy related		-	6	-	pF
R_g	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	20	-	Ω
Q_g	Total gate charge	V_{DD} = 840 V, I_D = 1.5 A, V_{GS} = 0 to 10 V (see Figure 15. Test circuit for gate charge behavior)	-	10	-	nC
Q_{gs}	Gate-source charge		-	1.5	-	nC
Q_{gd}	Gate-drain charge		-	8	-	nC

1. *$C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.*
2. *$C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 525 V, I_D = 0.75 A,	-	14.5	-	ns
t_r	Rise time	R_G = 4.7 Ω, V_{GS} = 10 V	-	8.5	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	35	-	ns
t_f	Fall time		-	38.5	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		1.5	A
I_{SDM} (1)	Source-drain current (pulsed)		-		6	A
V_{SD} (2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 1.5 A	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 1.5 A, di/dt = 100 A/µs, V_{DD} = 60 V (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	326		ns
Q_{rr}	Reverse recovery charge		-	1.19		µC
I_{RRM}	Reverse recovery current		-	7.3		A
t_{rr}	Reverse recovery time	I_{SD} = 1.5 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_J = 150 °C (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	525		ns
Q_{rr}	Reverse recovery charge		-	1.83		µC
I_{RRM}	Reverse recovery current		-	7		A

1. *Pulse width is limited by safe operating area.*
2. *Pulse test: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

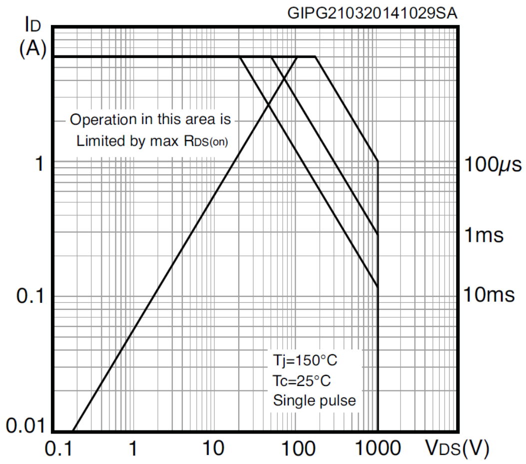


Figure 2. Normalized transient thermal impedance

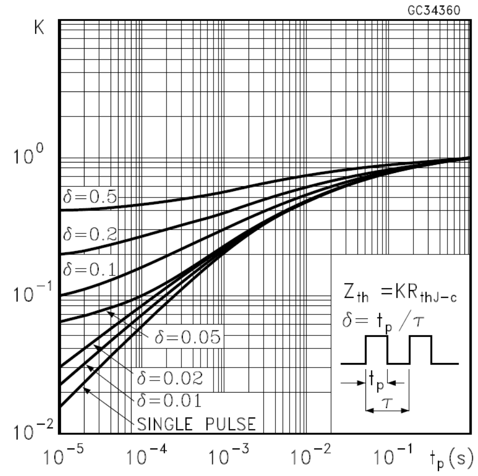


Figure 3. Typical output characteristics

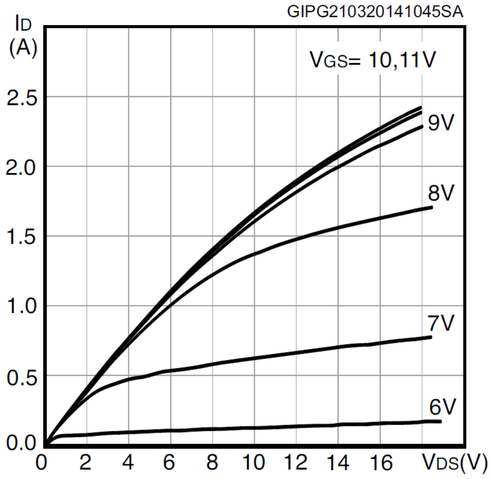


Figure 4. Typical transfer characteristics

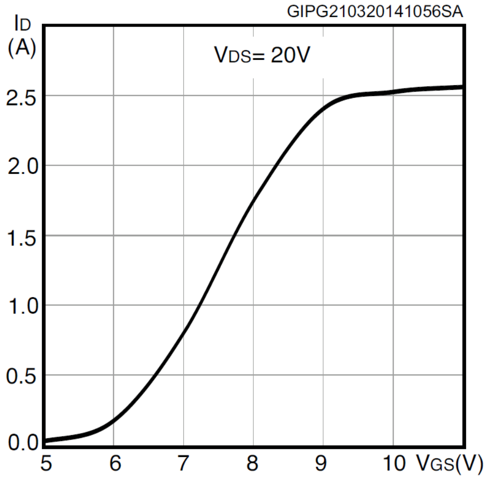


Figure 5. Typical gate charge characteristics

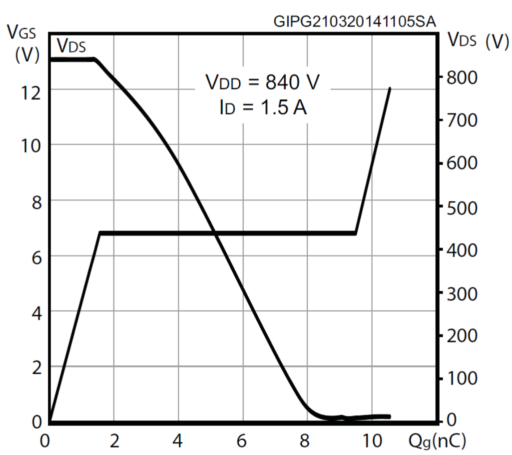


Figure 6. Typical drain-source on-resistance

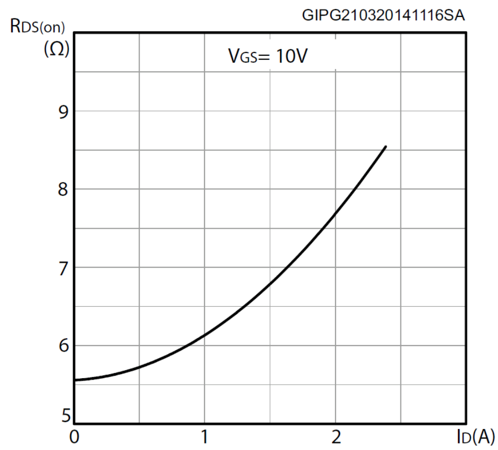


Figure 7. Typical capacitance characteristics

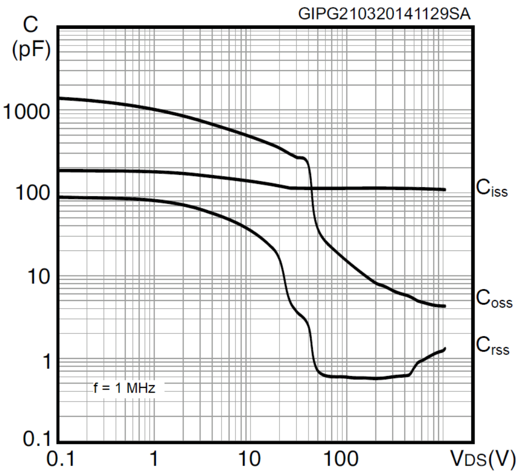


Figure 8. Typical output capacitance stored energy

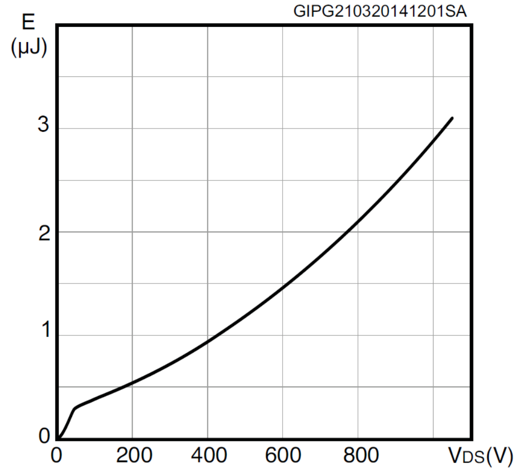


Figure 9. Normalized breakdown voltage vs temperature

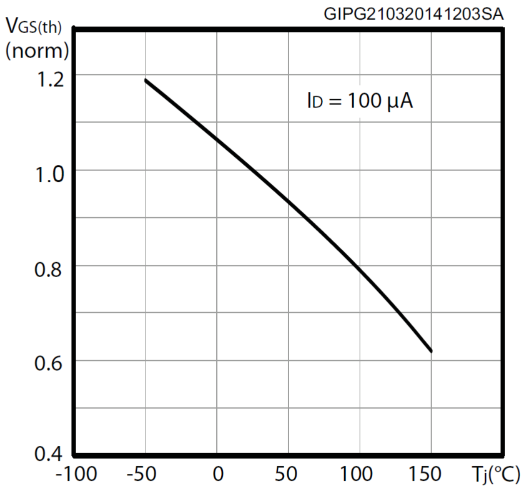


Figure 10. Normalized on-resistance vs temperature

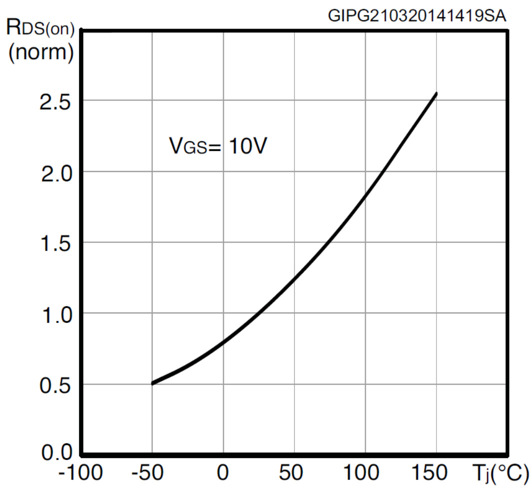


Figure 11. Typical reverse diode forward characteristics

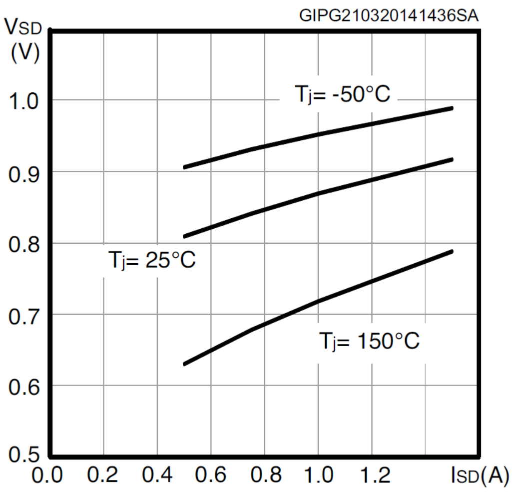


Figure 12. Normalized breakdown voltage vs temperature

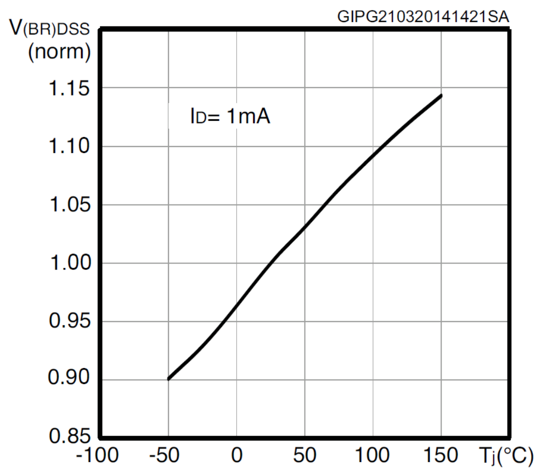
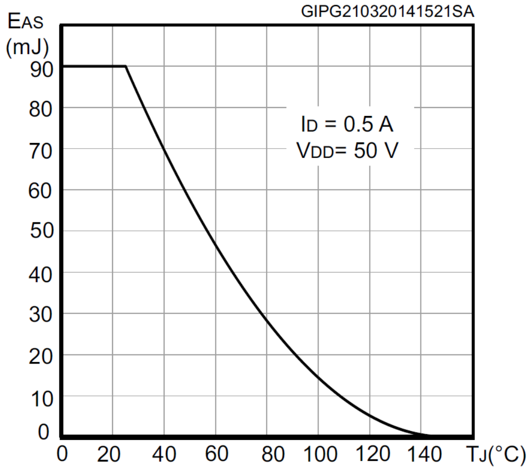


Figure 13. Maximum avalanche energy vs temperature



3 Test circuits

Figure 14. Test circuit for resistive load switching times

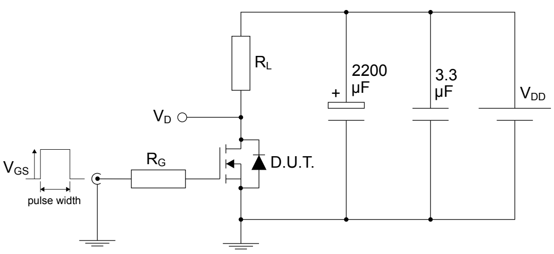


Figure 15. Test circuit for gate charge behavior

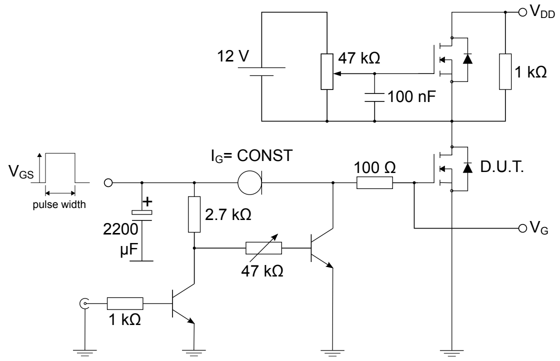


Figure 16. Test circuit for inductive load switching and diode recovery times

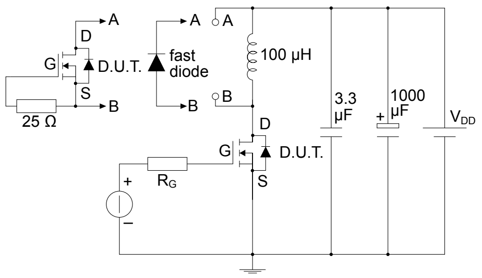


Figure 17. Unclamped inductive load test circuit

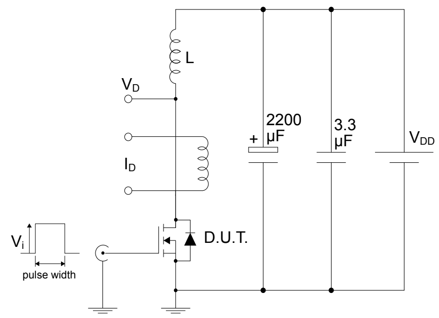


Figure 18. Unclamped inductive waveform

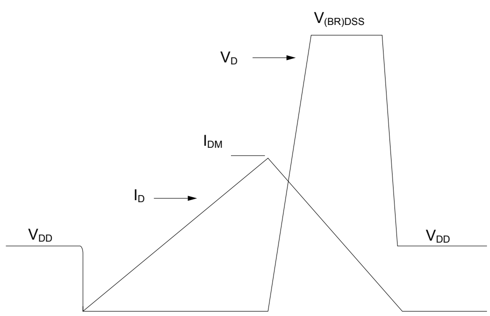
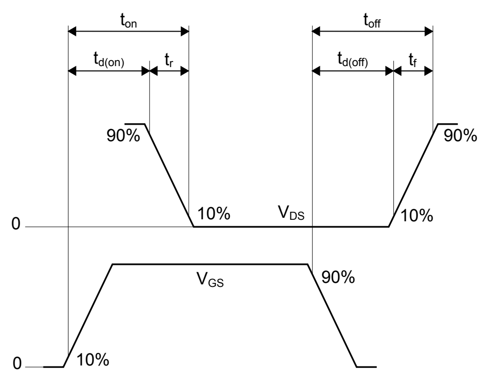


Figure 19. Switching time waveform



4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 DPAK (TO-252) type A package information

Figure 20. DPAK (TO-252) type A package outline

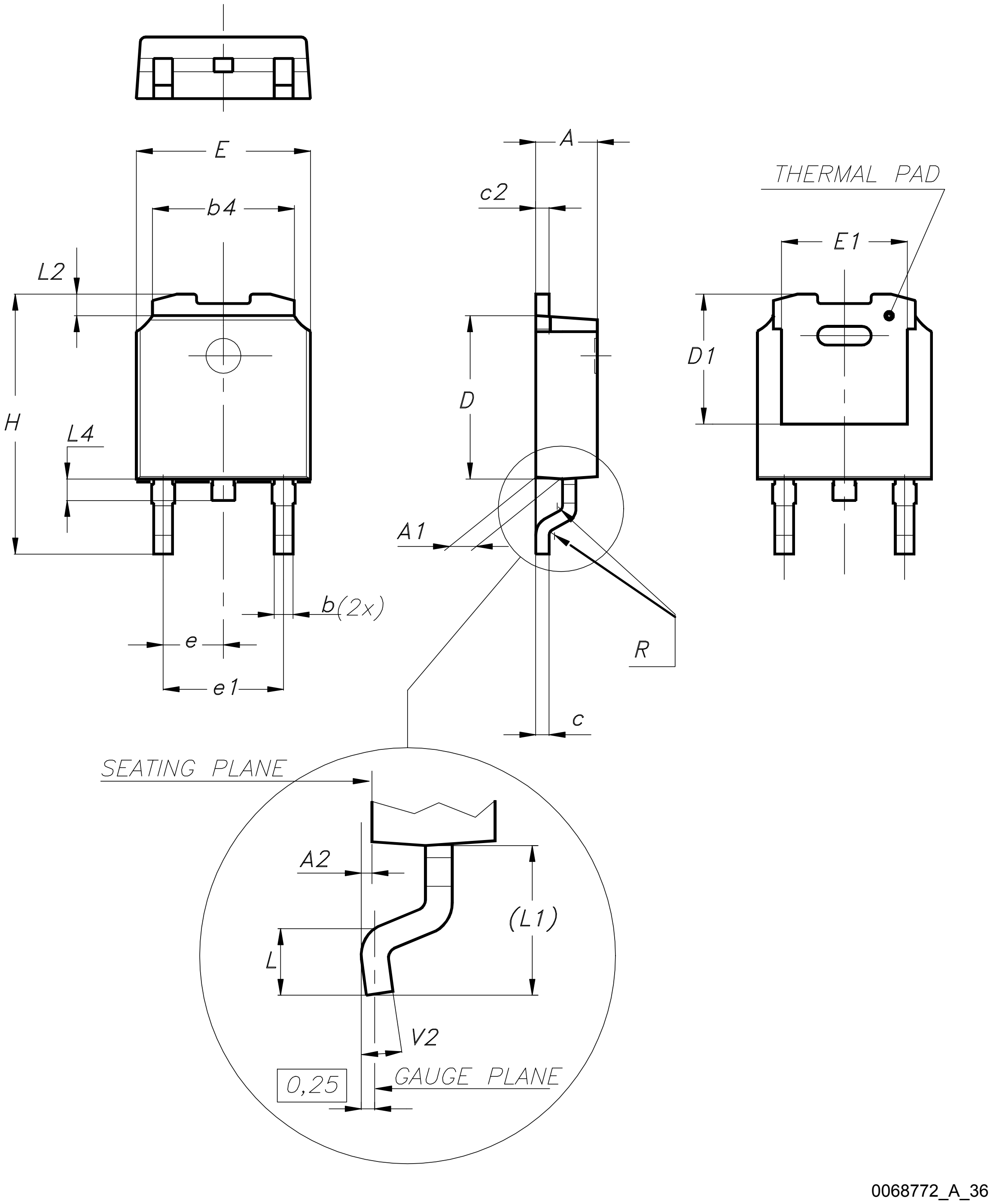


Table 8. DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

4.2 DPAK (TO-252) type A2 package information

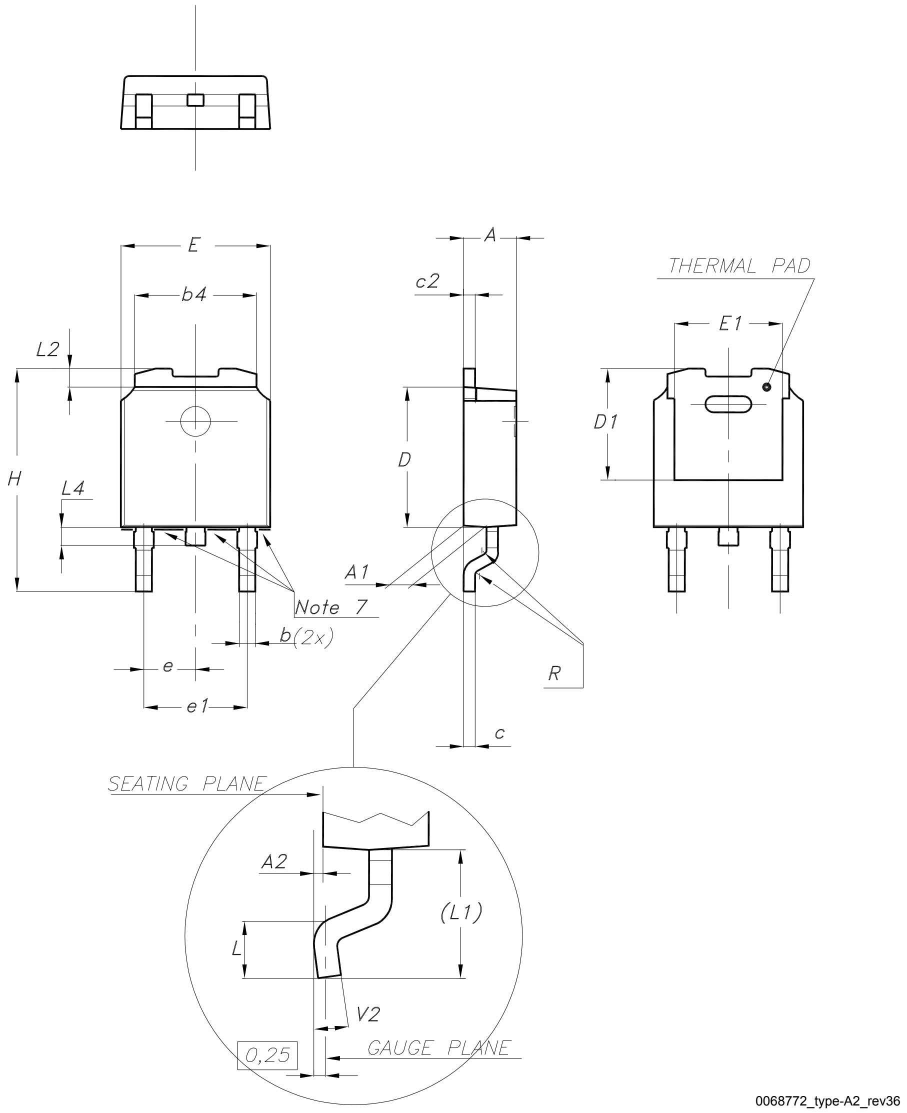
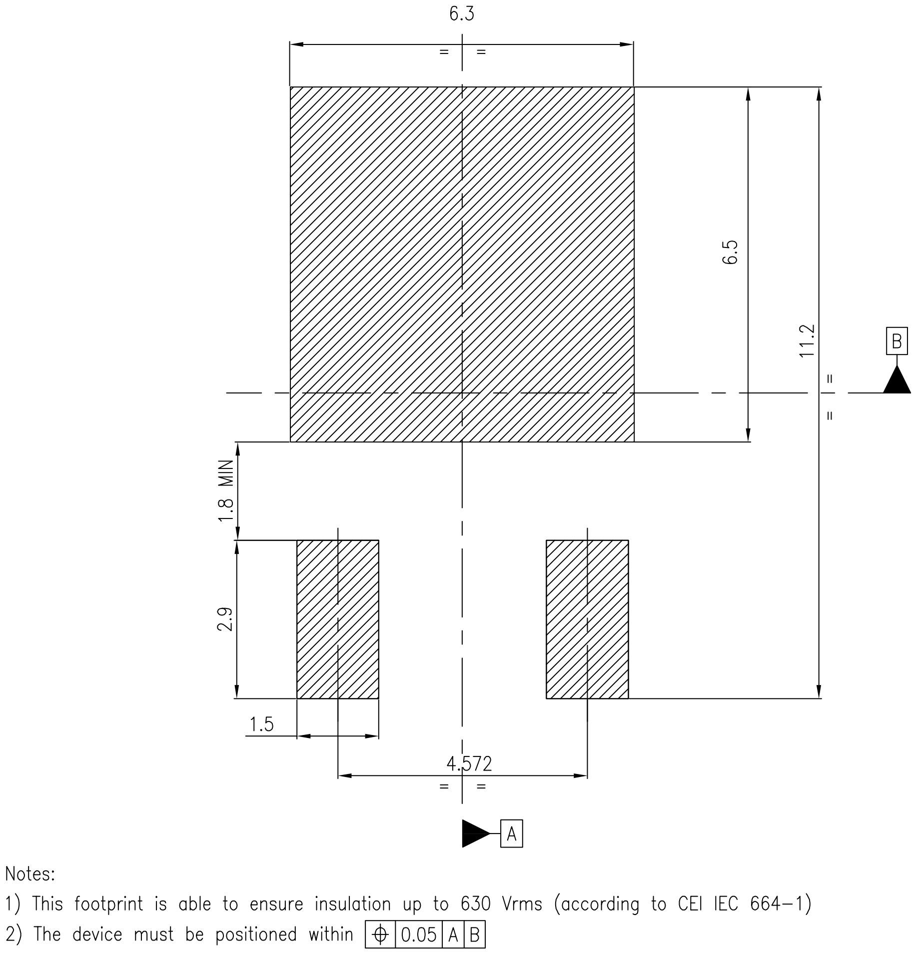


Figure 21. DPAK (TO-252) type A2 package outline

Table 9. DPAK (TO-252) type A2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 22. **DPAK (TO-252) recommended footprint (dimensions are in mm)**



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4.3 DPAK (TO-252) packing information

Figure 23. **DPAK (TO-252) tape outline**

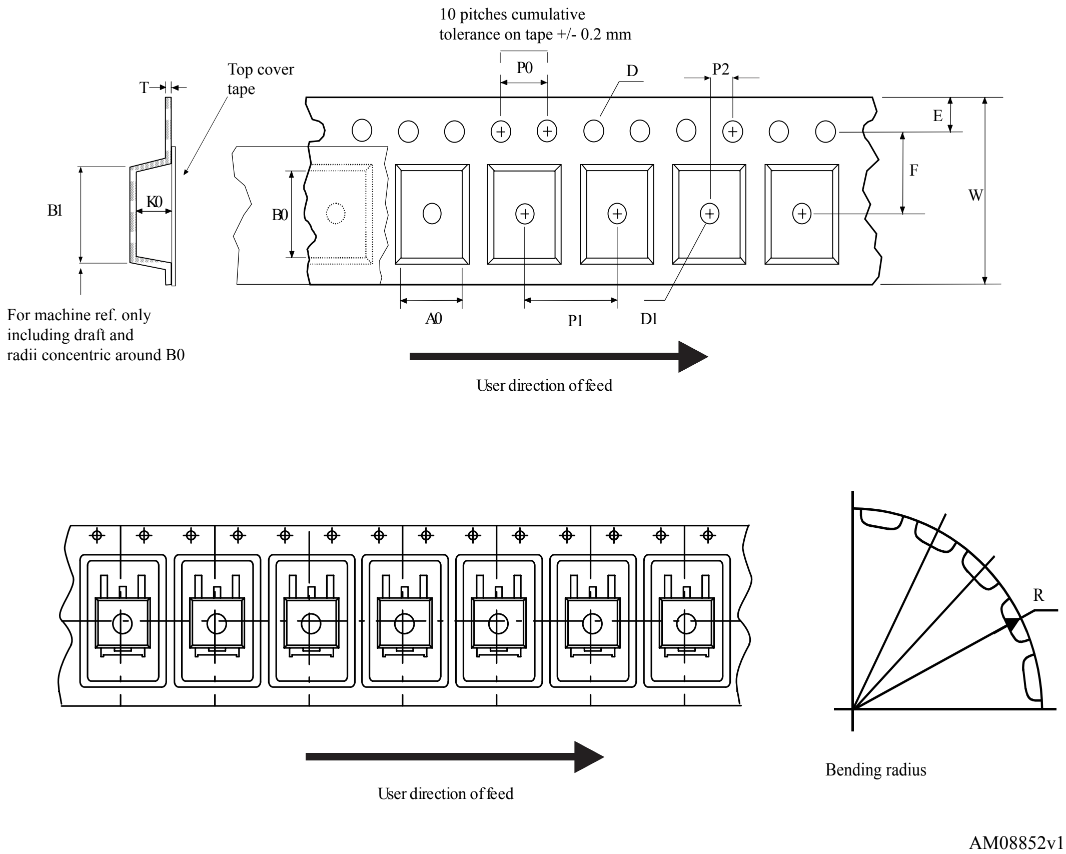

Figure 24. DPAK (TO-252) reel outline

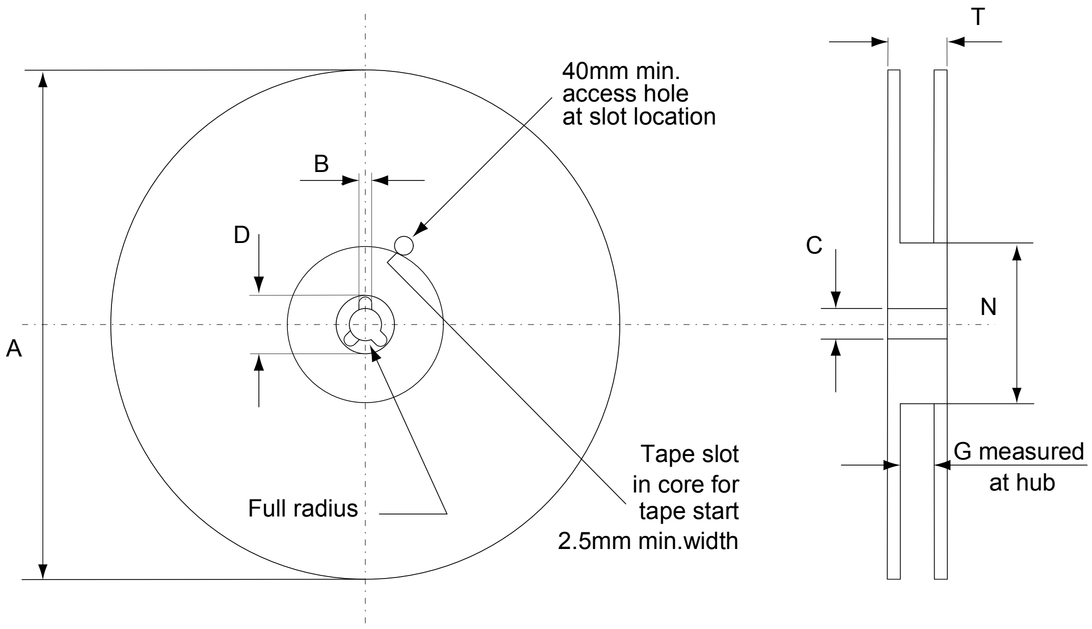

Table 10. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Revision history

Table 11. Document revision history

Date	Revision	Changes
08-May-2014	1	First release.
14-Nov-2014	2	Updated title, features and description in cover page. Document status promoted from preliminary to production data. Updated title, features and description in cover page. Updated *Figure 9: Static drain-source on-resistance*, *Section 4.1: DPAK, STD2N105K5* and *Section 4.3: IPAK, STU2N105K5*. Minor text changes.
19-Nov-2014	3	Updated V_{GS} in *Table 2: Absolute maximum ratings* and I_{GSS} in*Table 4: On /off states*.
28-Jun-2023	4	The part numbers STP2N105K5, and STU2N105K5 have been moved to a separate datasheet and the document has been updated accordingly. Removed *Table 8. Gate-source Zener diode*. Updated *Figure 7. Typical capacitance characteristics.* Updated *Section 4.1 DPAK (TO-252) package information.*
07-Apr-2026	5	Updated Section 4: Package information. Minor text changes.

Contents