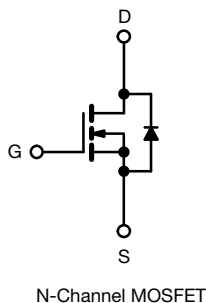
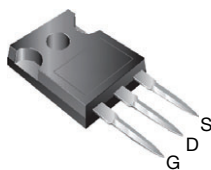


Power MOSFET

TO-247AC


FEATURES

- Superfast body diode eliminates the need for external diodes in ZVS applications
- Lower gate charge results in simpler drive requirements
- Enhanced dV/dt capabilities offer improved ruggedness
- Higher gate voltage threshold offers improved noise immunity
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS*
Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

APPLICATIONS

- Zero voltage switching (SMPS)
- Telecom and server power supplies
- Uninterruptible power supplies
- Motor control applications

PRODUCT SUMMARY

V_{DS} (V)	600	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	0.21
Q_g (max.) (nC)	180	
Q_{gs} (nC)	61	
Q_{gd} (nC)	85	
Configuration	Single	

ORDERING INFORMATION

Package	TO-247AC
Lead (Pb)-free	IRFP26N60LPbF

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	600	V
Gate-source voltage	V_{GS}	± 30	
Continuous drain current	V_{GS} at 10 V	$T_C = 25\text{ }^\circ\text{C}$	A
		$T_C = 100\text{ }^\circ\text{C}$	
Pulsed drain Current ^a	I_{DM}	100	
Linear derating Factor		3.8	W/ $^\circ\text{C}$
Single pulse avalanche energy ^b	E_{AS}	570	mJ
Repetitive avalanche current ^a	I_{AR}	26	A
Repetitive avalanche energy ^a	E_{AR}	47	mJ
Maximum power dissipation	P_D	470	W
Peak diode recovery dV/dt ^c	dV/dt	21	V/ns
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$
Soldering recommendations (peak temperature) ^d	for 10 s	300	
Mounting torque	6-32 or M3 screw	10	lbf · in
		1.1	N · m

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 1.7\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 26\text{ A}$, dV/dt = 21 V/ns (see fig. 12)
- $I_{SD} \leq 26\text{ A}$, dI/dt $\leq 480\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$
- 1.6 mm from case

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	40	°C/W
Case-to-sink, flat, greased surface	R_{thCS}	0.24	-	
Maximum junction-to-case (drain)	R_{thJC}	-	0.27	

SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

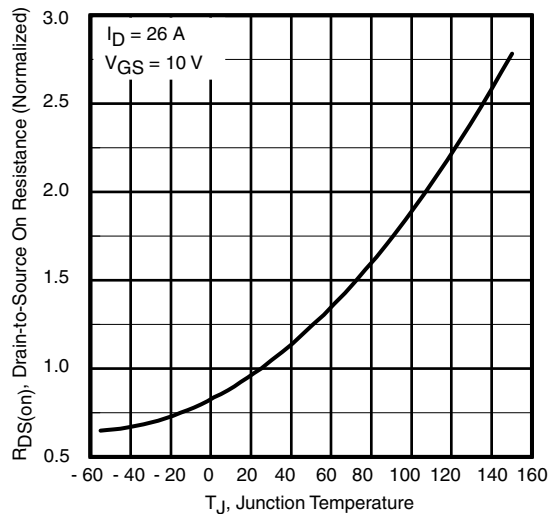
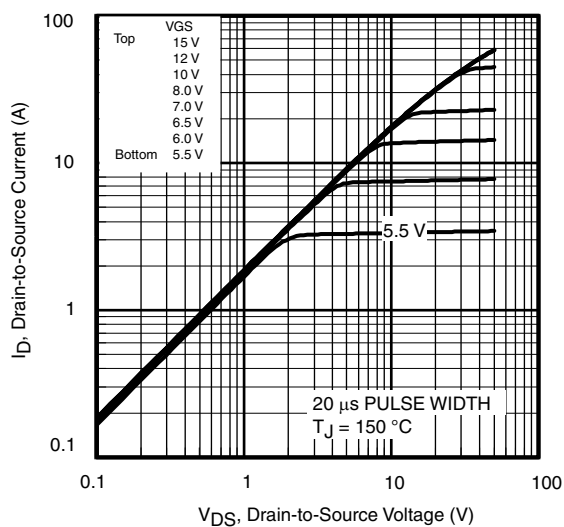
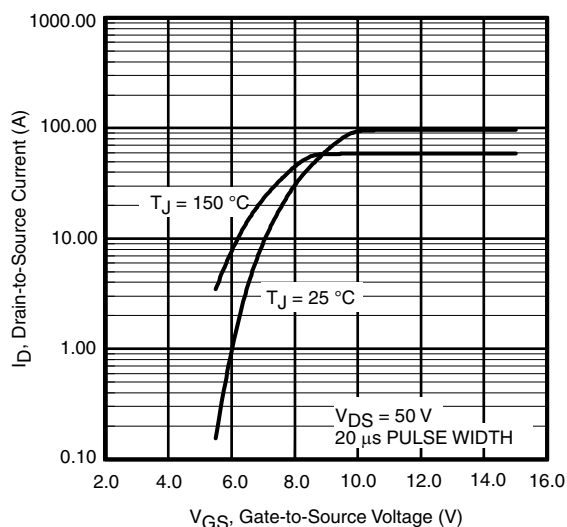
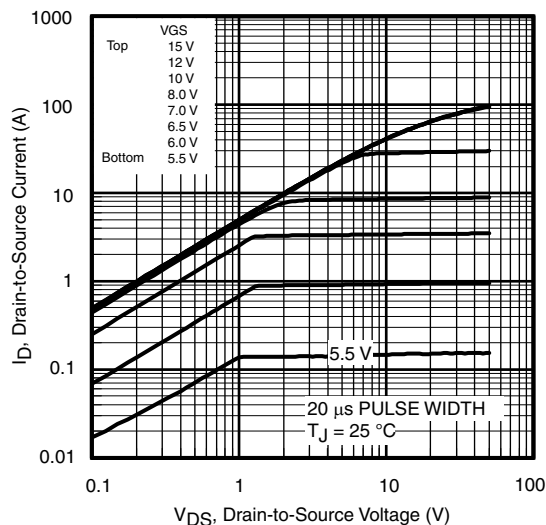
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		600	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.33	-	V/°C
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		3.0	-	5.0	V
Gate-source leakage	I _{GSS}	V _{GS} = ± 30 V		-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 600 V, V _{GS} = 0 V		-	-	50	μA
		V _{DS} = 480 V, V _{GS} = 0 V, T _J = 125 °C		-	-	2.0	mA
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 10 A ^b	-	0.21	0.25	Ω
Forward transconductance	g _{fs}	V _{DS} = 50 V, I _D = 16 A		13	-	-	S
Dynamic							
Input capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	5020	-	pF
Output capacitance	C _{oss}			-	450	-	
Reverse transfer capacitance	C _{rss}			-	34	-	
Effective output capacitance	C _{oss} eff.	V _{GS} = 0 V	V _{DS} = 0 V to 480 V ^c	-	230	-	
Effective output Ccapacitance (energy related)	C _{oss} eff. (ER)			-	170	-	
Total gate charge	Q _g	V _{GS} = 10 V	I _D = 26 A, V _{DS} = 480 V, see fig. 7 and 15 ^b	-	-	180	nC
Gate-source charge	Q _{gs}			-	-	61	
Gate-drain charge	Q _{gd}			-	-	85	
Turn-on delay time	t _{d(on)}	V _{DD} = 300 V, I _D = 26 A, R _g = 4.3 Ω, V _{GS} = 10 V see fig. 11a and 11b ^b		-	31	-	ns
Rise time	t _r			-	110	-	
Turn-off delay time	t _{d(off)}			-	47	-	
Fall time	t _f			-	42	-	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	26	A
Pulsed diode forward current ^a	I _{SM}			-	-	100	
Body diode voltage	V _{SD}	T _J = 25 °C, I _S = 26 A, V _{GS} = 0 V ^b		-	-	1.5	V
Body diode reverse recovery time	t _{rr}	T _J = 25 °C, I _F = 26 A		-	170	250	ns
Body diode reverse recovery charge		T _J = 125 °C, dI/dt = 100 A/μs ^b		-	210	320	
Continuous source-drain diode current	Q _{rr}	T _J = 25 °C, I _F = 26 A, V _{GS} = 0 V ^b		-	670	1000	nC
Pulsed diode forward current ^a		T _J = 125 °C, dI/dt = 100 A/μs ^b		-	1050	1570	
Reverse recovery current	I _{RRM}	T _J = 25 °C		-	7.3	11	A
Forward turn-on time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

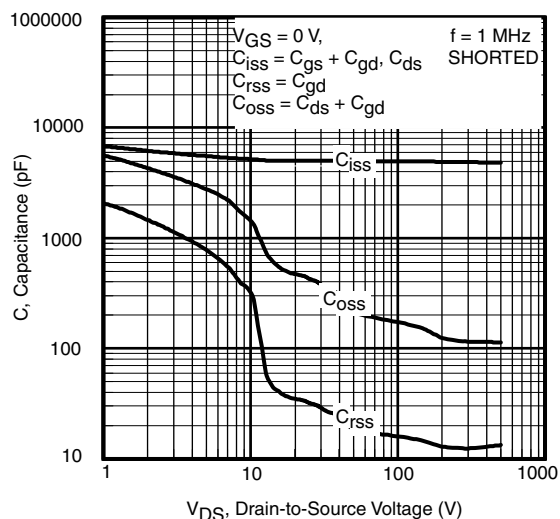
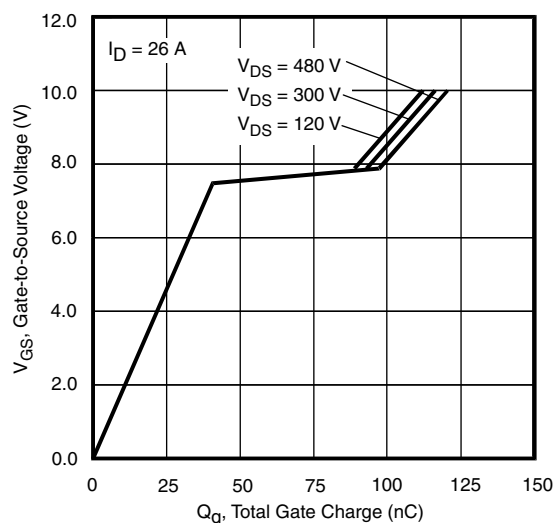
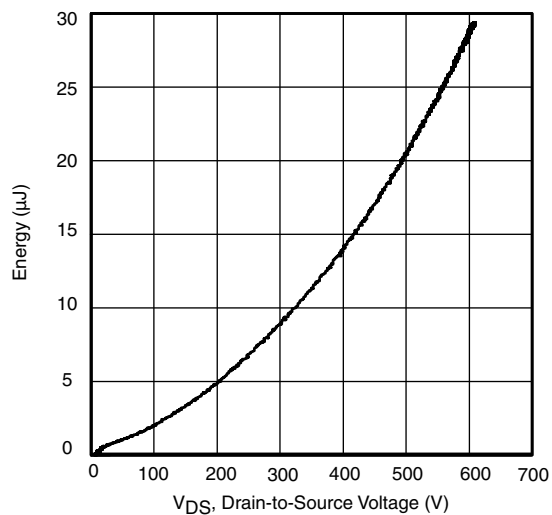
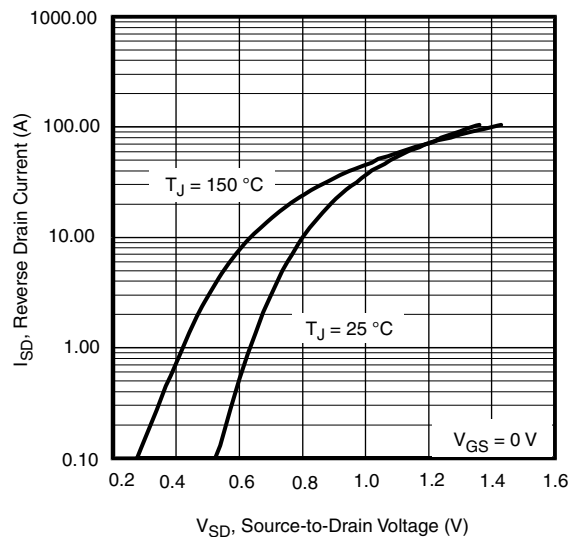
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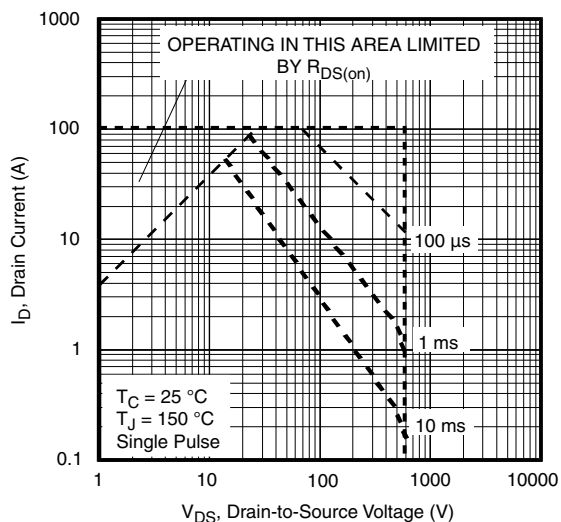
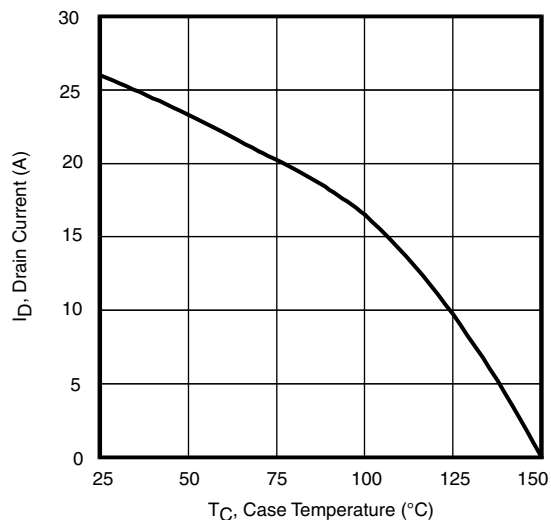
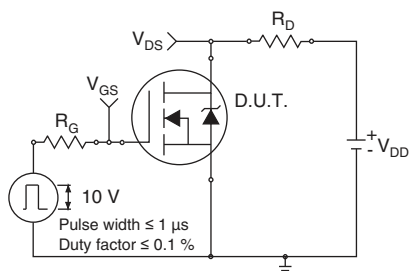
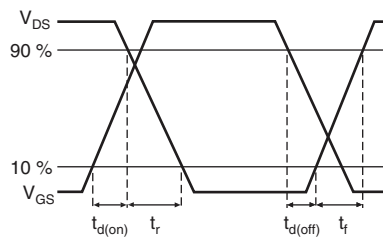
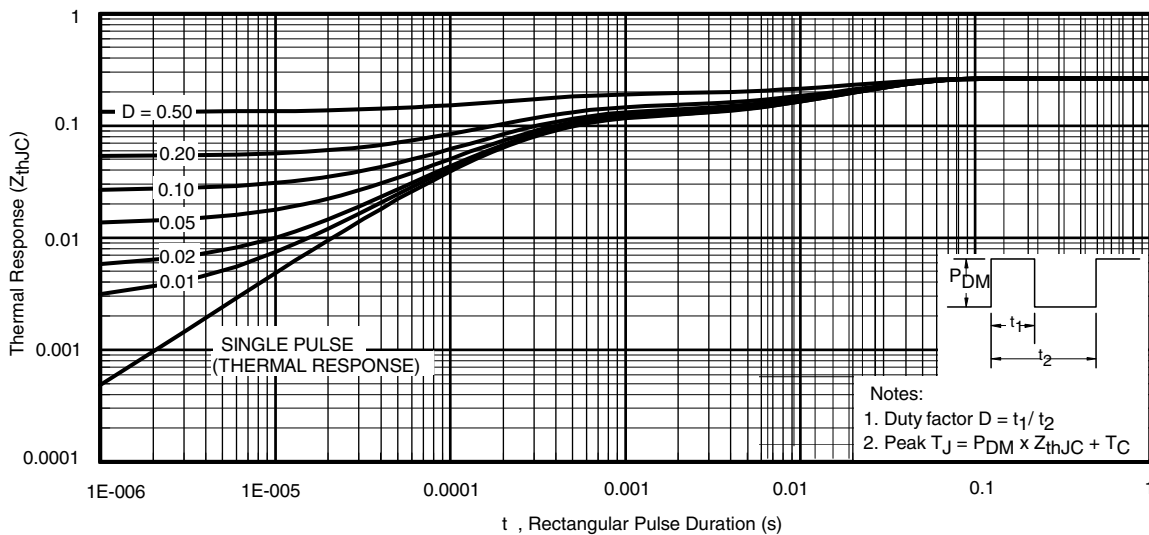
- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$
- c. $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}
 $C_{oss\text{ eff. (ER)}}$ is a fixed capacitance that stores the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}

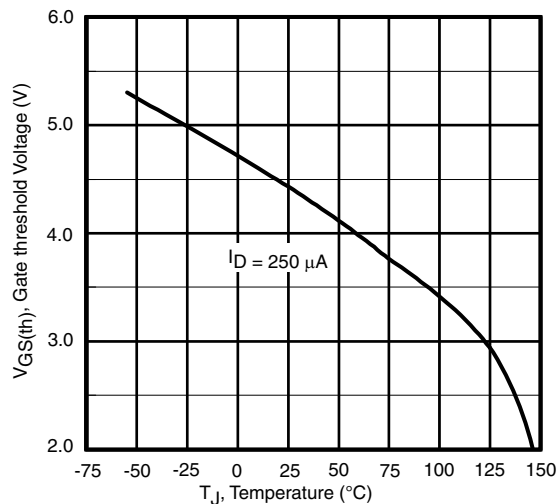
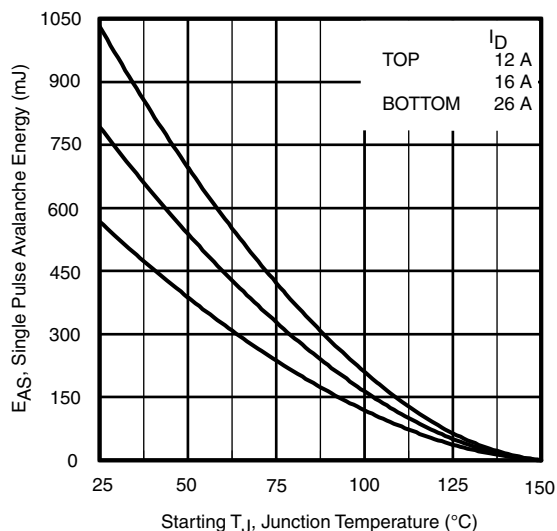
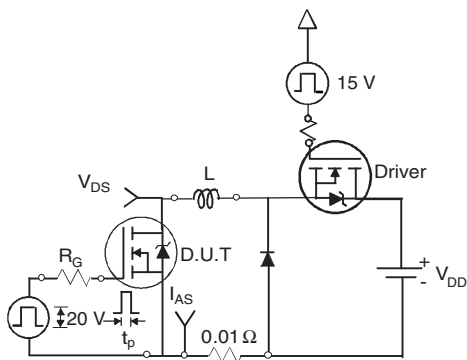
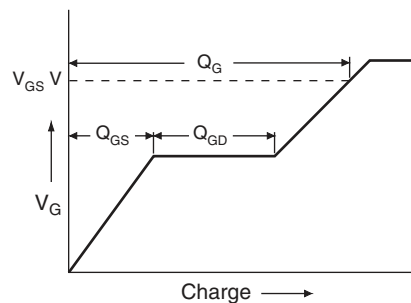
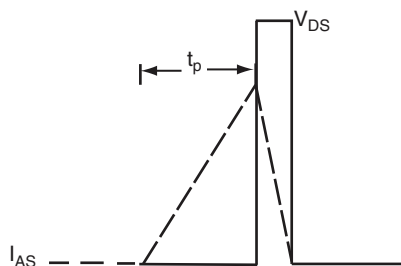
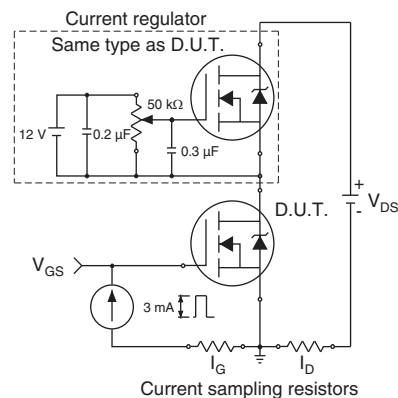


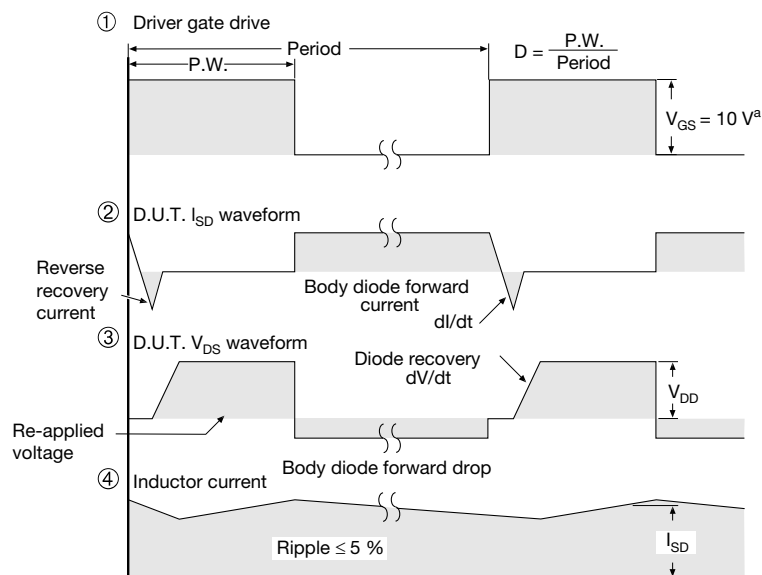
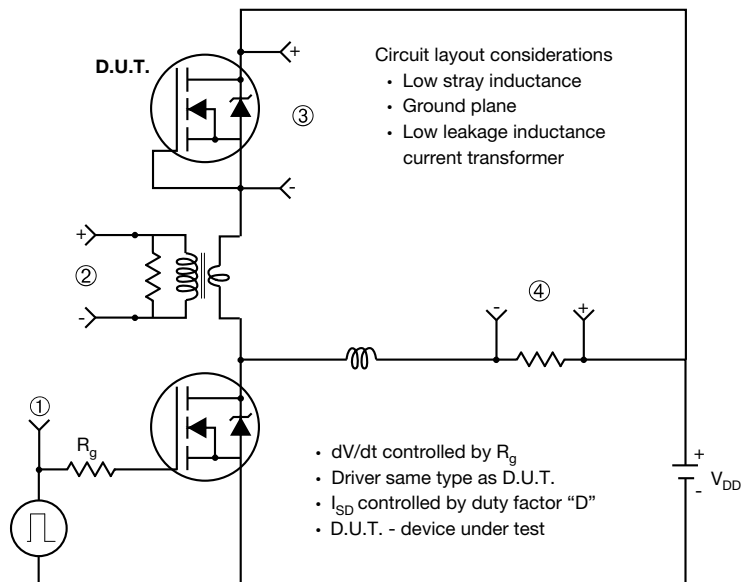
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)




Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

Fig. 6 - Typical Output Capacitance Stored Energy vs. V_{DS}

Fig. 8 - Typical Source-Drain Diode Forward Voltage


Fig. 9 - Maximum Safe Operating Area

Fig. 11 - Maximum Drain Current vs. Case Temperature

Fig. 10 - Switching Time Test Circuit

Fig. 12 - Switching Time Waveforms

Fig. 13 - Maximum Effective Transient Thermal Impedance, Junction-to-Case


Fig. 14 - Threshold Voltage vs. Temperature

Fig. 17 - Maximum Avalanche Energy vs. Drain Current

Fig. 15 - Unclamped Inductive Test Circuit

Fig. 18 - Basic Gate Charge Waveform

Fig. 16 - Unclamped Inductive Waveforms

Fig. 19 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

Note

a. $V_{GS} = 5\text{ V}$ for logic level devices

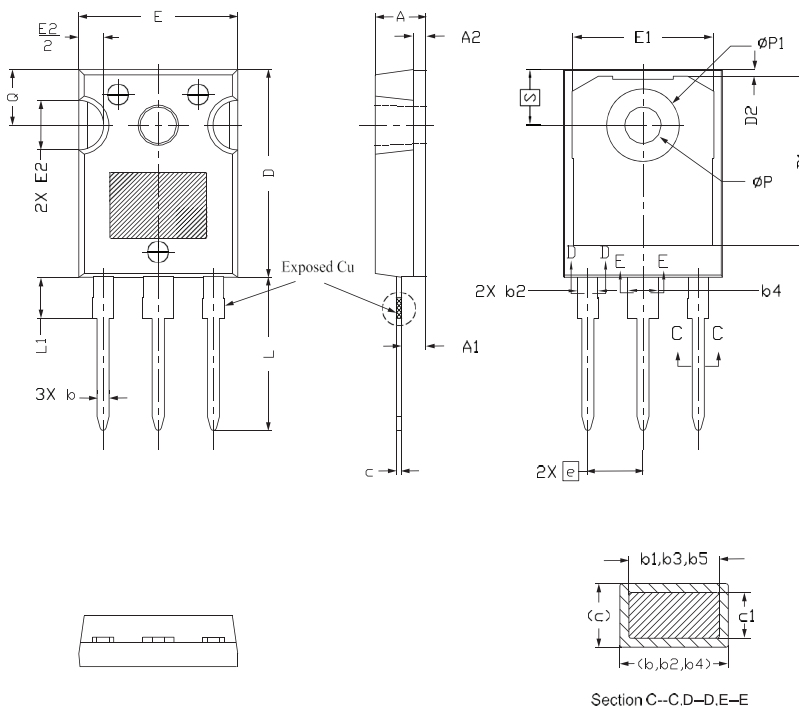
Fig. 20 - For N-Channel

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TO-247AC (High Voltage)

VERSION 1: FACILITY CODE = 9



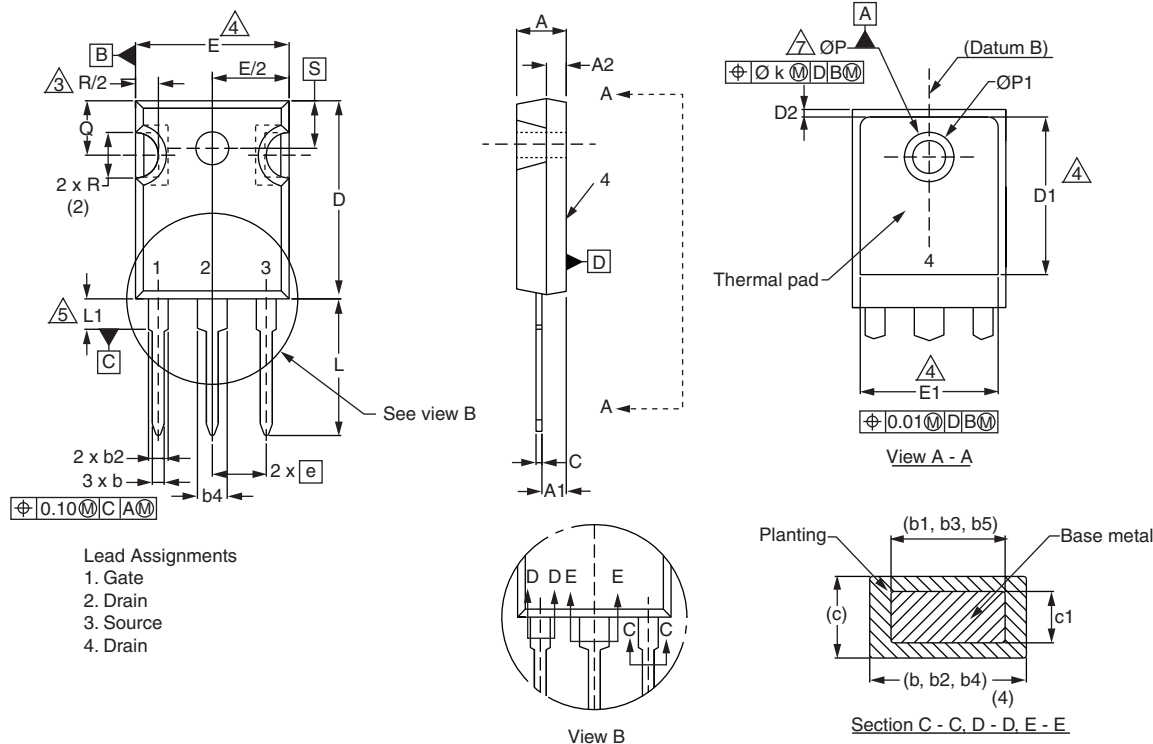
Section C--C,D--D,E--E

MILLIMETERS				
DIM.	MIN.	NOM.	MAX.	NOTES
A	4.83	5.02	5.21	
A1	2.29	2.41	2.55	
A2	1.17	1.27	1.37	
b	1.12	1.20	1.33	
b1	1.12	1.20	1.28	
b2	1.91	2.00	2.39	6
b3	1.91	2.00	2.34	
b4	2.87	3.00	3.22	6, 8
b5	2.87	3.00	3.18	
c	0.40	0.50	0.60	6
c1	0.40	0.50	0.56	
D	20.40	20.55	20.70	4

MILLIMETERS				
DIM.	MIN.	NOM.	MAX.	NOTES
D1	16.46	16.76	17.06	5
D2	0.56	0.66	0.76	
E	15.50	15.70	15.87	4
E1	13.46	14.02	14.16	5
E2	4.52	4.91	5.49	3
e	5.46 BSC			
L	14.90	15.15	15.40	
L1	3.96	4.06	4.16	6
Ø P	3.56	3.61	3.65	7
Ø P1	7.19 ref.			
Q	5.31	5.50	5.69	
S	5.51 BSC			

Notes

- (1) Package reference: JEDEC® TO247, variation AC
- (2) All dimensions are in mm
- (3) Slot required, notch may be rounded
- (4) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outermost extremes of the plastic body
- (5) Thermal pad contour optional with dimensions D1 and E1
- (6) Lead finish uncontrolled in L1
- (7) Ø P to have a maximum draft angle of 1.5° to the top of the part with a maximum hole diameter of 3.91 mm
- (8) Dimension b2 and b4 does not include dambar protrusion. Allowable dambar protrusion shall be 0.1 mm total in excess of b2 and b4 dimension at maximum material condition

**VERSION 2: FACILITY CODE = Y**

DIM.	MILLIMETERS		NOTES
	MIN.	MAX.	
A	4.58	5.31	
A1	2.21	2.59	
A2	1.17	2.49	
b	0.99	1.40	
b1	0.99	1.35	
b2	1.53	2.39	
b3	1.65	2.37	
b4	2.42	3.43	
b5	2.59	3.38	
c	0.38	0.86	
c1	0.38	0.76	
D	19.71	20.82	
D1	13.08	-	

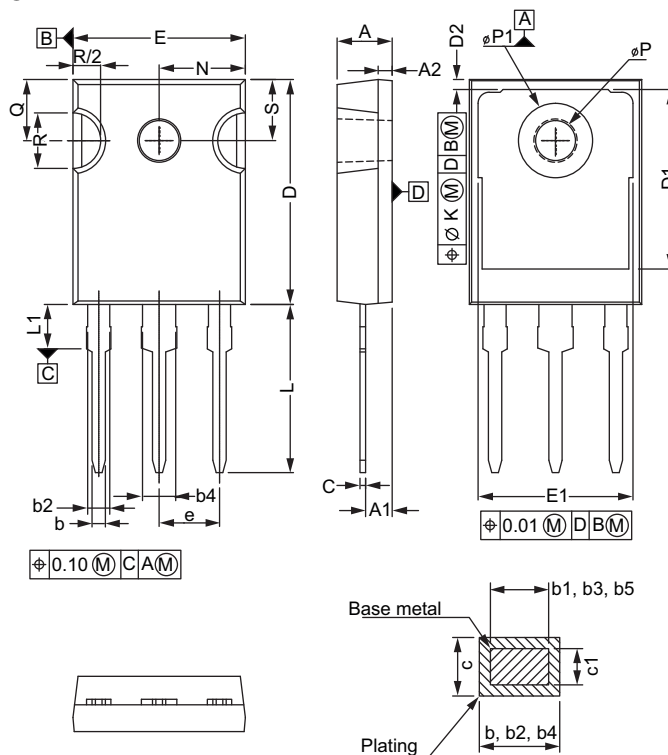
DIM.	MILLIMETERS		NOTES
	MIN.	MAX.	
D2	0.51	1.30	
E	15.29	15.87	
E1	13.72	-	
e	5.46 BSC		
Ø k	0.254		
L	14.20	16.25	
L1	3.71	4.29	
Ø P	3.51	3.66	
Ø P1	-	7.39	
Q	5.31	5.69	
R	4.52	5.49	
S	5.51 BSC		

Notes

- (1) Dimensioning and tolerancing per ASME Y14.5M-1994
- (2) Contour of slot optional
- (3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Thermal pad contour optional with dimensions D1 and E1
- (5) Lead finish uncontrolled in L1
- (6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")
- (7) Outline conforms to JEDEC outline TO-247 with exception of dimension c



VERSION 3: FACILITY CODE = N



MILLIMETERS		
DIM.	MIN.	MAX.
A	4.65	5.31
A1	2.21	2.59
A2	1.17	1.37
b	0.99	1.40
b1	0.99	1.35
b2	1.65	2.39
b3	1.65	2.34
b4	2.59	3.43
b5	2.59	3.38
c	0.38	0.89
c1	0.38	0.84
D	19.71	20.70
D1	13.08	-

MILLIMETERS		
DIM.	MIN.	MAX.
D2	0.51	1.35
E	15.29	15.87
E1	13.46	-
e	5.46 BSC	
k	0.254	
L	14.20	16.10
L1	3.71	4.29
N	7.62 BSC	
P	3.56	3.66
P1	-	7.39
Q	5.31	5.69
R	4.52	5.49
S	5.51 BSC	

ECN: E22-0452-Rev. G, 31-Oct-2022
DWG: 5971

Notes

- (1) Dimensioning and tolerancing per ASME Y14.5M-1994
- (2) Contour of slot optional
- (3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Thermal pad contour optional with dimensions D1 and E1
- (5) Lead finish uncontrolled in L1
- (6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")



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