

MOSFET – P-Channel, POWERTRENCH®

-30 V, -82 A, 6.8 mΩ

FDMS6673BZ, FDMS6673BZ-NC

General Description

The FDMS6673BZ has been designed to minimize losses in load switch applications. Advancements in both silicon and package technologies have been combined to offer the lowest $R_{DS(on)}$ and ESD protection.

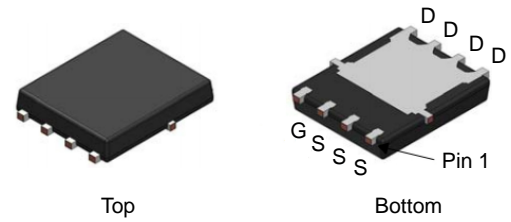
Features

- Max $R_{DS(on)}$ = 6.8 mΩ at $V_{GS} = -10$ V, $I_D = -15.2$ A
- Max $R_{DS(on)}$ = 12.5 mΩ at $V_{GS} = -4.5$ V, $I_D = -11.2$ A
- Advanced Package and Silicon Combination for Low $R_{DS(on)}$
- HBM ESD Protection Level of 8 kV Typical (Note 3)
- MSL1 Robust Package Design
- This Device is Halide Free and RoHS Compliant with Exemption 7a, Pb-Free 2LI (on second level interconnection)

Applications

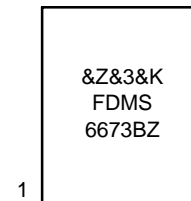
- Load Switch in Notebook and Server
- Notebook Battery Pack Power Management

V_{DS}	$R_{DS(on)}$ MAX	I_D Max
-30 V	6.8 mΩ @ $V_{GS} = -10$ V	-82 A
	12.5 mΩ @ $V_{GS} = -4.5$ V	



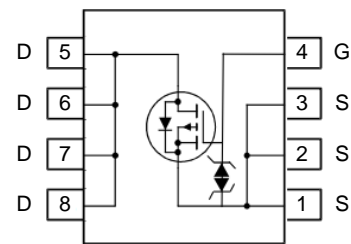
PQFN8 5X6, 1.27P
Power 56
CASE 483AE

MARKING DIAGRAM



- &Z = Assembly Plant Code
- &3 = 3-Digit Date Code
- &K = 2-Digits Lot Run Code
- FDMS6673BZ = Specific Device Code

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

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MOSFET MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating	Unit	
V_{DS}	Drain to Source Voltage	-30	V	
V_{GS}	Gate to Source Voltage	± 25	V	
I_D	Drain Current	Continuous, $T_C = 25\text{ }^\circ\text{C}$ (Note 5)	-82	A
		Continuous, $T_C = 100\text{ }^\circ\text{C}$ (Note 5)	-52	
		Continuous, $T_A = 25\text{ }^\circ\text{C}$ (Note 1a)	-15.2	
		Pulsed (Note 4)	-422	
P_D	Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	73	W
		$T_A = 25\text{ }^\circ\text{C}$ (Note 1a)	2.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Rating	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.7	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = -250\text{ }\mu\text{A}, V_{GS} = 0\text{ V}$	-30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		-18		$\text{mV}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -24\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 25\text{ V}, V_{DS} = 0\text{ V}$			± 10	μA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250\text{ }\mu\text{A}$	-1.0	-1.8	-3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		7		$\text{mV}/^\circ\text{C}$
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -10\text{ V}, I_D = -15.2\text{ A}$		5.2	6.8	$\text{m}\Omega$
		$V_{GS} = -4.5\text{ V}, I_D = -11.2\text{ A}$		7.8	12.5	
		$V_{GS} = -10\text{ V}, I_D = -15.2\text{ A}, T_J = 125\text{ }^\circ\text{C}$		7.5	9.8	
g_{FS}	Forward Transconductance	$V_{DS} = -5\text{ V}, I_D = -15.2\text{ A}$		76		S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		4444	5915	pF
C_{oss}	Output Capacitance			781	1040	
C_{rss}	Reverse Transfer Capacitance			695	1045	
R_g	Gate Resistance			4.5		Ω

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -15\text{ V}, I_D = -15.2\text{ A}, V_{GS} = -10\text{ V}, R_{GEN} = 6\text{ }\Omega$		14	26	ns
t_r	Rise Time			28	45	
$t_{d(off)}$	Turn-Off Delay Time			97	156	
t_f	Fall Time			79	127	

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ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS						
Q _g	Total Gate Charge	V _{GS} = 0 V to -10 V, V _{DD} = -15 V, I _D = -15.2 A		93	130	nC
		V _{GS} = 0 V to -5 V, V _{DD} = -15 V, I _D = -15.2 A		52	73	
Q _{gs}	Gate to Source Charge	V _{DD} = -15 V, I _D = -15.2 A		13		nC
Q _{gd}	Gate to Drain "Miller" Charge			26		nC

DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = -2.1 A (Note 2)		0.7	1.20	V
		V _{GS} = 0 V, I _S = -15.2 A (Note 2)		0.8	1.25	
t _{rr}	Reverse Recovery Time	I _F = -15.2 A, di/dt = 100 A/μs		33	53	ns
Q _{rr}	Reverse Recovery Charge			20	32	nC

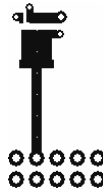
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

- R_{θJA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.



a. 50 °C/W when mounted on a 1 in² pad of 2 oz copper.



b. 125 °C/W when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
- The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.
- Pulsed I_d please refer to Figure 11 SOA graph for more details.
- Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal electro-mechanical application board design.

TYPICAL CHARACTERISTICS ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted)

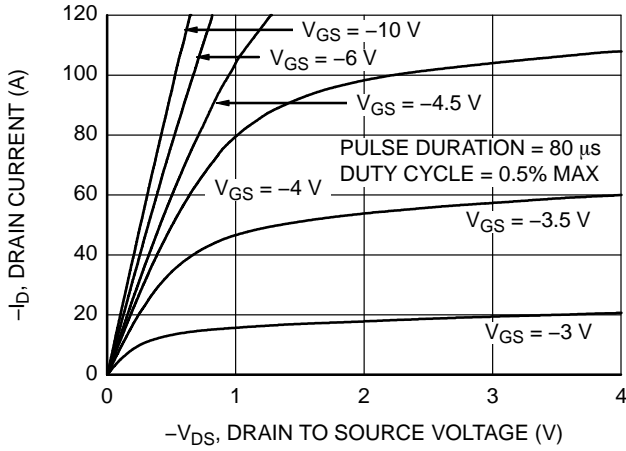


Figure 1. On Region Characteristics

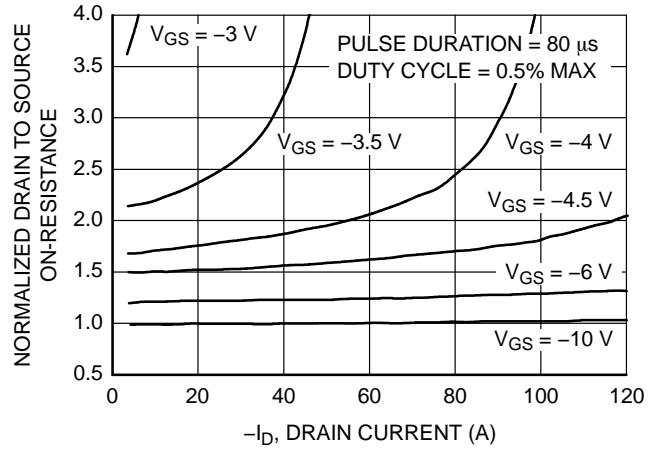


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

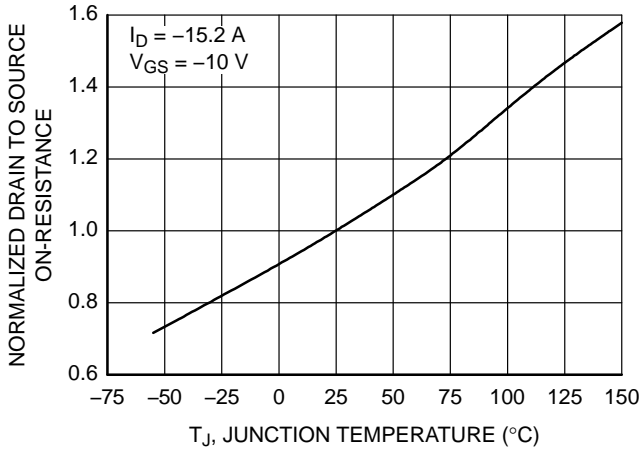


Figure 3. Normalized On Resistance vs. Junction Temperature

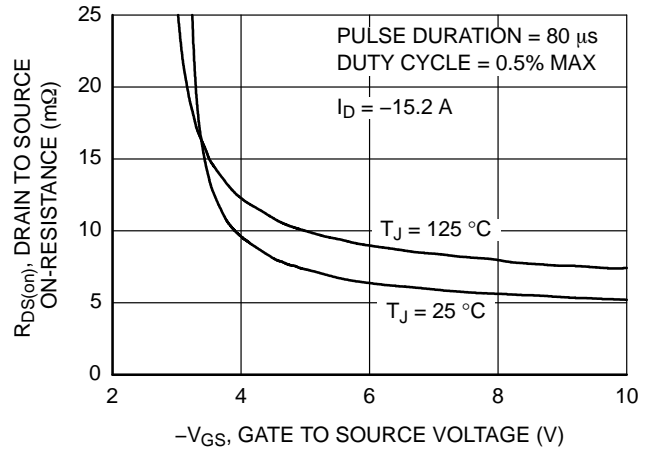


Figure 4. On-Resistance vs. Gate to Source Voltage

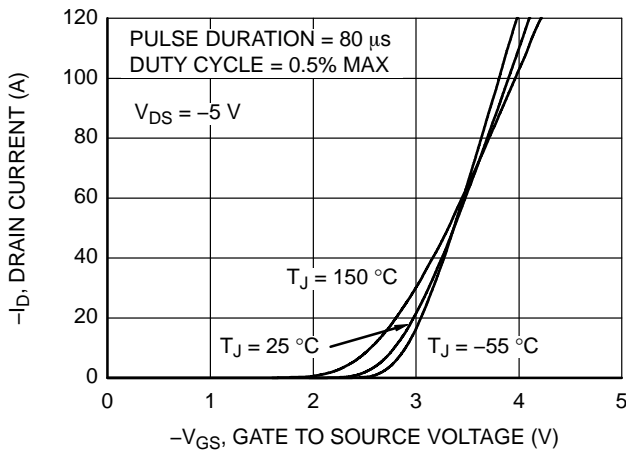


Figure 5. Transfer Characteristics

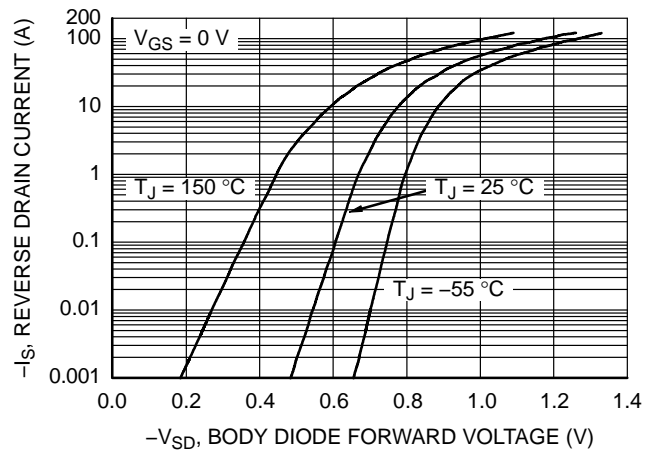


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

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TYPICAL CHARACTERISTICS ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted) (continued)

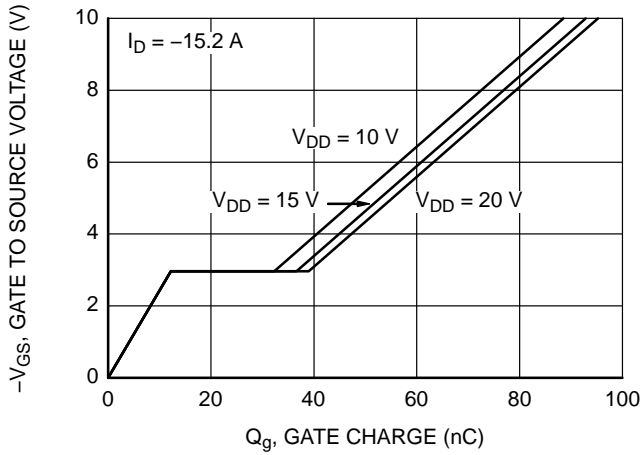


Figure 7. Gate Charge Characteristics

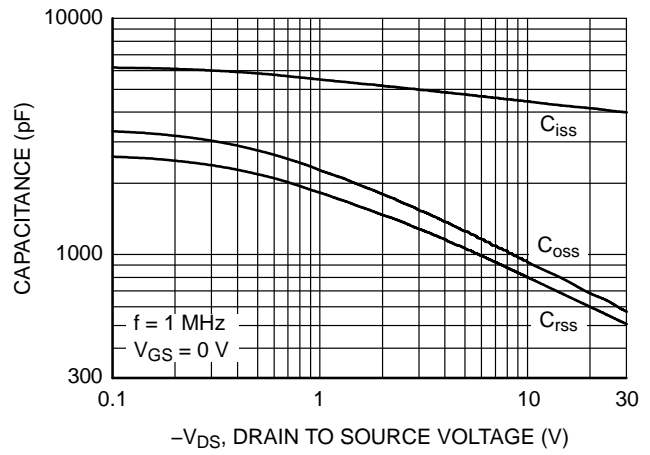


Figure 8. Capacitance vs. Drain to Source Voltage

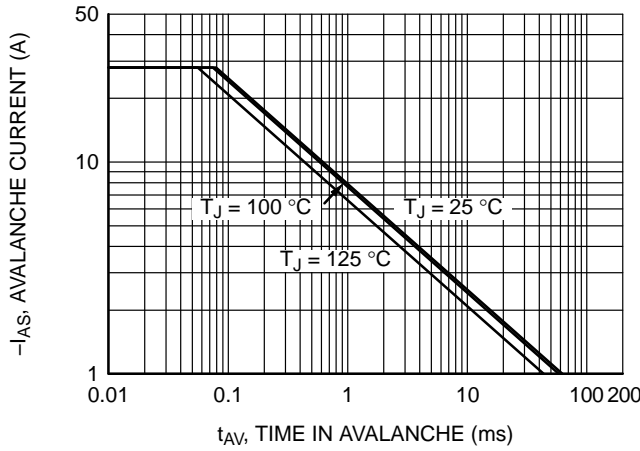


Figure 9. Unclamped Inductive Switching Capability

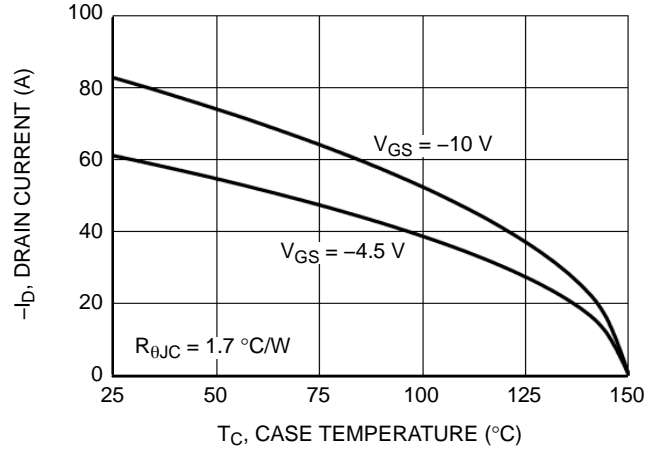


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

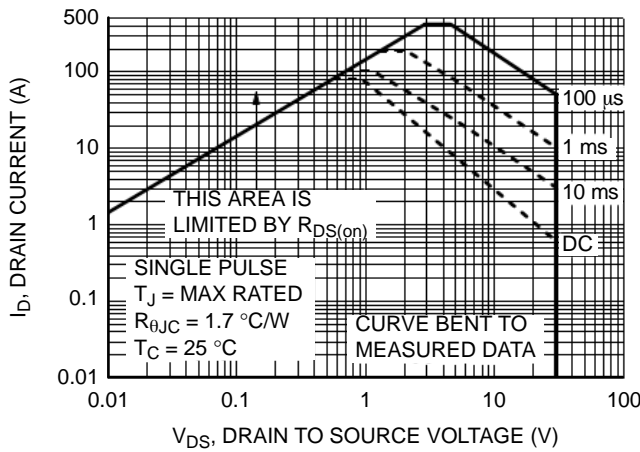


Figure 11. Forward Bias Safe Operating Area

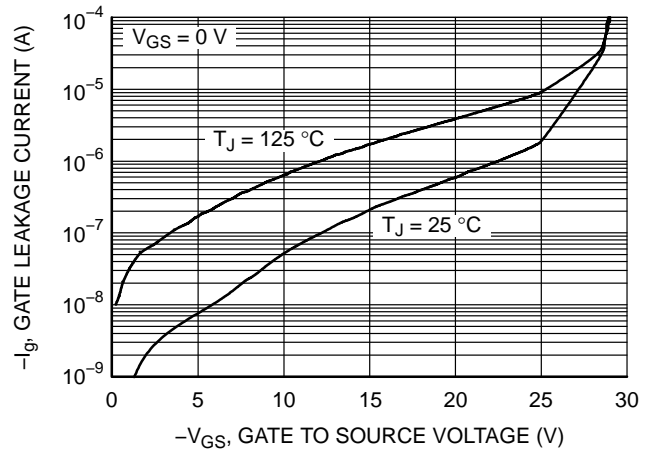


Figure 12. I_{gss} vs. V_{gss}

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TYPICAL CHARACTERISTICS ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted) (continued)

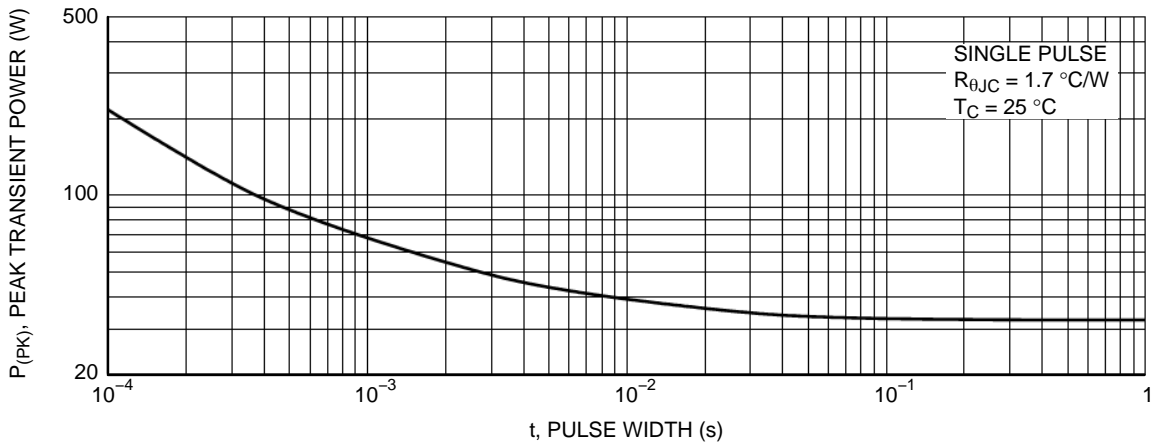


Figure 13. Single Pulse Maximum Power Dissipation

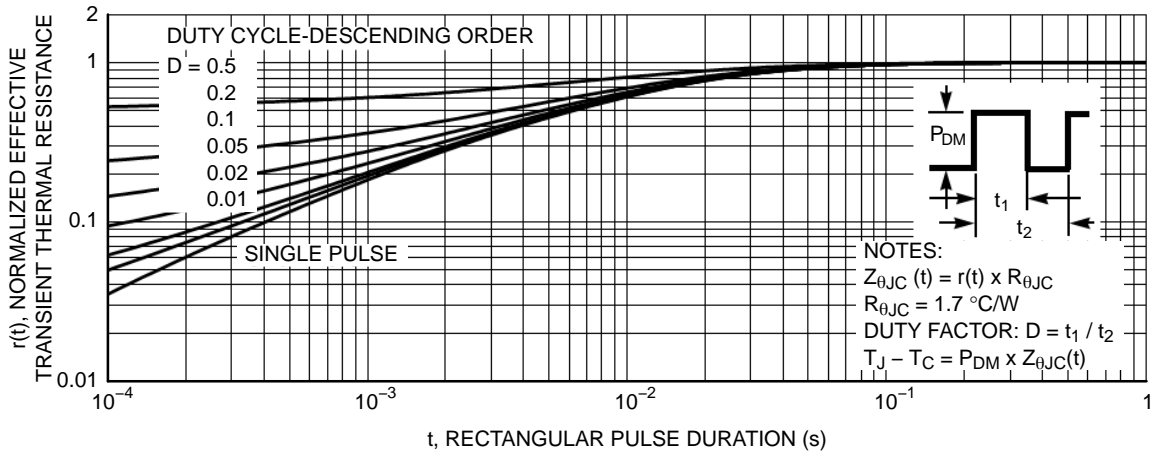


Figure 14. Junction-to-Case Transient Thermal Response Curve

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package Type	Reel Size	Tape Width	Shipping [†]
FDMS6673BZ	FDMS6673BZ	PQFN8 5X6, 1.27P Power 56	13"	12 mm	3000 / Tape & Reel
FDMS6673BZ-NC					

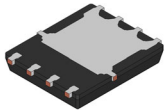
[†] For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

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REVISION HISTORY

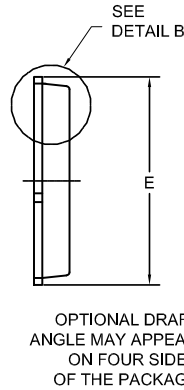
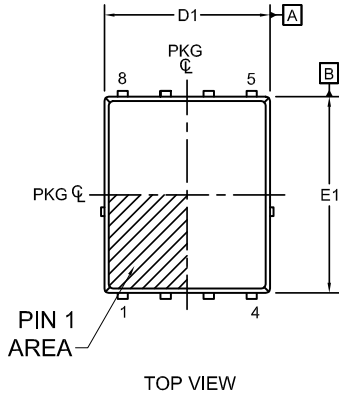
Revision	Description of Changes	Date
2	Converted the document to onsemi format. Added new OPN.	6/1/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.



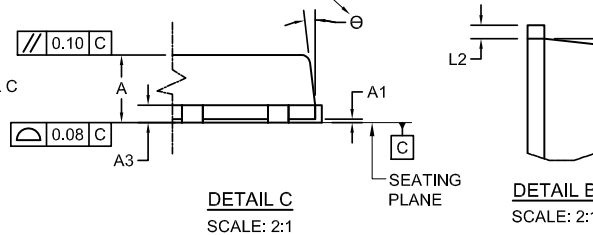
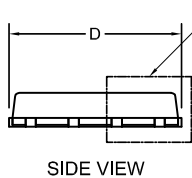
PQFN8 5X6, 1.27P
CASE 483AE
ISSUE C

DATE 21 JAN 2022

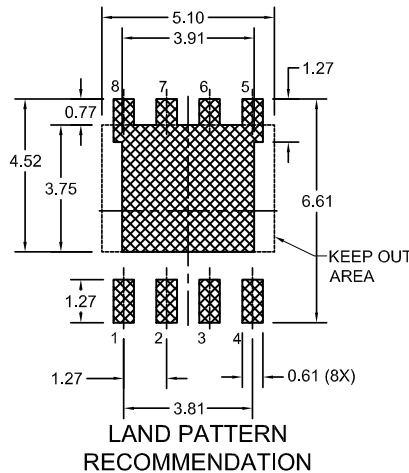
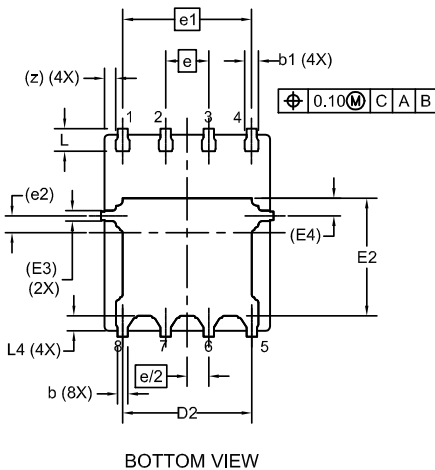


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
b	0.21	0.31	0.41
b1	0.31	0.41	0.51
A3	0.15	0.25	0.35
D	4.90	5.00	5.20
D1	4.80	4.90	5.00
D2	3.61	3.82	3.96
E	5.90	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.78
E3	0.30 REF		
E4	0.52 REF		
e	1.27 BSC		
e/2	0.635 BSC		
e1	3.81 BSC		
e2	0.50 REF		
L	0.51	0.66	0.76
L2	0.05	0.18	0.30
L4	0.34	0.44	0.54
z	0.34 REF		
θ	0°	-	12°



*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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