

Constant Voltage / Constant Current Secondary-Side Controller

NCS1002



SOIC-8
D SUFFIX
CASE 751

Description

The NCS1002 is a highly integrated solution for Switching Mode Power Supply (SMPS) applications requiring a dual control loop to perform Constant Voltage (CV) and Constant Current (CC) regulation. The NCS1002 integrates a 2.5 V voltage reference and two precision op amps. The voltage reference, along with Op Amp 1, is the core of the voltage control-loop. Op Amp 2 is an independent, uncommitted amplifier specifically designed for the current control. Key external components needed to complete the two control loops are: (a) A resistor divider that senses the output of the power supply (battery charger) and fixes the voltage regulation set point at the specified value. (b) A sense resistor that feeds the current sensing circuit with a voltage proportional to the DC output current. This resistor determines the current regulation set point and must be adequately rated in terms of power dissipation. The NCS1002 comes in a small 8-pin SOIC package and is ideal for space-shrunk applications such as battery chargers.

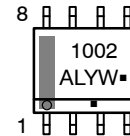
Features

- Low Input Offset Voltage: 0.5 mV, Typ
- Input Common-Mode Range includes Ground
- Low Quiescent Current: 300 μ A per Op Amp at $V_{CC} = 5$ V
- Large Output Voltage Swing
- Wide Power Supply Range: 3 V to 32 V
- High ESD Protection: 2 kV
- These are Pb-Free Devices

Typical Applications

- Battery Chargers
- Switch Mode Power Supplies

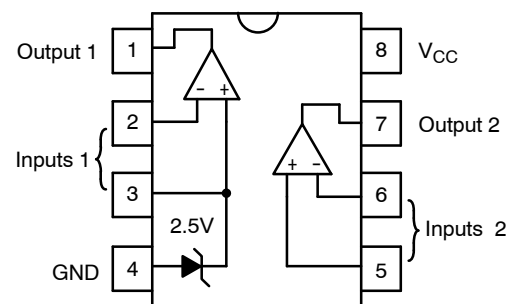
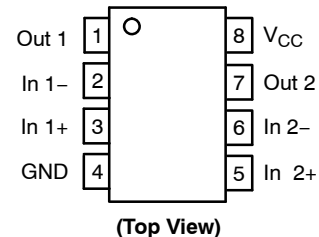
MARKING DIAGRAM



- A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
■ = Pb-Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
V_{CC}	Supply Voltage (V_{CC} to GND)	36	V
V_{id}	Differential Input Voltage	36	V
V_i	Input Voltage	-0.3 to +36	V
V_{ESD}	ESD Protection Voltage at Pin Human Body Model	2000	V
T_J	Maximum Junction Temperature	150	°C
T_A	Specification Temperature Range (T_{min} to T_{max})	-40 to +105	°C
T_{oper}	Operating Free-Air Temperature Range	-55 to +125	°C
T_{stg}	Storage Temperature Range	-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Rating	Unit
$R_{\theta JA}$	Thermal Resistance Junction-to-Ambient	175	°C/W



ELECTRICAL CHARACTERISTICS

Symbol	Characteristics	Conditions	Min	Typ	Max	Unit
I_{CC}	Total Supply Current, excluding current in the Voltage Reference $V_{CC} = 5\text{ V}$, no load; $-40 \leq T_A \leq +105^\circ\text{C}$			0.3	0.4	mA
I_{CC}	Total Supply Current, excluding Current in the Voltage Reference $V_{CC} = 30\text{ V}$, no load; $-40 \leq T_A \leq +105^\circ\text{C}$				0.75	mA

OP AMP 1 (OP AMP WITH NONINVERTING INPUT CONNECTED TO THE INTERNAL V_{ref}) $(V_{CC} = 5\text{ V}, T_A = 25^\circ\text{C}$ unless otherwise noted)

V_{IO}	Input Offset Voltage	$T_A = 25^\circ\text{C}$			2.0	mV
		$-40 \leq T_A \leq +105^\circ\text{C}$			3.0	mV
DV_{IO}	Input Offset Voltage Drift ($-40 \leq T_A \leq +105^\circ\text{C}$)			7.0		$\mu\text{V}/^\circ\text{C}$
I_{IB}	Input Bias Current (Inverting Input Only) $T_A = 25^\circ\text{C}$			20		nA
AVD	Large Signal Voltage Gain ($V_{CC} = 15\text{ V}$, $R_L = 2\text{ k}\Omega$, $V_{ICM} = 0\text{ V}$)			100		V/mV
PSRR	Power Supply Rejection ($V_{CC} = 5.0\text{ V}$ to 30 V , $V_{OUT} = 2\text{ V}$)		80	100		dB
I_{SOURCE}	Output Source Current ($V_{CC} = 15\text{ V}$, $V_{OUT} = 2.0\text{ V}$, $V_{id} = 1\text{ V}$)		20	40		mA
I_O	Short Circuit to GND ($V_{CC} = 15\text{ V}$)			40	60	mA
I_{SINK}	Output Current Sink ($V_{id} = -1\text{ V}$)	$V_{CC} = +15\text{ V}$, $V_{OUT} = 0.2\text{ V}$ (Note 1)	1	10		mA
		$V_{CC} = +15\text{ V}$, $V_{OUT} = 2\text{ V}$	10	20		mA
V_{OH}	Output Voltage Swing, High ($V_{CC} = 30\text{ V}$)	$R_L = 2\text{ k}\Omega$, $T_A = 25^\circ\text{C}$	26	27		V
		$-40 \leq T_A \leq +105^\circ\text{C}$	26			
		$R_L = 10\text{ k}\Omega$, $T_A = 25^\circ\text{C}$	27	28		
		$-40 \leq T_A \leq +105^\circ\text{C}$	27			
V_{OL}	Output Voltage Swing, Low	$R_L = 10\text{ k}\Omega$, $T_A = 25^\circ\text{C}$		5.0	50	mV
		$-40 \leq T_A \leq +105^\circ\text{C}$			50	
SR	Slew Rate ($AV = +1$, $V_i = 0.5\text{ V}$ to 2 V , $V_{CC} = 15\text{ V}$, $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$)		0.2	0.4		V/ μs
GBP	Gain Bandwidth Product ($V_{CC} = 30\text{ V}$, $AV = +1$, (Note 1) $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$, $f = 100\text{ kHz}$, $V_{IN} = 10\text{ mV}_{PP}$)		0.5	0.9		MHz
THD	Total Harmonic Distortion ($f = 1\text{ kHz}$, $AV = 10$, $R_L = 2\text{ k}\Omega$, $V_{CC} = 30\text{ V}$, $V_{OUT} = 2\text{ V}_{PP}$)			0.08		%

OP AMP 2 (INDEPENDENT OP AMP) ($V_{CC} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$ unless otherwise noted)

V_{IO}	Input Offset Voltage	$T_A = 25^\circ\text{C}$		0.5	2.0	mV
		$-40 \leq T_A \leq +105^\circ\text{C}$			3.0	
DV_{IO}	Input Offset Voltage Drift ($-40 \leq T_A \leq +105^\circ\text{C}$)			7.0		$\mu\text{V}/^\circ\text{C}$
I_{IO}	Input Offset Current	$T_A = 25^\circ\text{C}$		2.0	75	nA
		$-40 \leq T_A \leq +105^\circ\text{C}$			150	
I_B	Input Bias Current	$T_A = 25^\circ\text{C}$		20	150	nA
		$-40 \leq T_A \leq +105^\circ\text{C}$			200	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Guaranteed by design and/or characterization.
2. The input common-mode voltage of either input signal should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode range is $V_{CC} - 1.5\text{ V}$. Both inputs can go to $V_{CC} + 0.3\text{ V}$ without damage.
3. The Dynamic Impedance is defined as $|Z_{KA}| = \Delta V_{KA} / \Delta I_K$.
4. Guaranteed by design and/or characterization.



ELECTRICAL CHARACTERISTICS (continued)

Symbol	Characteristics	Conditions	Min	Typ	Max	Unit
OP AMP 2 (INDEPENDENT OP AMP) (continued) ($V_{CC} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$ unless otherwise noted)						
AVD	Large Signal Voltage Gain ($V_{CC} = 15\text{ V}$, $R_L = 2\text{ k}\Omega$, $V_{OUT} = 1.4\text{ V}$ to 11.4 V)	$T_A = 25^\circ\text{C}$	50	100		V/mV
		$-40 \leq T_A \leq +105^\circ\text{C}$	25			
PSRR	Power Supply Rejection ($V_{CC} = 5\text{ V}$ to 30 V)		65	100		dB
V_{ICM}	Input Common Mode Voltage Range (Note 2) ($V_{CC} = +30\text{ V}$)	$T_A = 25^\circ\text{C}$	0		$V_{CC} - 1.5$	V
		$-40 \leq T_A \leq +105^\circ\text{C}$	0		$V_{CC} - 2.0$	
CMRR	Common Mode Rejection Ratio (Note 4)	0 to $V_{CC} - 1.7\text{ V}$, $T_A = 25^\circ\text{C}$	70	85		dB
		0 to $V_{CC} - 2.2\text{ V}$, $-40 \leq T_A \leq +105^\circ\text{C}$	60			
I_{SOURCE}	Output Current Source ($V_{CC} = 15\text{ V}$, $V_{OUT} = 2\text{ V}$, $V_{ID} = +1\text{ V}$)		20	40		mA
I_O	Short-Circuit to GND ($V_{CC} = 15\text{ V}$)			40	60	mA
I_{SINK}	Output Current Sink ($V_{ID} = -1\text{ V}$)	$V_{CC} = +15\text{ V}$, $V_{OUT} = 0.2\text{ V}$	1	10		mA
		$V_{CC} = +15\text{ V}$, $V_{OUT} = 2\text{ V}$	10	20		mA
V_{OH}	Output Voltage Swing, High ($V_{CC} = 30\text{ V}$)	$R_L = 2\text{ k}\Omega$, $T_A = 25^\circ\text{C}$	26	27		V
		$-40 \leq T_A \leq +105^\circ\text{C}$	26			
		$R_L = 10\text{ k}\Omega$, $T_A = 25^\circ\text{C}$	27	28		
		$-40 \leq T_A \leq +105^\circ\text{C}$	27			
V_{OL}	Output Voltage Swing, Low	$R_L = 10\text{ k}\Omega$, $T_A = 25^\circ\text{C}$		5.0	50	mV
		$-40 \leq T_A \leq +105^\circ\text{C}$			50	
SR	Slew Rate ($AV = +1$, $V_i = 0.5\text{ V}$ to 3 V , $V_{CC} = 15\text{ V}$, $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$)		0.2	0.4		V/ μs
GBP	Gain Bandwidth Product ($V_{CC} = 30\text{ V}$, $AV = +1$, $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$, $f = 100\text{ kHz}$, $V_{IN} = 10\text{ mV}_{PP}$) (Note 4)		0.5	0.9		MHz
THD	Total Harmonic Distortion ($f = 1\text{ kHz}$, $AV = 10$, $R_L = 2\text{ k}\Omega$, $V_{CC} = 30\text{ V}$, $V_{OUT} = 2\text{ V}_{PP}$)			0.08		%
e_{noise}	Equivalent Input Noise Voltage ($f = 1\text{ kHz}$, $R_S = 100\text{ }\Omega$, $V_{CC} = 30\text{ V}$)			50		nV/ $\sqrt{\text{Hz}}$

VOLTAGE REFERENCE (continued) ($V_{CC} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$ unless otherwise noted)

I_K	Cathode Current		0.075		100	mA
V_{ref}	Reference Voltage ($I_K = 1\text{ mA}$)	$T_A = 25^\circ\text{C}$	2.49	2.5	2.51	V
		$-40 \leq T_A \leq +105^\circ\text{C}$	2.48	2.5	2.52	
ΔV_{ref}	Reference Deviation over Temperature ($V_{KA} = V_{ref}$, $I_K = 10\text{ mA}$, $-40 \leq T_A \leq +105^\circ\text{C}$) (Note 4)			7.0	30	mV
I_{min}	Minimum Cathode Current for Regulation ($2.4875\text{ V}_f \leq V_{KA} \leq 2.5125\text{ V}_f$)			40	75	μA
$ Z_{KA} $	Dynamic Impedance (Note 3) ($V_{KA} = V_{ref}$, $I_K = 1\text{ mA}$ to 100 mA , $f < 1\text{ kHz}$)			0.2	0.5	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Guaranteed by design and/or characterization.
2. The input common-mode voltage of either input signal should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode range is $V_{CC} - 1.5\text{ V}$. Both inputs can go to $V_{CC} + 0.3\text{ V}$ without damage.
3. The Dynamic Impedance is defined as $|Z_{KA}| = \Delta V_{KA} / \Delta I_K$.
4. Guaranteed by design and/or characterization.



TYPICAL CHARACTERISTICS

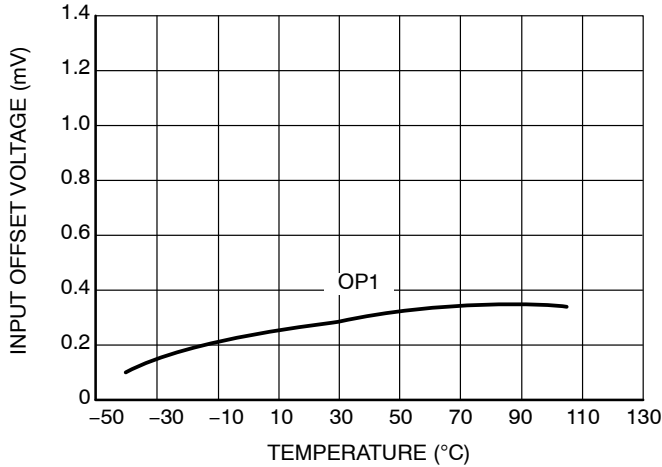


Figure 1. Input Offset Voltage vs. Temperature

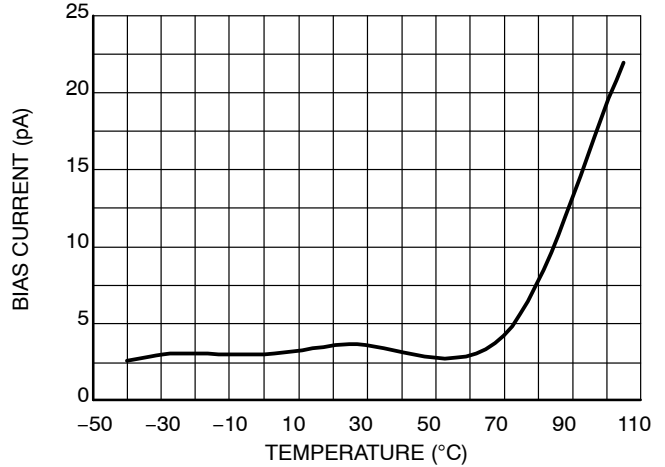


Figure 2. IB vs. Temperature

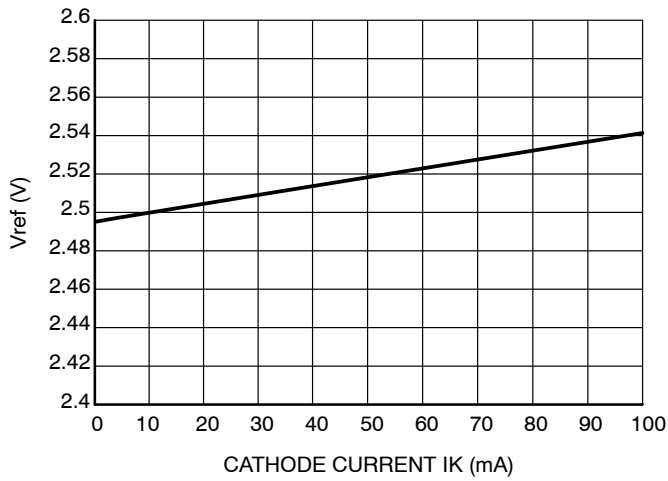


Figure 3. Vref as a Function of IK

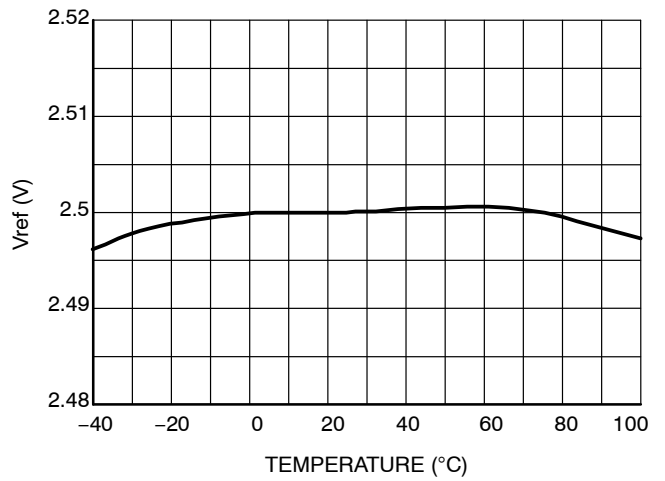


Figure 4. Vref Over Temperature

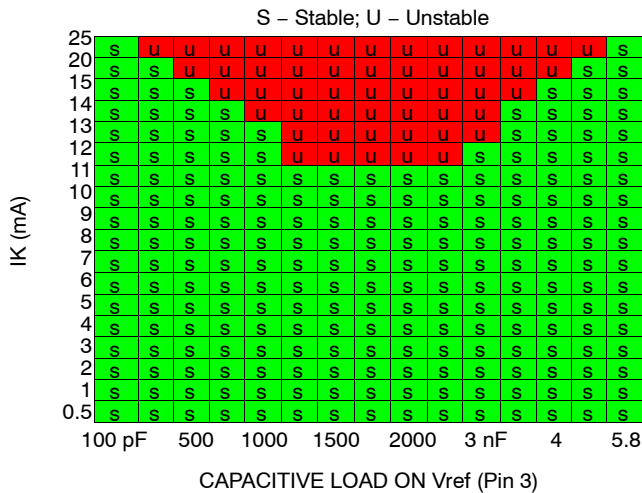


Figure 5. Region of Reference Stability vs. Capacitive Load (Pin 3)

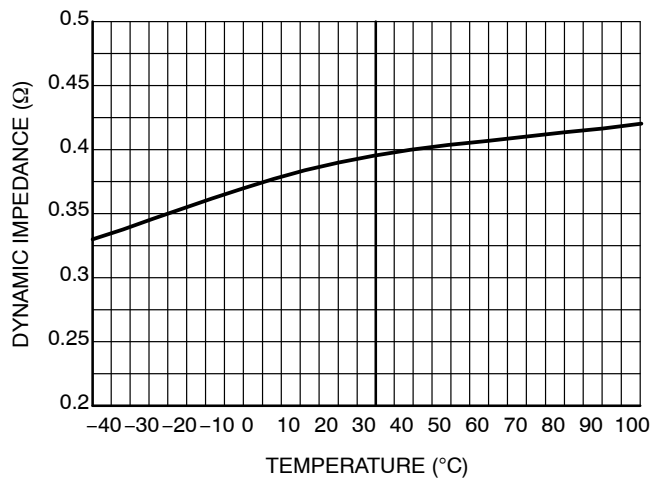


Figure 6. Ref Dynamic Impedance vs. Temperature

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TYPICAL CHARACTERISTICS

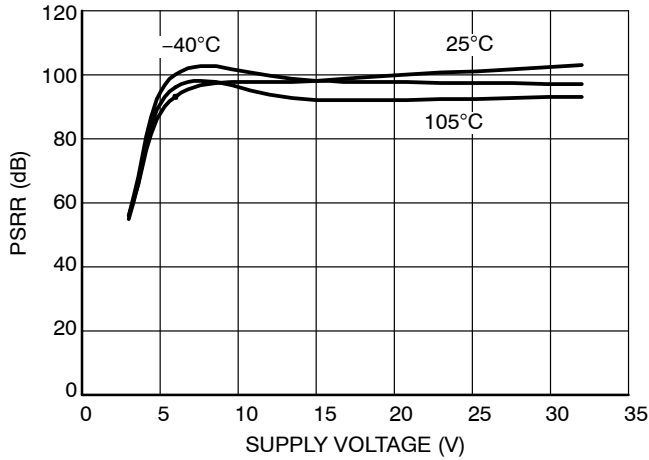


Figure 7. NCS1002 PSRR vs. Supply Voltage

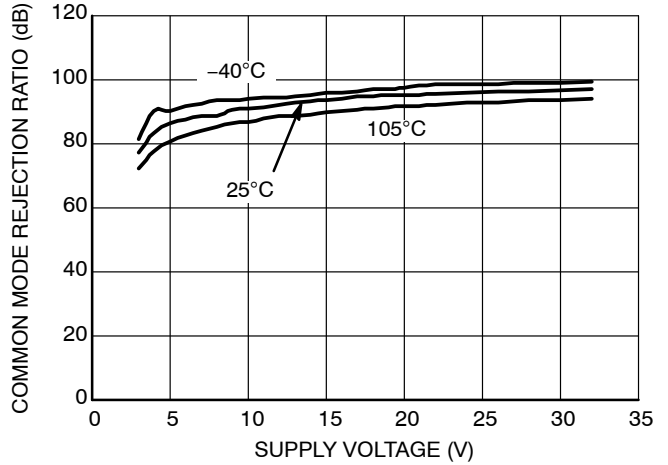


Figure 8. NCS1002 CMRR vs. Supply Voltage

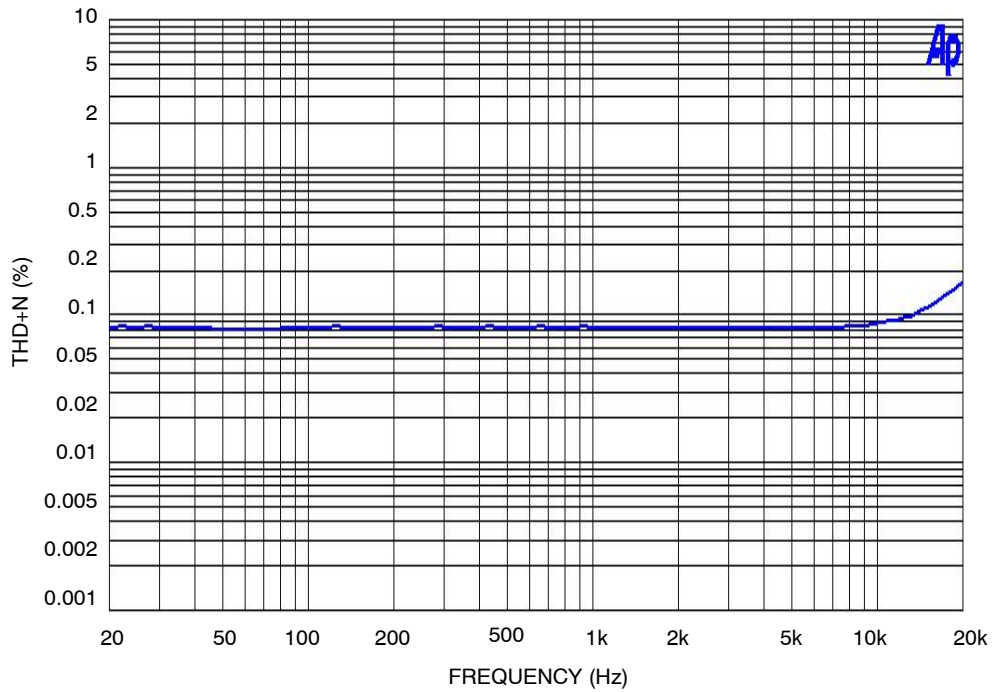


Figure 9. THD+N

ORDERING INFORMATION

Device	Package	Shipping†
NCS1002DR2G	SOIC-8 (Pb-Free)	2,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

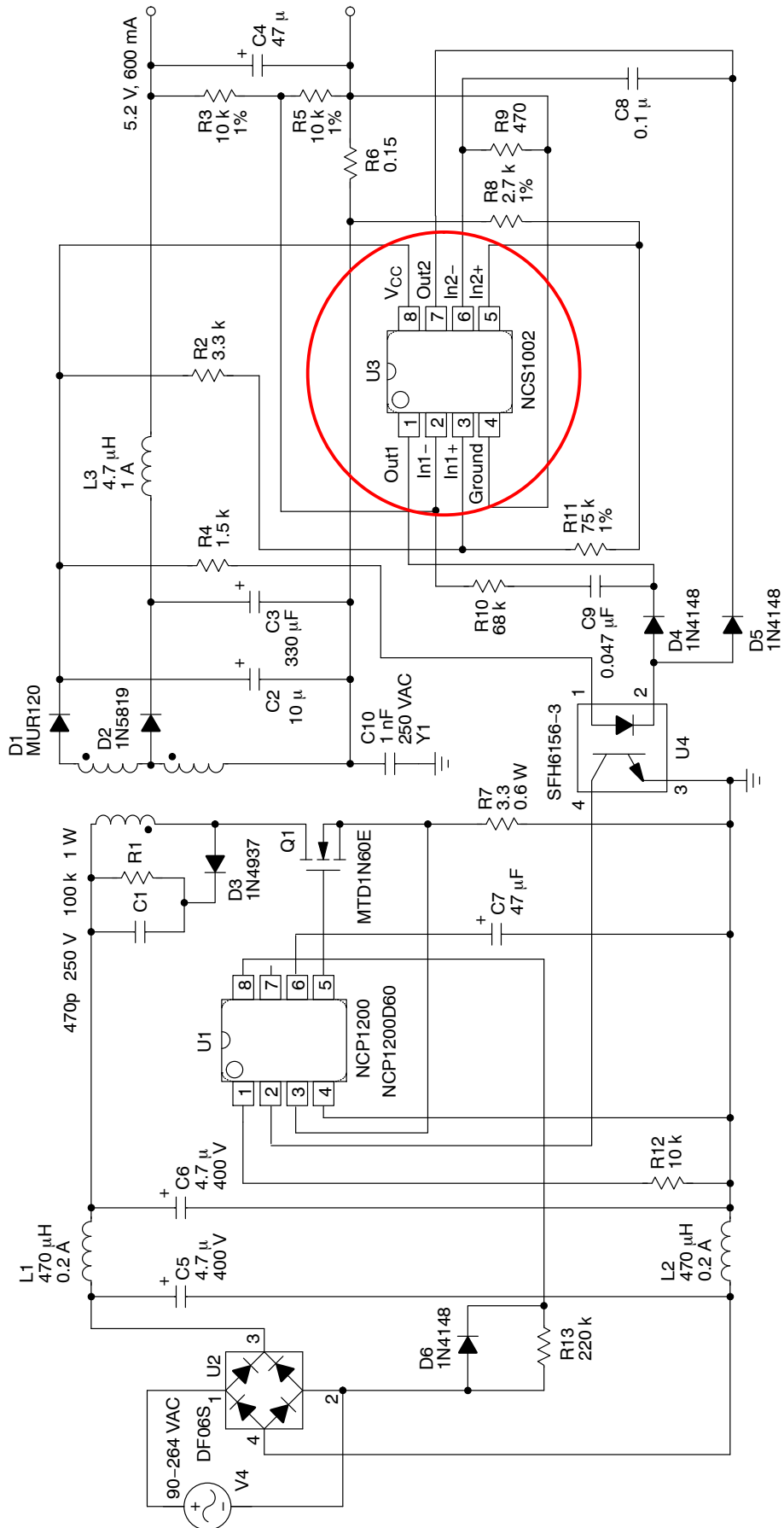
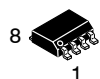


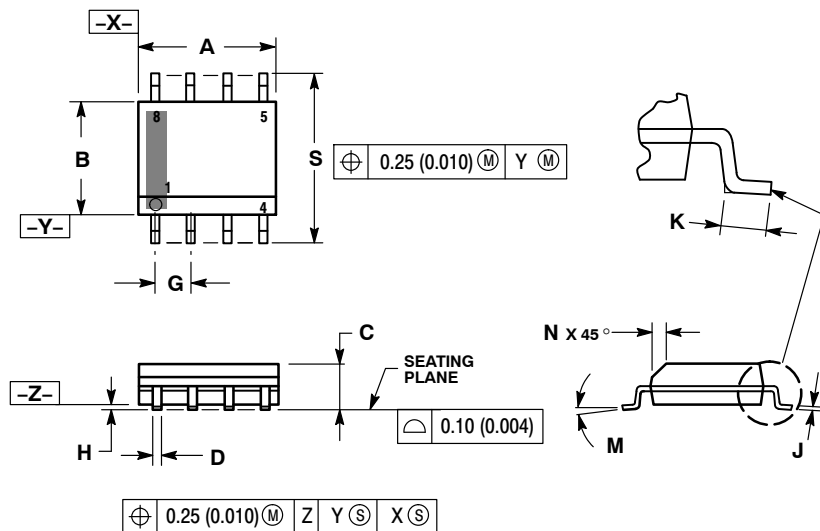
Figure 1. AC Adapter Application



SCALE 1:1

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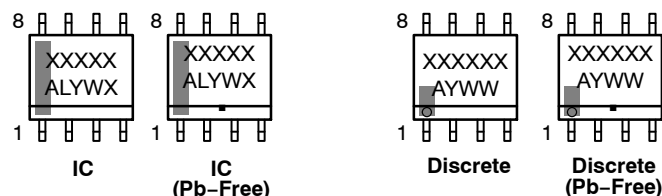
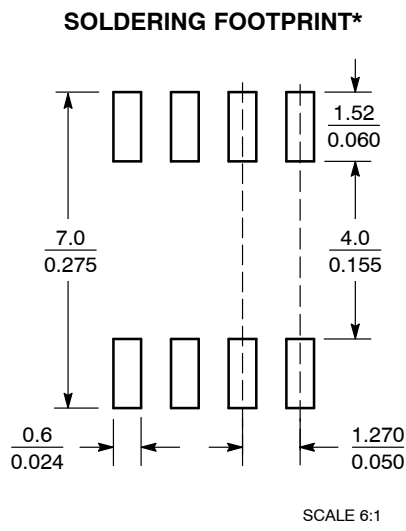


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

GENERIC
MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-8 NB	PAGE 1 OF 2

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STYLE 1: PIN 1. EMITTER 2. COLLECTOR 3. COLLECTOR 4. EMITTER 5. EMITTER 6. BASE 7. BASE 8. EMITTER	STYLE 2: PIN 1. COLLECTOR, DIE, #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. BASE, #2 6. EMITTER, #2 7. BASE, #1 8. EMITTER, #1	STYLE 3: PIN 1. DRAIN, DIE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. GATE, #2 6. SOURCE, #2 7. GATE, #1 8. SOURCE, #1	STYLE 4: PIN 1. ANODE 2. ANODE 3. ANODE 4. ANODE 5. ANODE 6. ANODE 7. ANODE 8. COMMON CATHODE
STYLE 5: PIN 1. DRAIN 2. DRAIN 3. DRAIN 4. DRAIN 5. GATE 6. GATE 7. SOURCE 8. SOURCE	STYLE 6: PIN 1. SOURCE 2. DRAIN 3. DRAIN 4. SOURCE 5. SOURCE 6. GATE 7. GATE 8. SOURCE	STYLE 7: PIN 1. INPUT 2. EXTERNAL BYPASS 3. THIRD STAGE SOURCE 4. GROUND 5. DRAIN 6. GATE 3 7. SECOND STAGE Vd 8. FIRST STAGE Vd	STYLE 8: PIN 1. COLLECTOR, DIE #1 2. BASE, #1 3. BASE, #2 4. COLLECTOR, #2 5. COLLECTOR, #2 6. EMITTER, #2 7. EMITTER, #1 8. COLLECTOR, #1
STYLE 9: PIN 1. EMITTER, COMMON 2. COLLECTOR, DIE #1 3. COLLECTOR, DIE #2 4. EMITTER, COMMON 5. EMITTER, COMMON 6. BASE, DIE #2 7. BASE, DIE #1 8. EMITTER, COMMON	STYLE 10: PIN 1. GROUND 2. BIAS 1 3. OUTPUT 4. GROUND 5. GROUND 6. BIAS 2 7. INPUT 8. GROUND	STYLE 11: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. DRAIN 2 7. DRAIN 1 8. DRAIN 1	STYLE 12: PIN 1. SOURCE 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN
STYLE 13: PIN 1. N.C. 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN	STYLE 14: PIN 1. N-SOURCE 2. N-GATE 3. P-SOURCE 4. P-GATE 5. P-DRAIN 6. P-DRAIN 7. N-DRAIN 8. N-DRAIN	STYLE 15: PIN 1. ANODE 1 2. ANODE 1 3. ANODE 1 4. ANODE 1 5. CATHODE, COMMON 6. CATHODE, COMMON 7. CATHODE, COMMON 8. CATHODE, COMMON	STYLE 16: PIN 1. EMITTER, DIE #1 2. BASE, DIE #1 3. EMITTER, DIE #2 4. BASE, DIE #2 5. COLLECTOR, DIE #2 6. COLLECTOR, DIE #2 7. COLLECTOR, DIE #1 8. COLLECTOR, DIE #1
STYLE 17: PIN 1. VCC 2. V2OUT 3. V1OUT 4. TXE 5. RXE 6. VEE 7. GND 8. ACC	STYLE 18: PIN 1. ANODE 2. ANODE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. CATHODE 8. CATHODE	STYLE 19: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. MIRROR 2 7. DRAIN 1 8. MIRROR 1	STYLE 20: PIN 1. SOURCE (N) 2. GATE (N) 3. SOURCE (P) 4. GATE (P) 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN
STYLE 21: PIN 1. CATHODE 1 2. CATHODE 2 3. CATHODE 3 4. CATHODE 4 5. CATHODE 5 6. COMMON ANODE 7. COMMON ANODE 8. CATHODE 6	STYLE 22: PIN 1. I/O LINE 1 2. COMMON CATHODE/VCC 3. COMMON CATHODE/VCC 4. I/O LINE 3 5. COMMON ANODE/GND 6. I/O LINE 4 7. I/O LINE 5 8. COMMON ANODE/GND	STYLE 23: PIN 1. LINE 1 IN 2. COMMON ANODE/GND 3. COMMON ANODE/GND 4. LINE 2 IN 5. LINE 2 OUT 6. COMMON ANODE/GND 7. COMMON ANODE/GND 8. LINE 1 OUT	STYLE 24: PIN 1. BASE 2. EMITTER 3. COLLECTOR/ANODE 4. COLLECTOR/ANODE 5. CATHODE 6. CATHODE 7. COLLECTOR/ANODE 8. COLLECTOR/ANODE
STYLE 25: PIN 1. VIN 2. N/C 3. REXT 4. GND 5. IOUT 6. IOUT 7. IOUT 8. IOUT	STYLE 26: PIN 1. GND 2. dv/dt 3. ENABLE 4. ILIMIT 5. SOURCE 6. SOURCE 7. SOURCE 8. VCC	STYLE 27: PIN 1. ILIMIT 2. OVLO 3. UVLO 4. INPUT+ 5. SOURCE 6. SOURCE 7. SOURCE 8. DRAIN	STYLE 28: PIN 1. SW_TO_GND 2. DASIC_OFF 3. DASIC_SW_DET 4. GND 5. V_MON 6. VBULK 7. VBULK 8. VIN
STYLE 29: PIN 1. BASE, DIE #1 2. EMITTER, #1 3. BASE, #2 4. EMITTER, #2 5. COLLECTOR, #2 6. COLLECTOR, #2 7. COLLECTOR, #1 8. COLLECTOR, #1	STYLE 30: PIN 1. DRAIN 1 2. DRAIN 1 3. GATE 2 4. SOURCE 2 5. SOURCE 1/DRAIN 2 6. SOURCE 1/DRAIN 2 7. SOURCE 1/DRAIN 2 8. GATE 1		

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