

MOSFET – Power, Complementary, ChipFET™

20 V, +3.9 A /-4.4 A

NTHD3100C

Features

- Complementary N-Channel and P-Channel MOSFET
- Small Size, 40% Smaller than TSOP-6 Package
- Leadless SMD Package Provides Great Thermal Characteristics
- Trench P-Channel for Low On Resistance
- Low Gate Charge N-Channel for Test Switching
- Pb-Free Packages are Available

Applications

- DC-DC Conversion Circuits
- Load Switch Applications Requiring Level Shift
- Drive Small Brushless DC Motors
- Ideal for Power Management Applications in Portable, Battery Powered Products

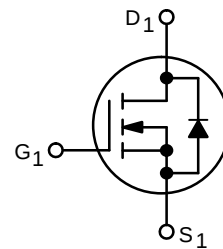
MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DS}	20	V
Gate-to-Source Voltage	N-Ch		V_{GS}	± 12	V
	P-Ch			± 8.0	
N-Channel Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	I_D	2.9	A
		$T_A = 85^\circ\text{C}$		2.1	
	$t \leq 10\text{ s}$	$T_A = 25^\circ\text{C}$		3.9	
		$T_A = 85^\circ\text{C}$		-2.3	
P-Channel Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	I_D	-3.2	A
		$T_A = 85^\circ\text{C}$		-2.3	
	$t \leq 10\text{ s}$	$T_A = 25^\circ\text{C}$		-4.4	
		$T_A = 85^\circ\text{C}$		-4.4	
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	P_D	1.1	W
		$t \leq 5\text{ s}$		3.1	
Pulsed Drain Current (Note 1)	N-Ch	$t = 10\text{ }\mu\text{s}$	I_{DM}	12	A
	P-Ch	$t = 10\text{ }\mu\text{s}$		-13	
Operating Junction and Storage Temperature			T_J, T_{STG}	-55 to 150	$^\circ\text{C}$
Source Current (Body Diode)			I_S	2.5	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 seconds)			T_L	260	$^\circ\text{C}$

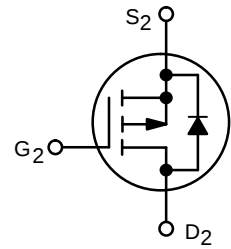
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).

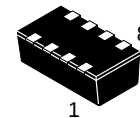
$V_{(BR)DSS}$	$R_{DS(on)}$ Typ	I_D MAX
N-Channel 20 V	58 m Ω @ 4.5 V	3.9 A
	77 m Ω @ 2.5 V	
P-Channel -20 V	64 m Ω @ -4.5 V	-4.4 A
	85 m Ω @ -2.5 V	



N-Channel MOSFET

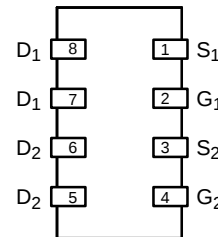


P-Channel MOSFET

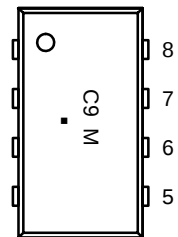


ChipFET
CASE 1206A
STYLE 2

PIN CONNECTIONS



MARKING DIAGRAM



- C9 = Specific Device Code
M = Month Code
■ = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 7.

NTHD3100C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	113	$^{\circ}\text{C/W}$
Junction-to-Ambient – $t \leq 10$ s (Note 2)	$R_{\theta JA}$	60	$^{\circ}\text{C/W}$

2. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	N/P	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS (Note 3)							
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	N	$V_{GS} = 0\text{ V}$	$I_D = 250\text{ }\mu\text{A}$	20		V
		P		$I_D = -250\text{ }\mu\text{A}$	-20		
Zero Gate Voltage Drain Current	I_{DSS}	N	$V_{GS} = 0\text{ V}, V_{DS} = 16\text{ V}$	$T_J = 25^{\circ}\text{C}$		1.0	μA
		P	$V_{GS} = 0\text{ V}, V_{DS} = -16\text{ V}$			-1.0	
		N	$V_{GS} = 0\text{ V}, V_{DS} = 16\text{ V}$	$T_J = 125^{\circ}\text{C}$		5.0	
		P	$V_{GS} = 0\text{ V}, V_{DS} = -16\text{ V}$			-5.0	
Gate-to-Source Leakage Current	I_{GSS}	N	$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$			± 100	nA
		P	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8.0\text{ V}$			± 100	

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	N	$V_{GS} = V_{DS}$	$I_D = 250\text{ }\mu\text{A}$	0.6	1.2	V
		P		$I_D = -250\text{ }\mu\text{A}$	-0.45	-1.5	
Drain-to-Source On Resistance	$R_{DS(on)}$	N	$V_{GS} = 4.5\text{ V}, I_D = 2.9\text{ A}$		58	80	m Ω
		P	$V_{GS} = -4.5\text{ V}, I_D = -3.2\text{ A}$		64	80	
		N	$V_{GS} = 2.5\text{ V}, I_D = 2.3\text{ A}$		77	115	
		P	$V_{GS} = -2.5\text{ V}, I_D = -2.2\text{ A}$		85	110	
Forward Transconductance	g_{FS}	N	$V_{DS} = 10\text{ V}, I_D = 2.9\text{ A}$		6.0		S
		P	$V_{DS} = -10\text{ V}, I_D = -3.2\text{ A}$		8.0		

CHARGES AND CAPACITANCES

Input Capacitance	C_{ISS}	N	$f = 1\text{ MHz}, V_{GS} = 0\text{ V}$	$V_{DS} = 10\text{ V}$		165	pF
		P		$V_{DS} = -10\text{ V}$		680	
Output Capacitance	C_{OSS}	N		$V_{DS} = 10\text{ V}$		80	
		P		$V_{DS} = -10\text{ V}$		100	
Reverse Transfer Capacitance	C_{RSS}	N		$V_{DS} = 10\text{ V}$		25	
		P		$V_{DS} = -10\text{ V}$		70	
Total Gate Charge	$Q_{G(TOT)}$	N		$V_{GS} = 4.5\text{ V}, V_{DS} = 10\text{ V}, I_D = 2.9\text{ A}$		2.3	nC
		P		$V_{GS} = -4.5\text{ V}, V_{DS} = -10\text{ V}, I_D = -3.2\text{ A}$		7.4	
Threshold Gate Charge	$Q_{G(TH)}$	N		$V_{GS} = 4.5\text{ V}, V_{DS} = 10\text{ V}, I_D = 2.9\text{ A}$		0.2	
		P		$V_{GS} = -4.5\text{ V}, V_{DS} = -10\text{ V}, I_D = -3.2\text{ A}$		0.6	
Gate-to-Source Gate Charge	Q_{GS}	N		$V_{GS} = 4.5\text{ V}, V_{DS} = 10\text{ V}, I_D = 2.9\text{ A}$		0.4	
		P		$V_{GS} = -4.5\text{ V}, V_{DS} = -10\text{ V}, I_D = -3.2\text{ A}$		1.4	
Gate-to-Drain "Miller" Charge	Q_{GD}	N		$V_{GS} = 4.5\text{ V}, V_{DS} = 10\text{ V}, I_D = 2.9\text{ A}$		0.7	
		P		$V_{GS} = -4.5\text{ V}, V_{DS} = -10\text{ V}, I_D = -3.2\text{ A}$		2.5	



NTHD3100C

ELECTRICAL CHARACTERISTICS (continued) ($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	N/P	Test Conditions	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS (Note 4)							
Turn-On Delay Time	$t_{d(ON)}$	N	$V_{GS} = 4.5\text{ V}$, $V_{DD} = 10\text{ V}$, $I_D = 2.9\text{ A}$, $R_G = 2.5\text{ }\Omega$		6.3		ns
Rise Time	t_r				10.7		
Turn-Off Delay Time	$t_{d(OFF)}$				9.6		
Fall Time	t_f				1.5		
Turn-On Delay Time	$t_{d(ON)}$	P	$V_{GS} = -4.5\text{ V}$, $V_{DD} = -10\text{ V}$, $I_D = -3.2\text{ A}$, $R_G = 2.5\text{ }\Omega$		5.8		
Rise Time	t_r				11.7		
Turn-Off Delay Time	$t_{d(OFF)}$				16		
Fall Time	t_f				12.4		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	N	$V_{GS} = 0\text{ V}$, $T_J = 25\text{ }^{\circ}\text{C}$	$I_S = 2.5\text{ A}$		0.8	1.15	V
		P		$I_S = -2.5\text{ A}$		-0.8	-1.2	
Reverse Recovery Time	t_{RR}	N	$V_{GS} = 0\text{ V}$, $dI_S / dt = 100\text{ A}/\mu\text{s}$	$I_S = 1.5\text{ A}$		12.5		ns
		P		$I_S = -1.5\text{ A}$		13.5		
Charge Time	t_a	N		$I_S = 1.5\text{ A}$		9.0		
		P		$I_S = -1.5\text{ A}$		9.5		
Discharge Time	t_b	N		$I_S = 1.5\text{ A}$		3.5		
		P		$I_S = -1.5\text{ A}$		4.0		
Reverse Recovery Charge	Q_{RR}	N		$I_S = 1.5\text{ A}$		6.0		nC
		P		$I_S = -1.5\text{ A}$		6.5		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: pulse width $\leq 250\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

4. Switching characteristics are independent of operating junction temperatures.



TYPICAL N-CHANNEL PERFORMANCE CURVES

($T_J = 25^\circ\text{C}$ unless otherwise noted)

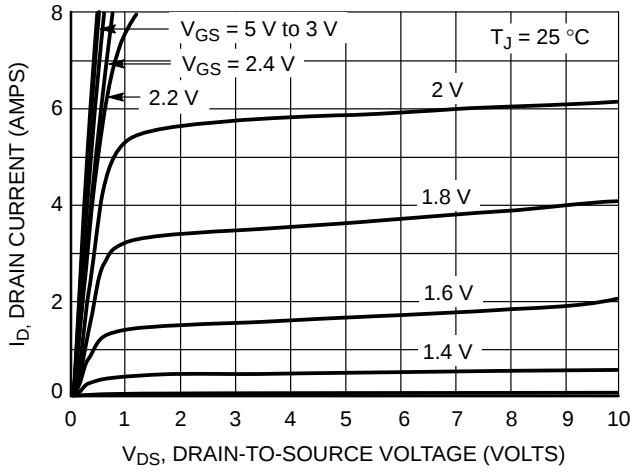


Figure 1. On-Region Characteristics

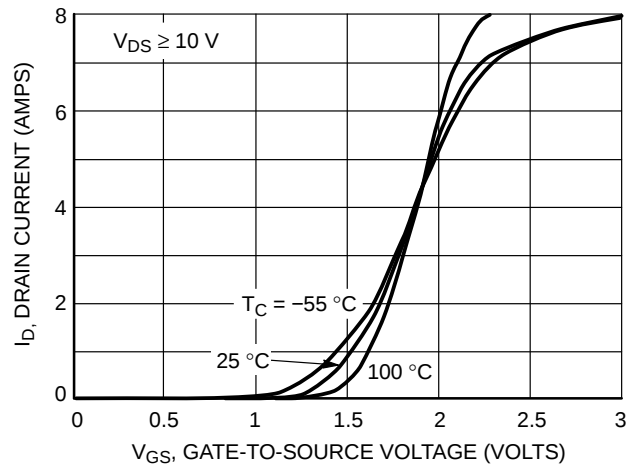


Figure 2. Transfer Characteristics

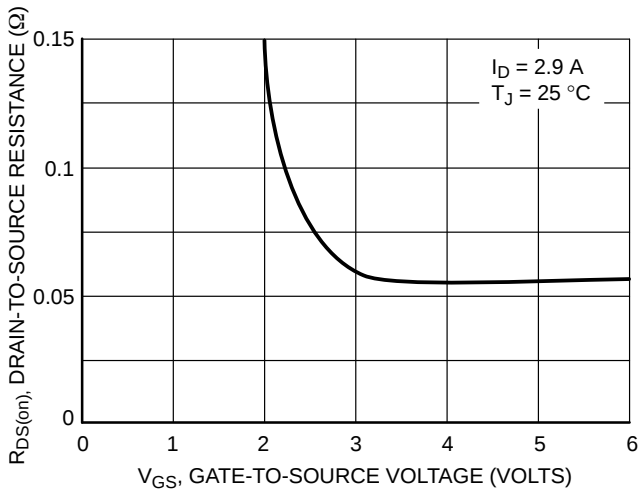


Figure 3. On-Resistance vs. Gate-to-Source Voltage

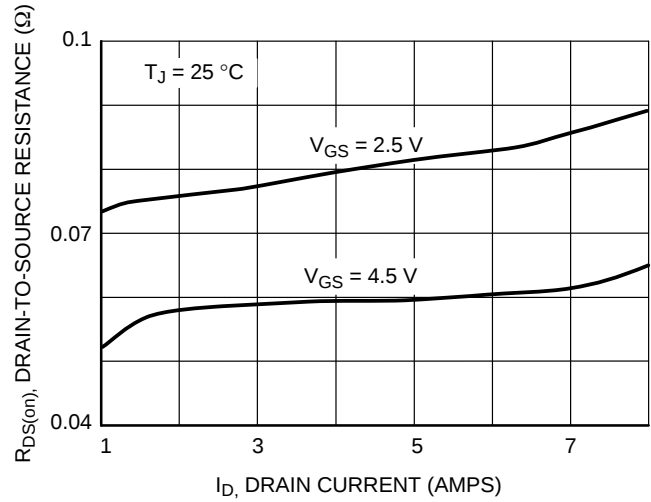


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

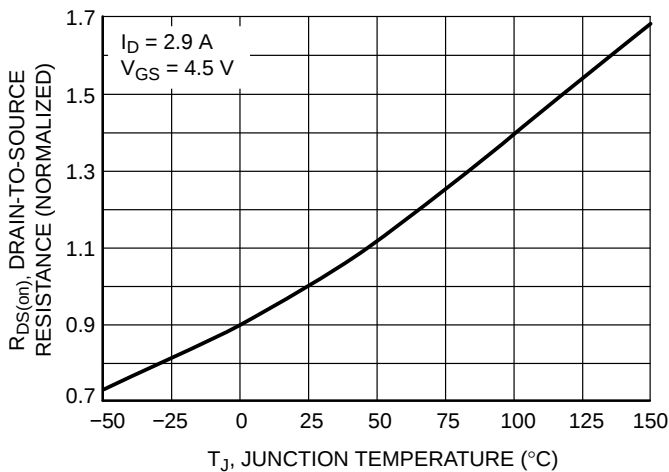


Figure 5. On-Resistance Variation with Temperature

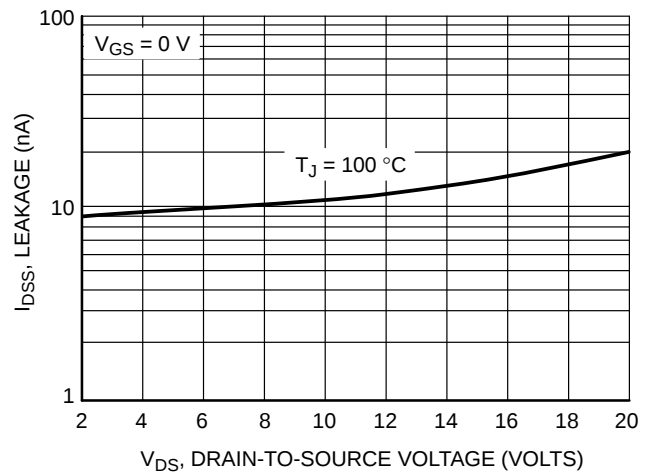
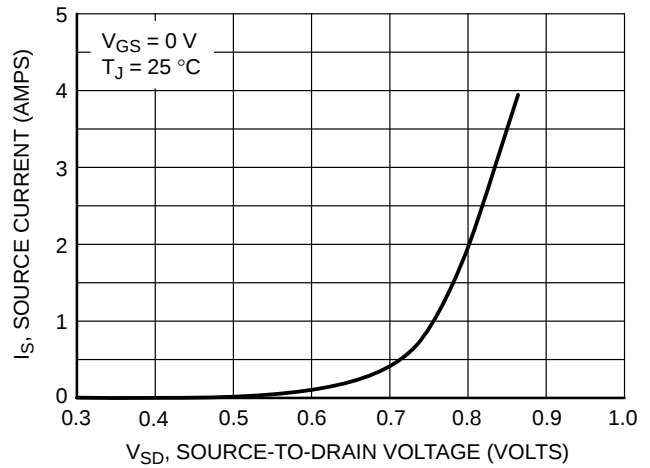
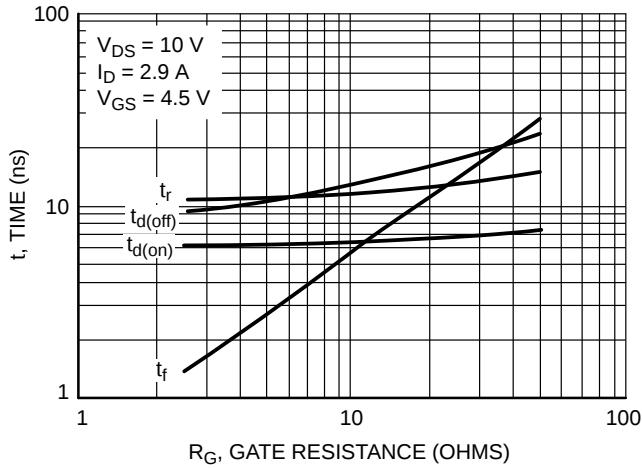
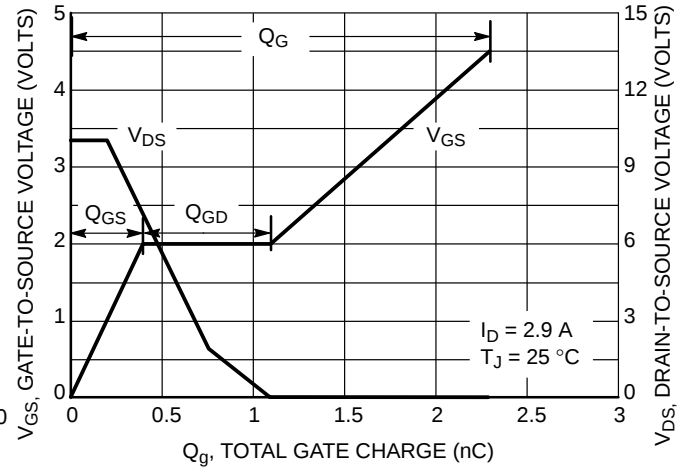
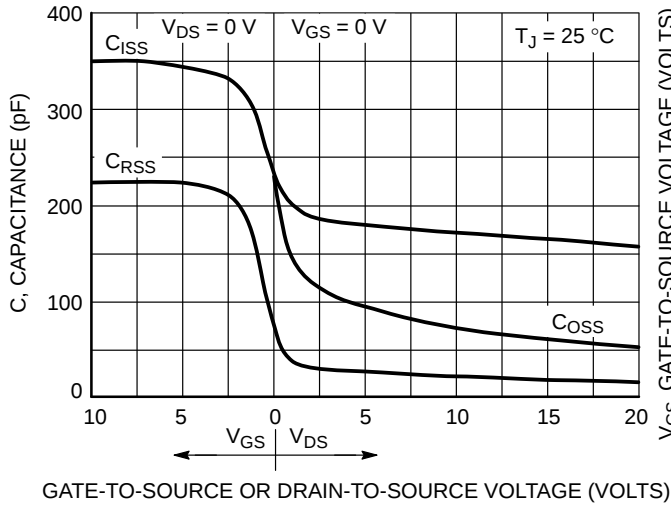


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL N-CHANNEL PERFORMANCE CURVES

($T_J = 25^\circ\text{C}$ unless otherwise noted)



TYPICAL P-CHANNEL PERFORMANCE CURVES

($T_J = 25^\circ\text{C}$ unless otherwise noted)

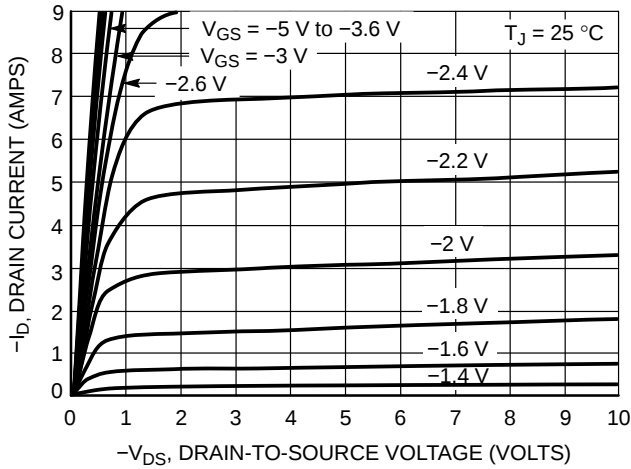


Figure 11. On-Region Characteristics

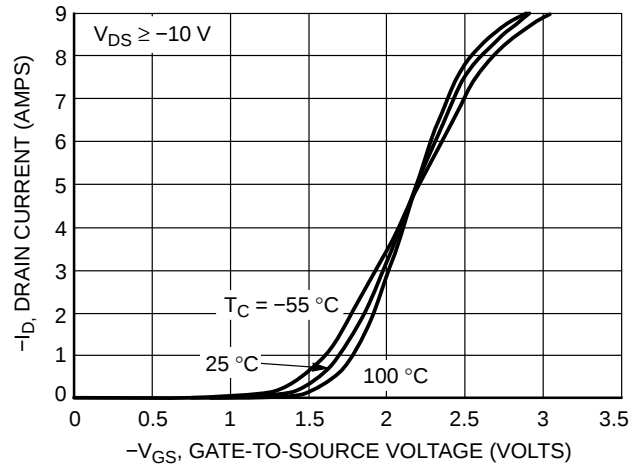


Figure 12. Transfer Characteristics

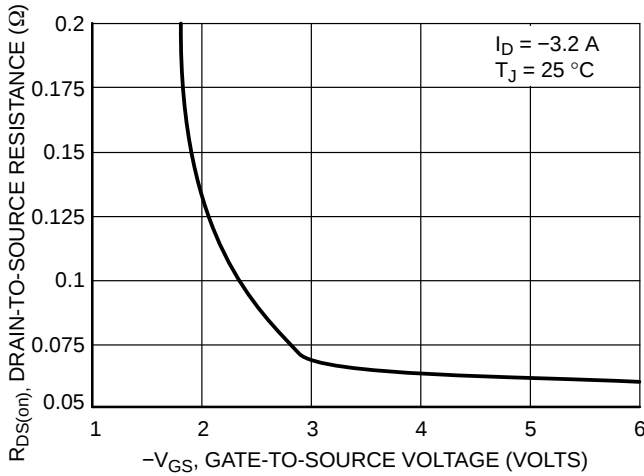


Figure 13. On-Resistance vs. Gate-to-Source Voltage

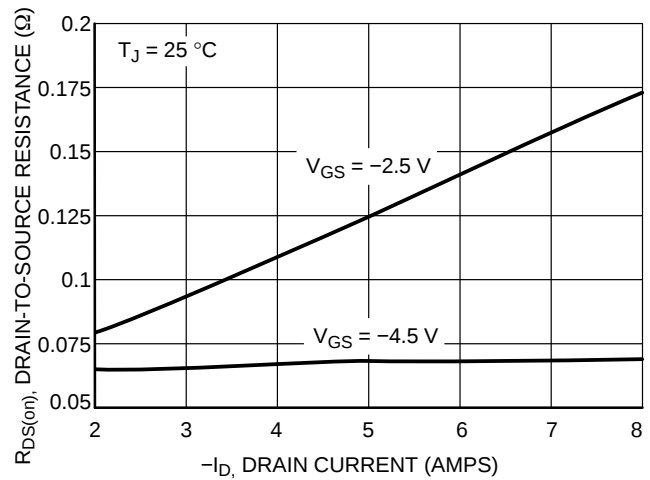


Figure 14. On-Resistance vs. Drain Current and Gate Voltage

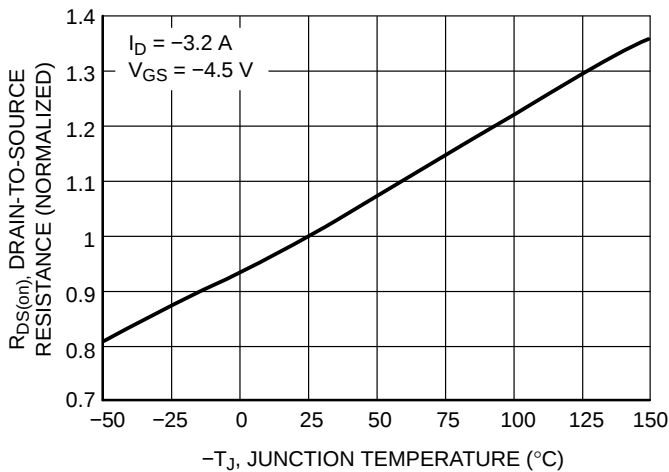


Figure 15. On-Resistance Variation with Temperature

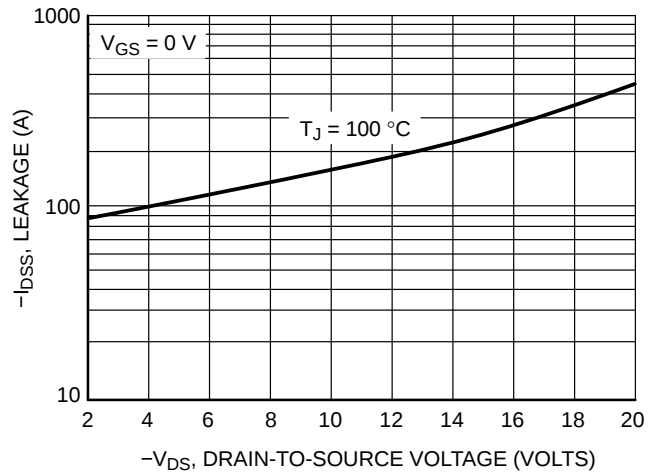


Figure 16. Drain-to-Source Leakage Current vs. Voltage

NTHD3100C

TYPICAL P-CHANNEL PERFORMANCE CURVES

($T_J = 25^\circ\text{C}$ unless otherwise noted)

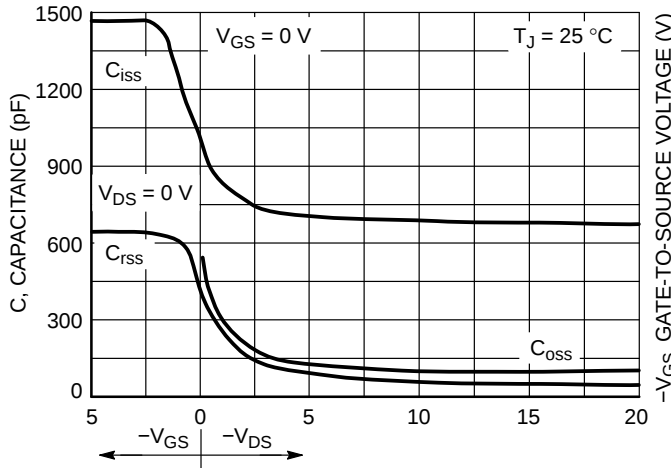


Figure 17. Capacitance Variation

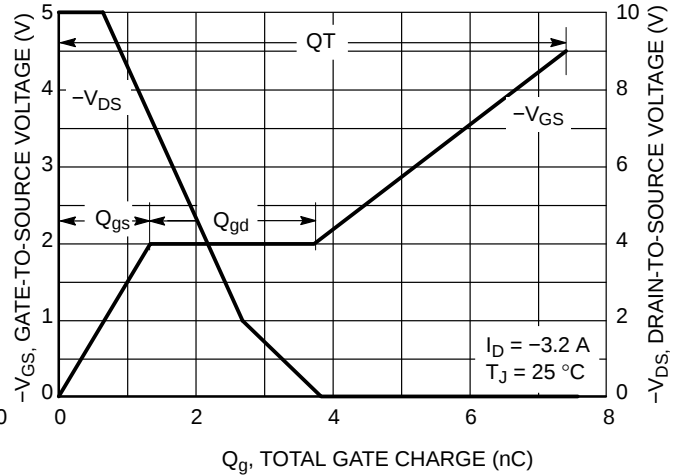


Figure 18. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

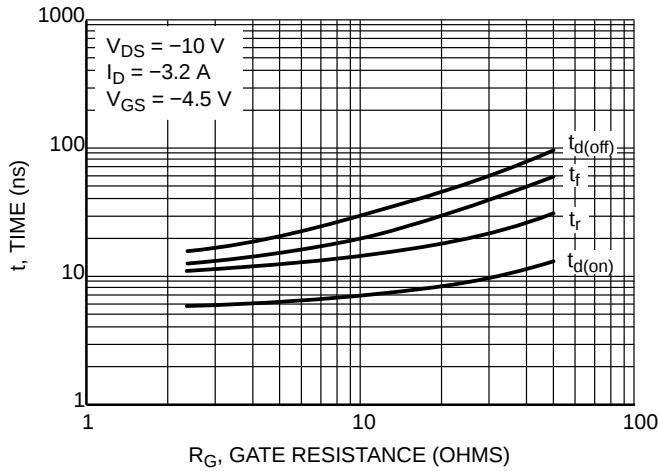


Figure 19. Resistive Switching Time Variation vs. Gate Resistance

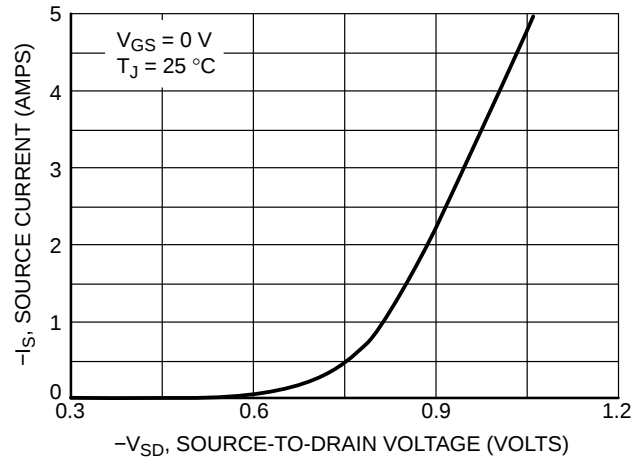


Figure 20. Diode Forward Voltage vs. Current

DEVICE ORDERING INFORMATION

Device	Package	Shipping [†]
NTHD3100CT1G	ChipFET (Pb-Free)	3000 / Tape & Reel

DISCONTINUED (Note 5)

NTHD3100CT1	ChipFET	3000 / Tape & Reel
NTHD3100CT3	ChipFET	10000 / Tape & Reel
NTHD3100CT3G	ChipFET (Pb-Free)	10000 / Tape & Reel

[†] For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

5. **DISCONTINUED:** These devices are not available. Please contact your onsemi representative for information. The most current information on these devices may be available on [www.onsemi.com](#).

ChipFET is a trademark of Vishay Siliconix.

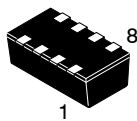
NTHD3100C

REVISION HISTORY

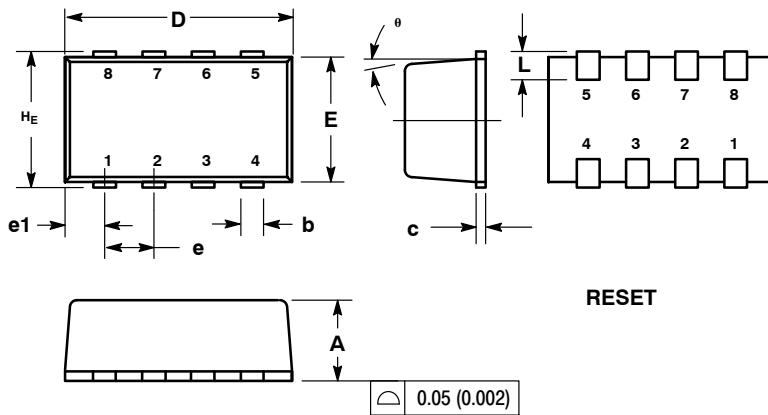
Revision	Description of Changes	Date
4	Rebranded the document to onsemi format. NTHD3100CT1, NTHD3100CT3, NTHD3100CT3G OPNs marked as Discontinued.	2/17/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.





SCALE 1:1



ChipFET™
CASE1206A-03
ISSUE K

DATE 19 MAY 2009

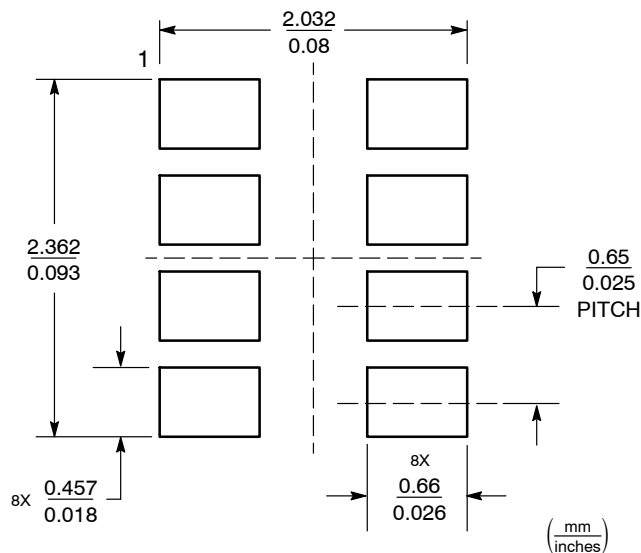
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.05	1.10	0.039	0.041	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.55	1.65	1.70	0.061	0.065	0.067
e	0.65 BSC			0.025 BSC		
e1	0.55 BSC			0.022 BSC		
L	0.28	0.35	0.42	0.011	0.014	0.017
H_E	1.80	1.90	2.00	0.071	0.075	0.079
θ	5° NOM			5° NOM		

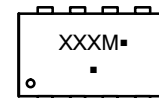
STYLE 1: PIN 1. DRAIN 2. DRAIN 3. DRAIN 4. GATE 5. SOURCE 6. DRAIN 7. DRAIN 8. DRAIN	STYLE 2: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. DRAIN 2 7. DRAIN 1 8. DRAIN 1	STYLE 3: PIN 1. ANODE 2. ANODE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. CATHODE 8. CATHODE	STYLE 4: PIN 1. COLLECTOR 2. COLLECTOR 3. COLLECTOR 4. BASE 5. EMITTER 6. COLLECTOR 7. COLLECTOR 8. COLLECTOR	STYLE 5: PIN 1. ANODE 2. ANODE 3. DRAIN 4. DRAIN 5. SOURCE 6. GATE 7. CATHODE 8. CATHODE	STYLE 6: PIN 1. ANODE 2. DRAIN 3. DRAIN 4. GATE 5. SOURCE 6. DRAIN 7. DRAIN 8. CATHODE / DRAIN
---	---	---	--	---	---

SOLDERING FOOTPRINT



Basic Style

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Month Code
▪ = Pb-Free Package
(Note: Microdot may be in either location)

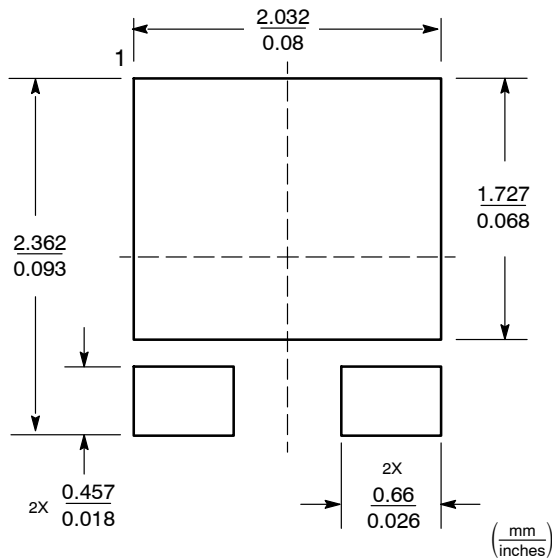
*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

OPTIONAL SOLDERING FOOTPRINTS ON PAGE 2

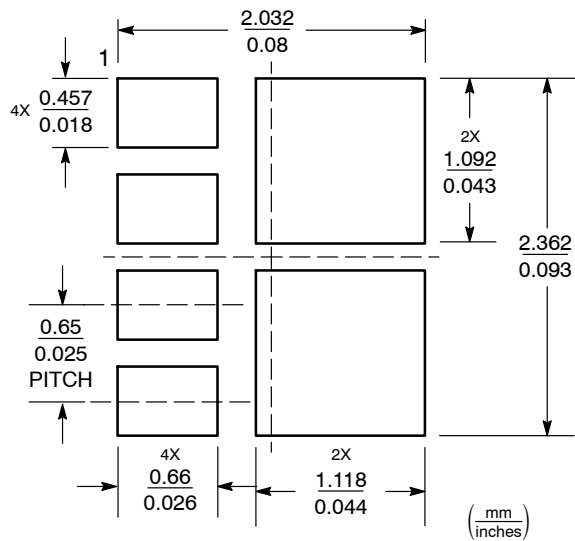
DOCUMENT NUMBER:	98AON03078D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	ChipFET	PAGE 1 OF 2

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

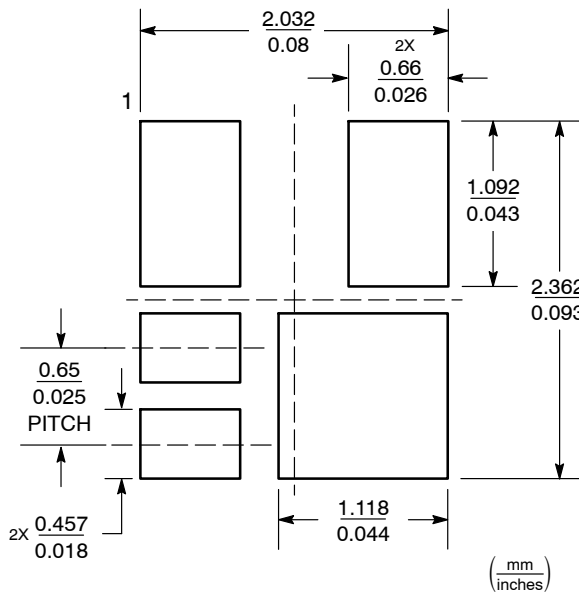
ADDITIONAL SOLDERING FOOTPRINTS*



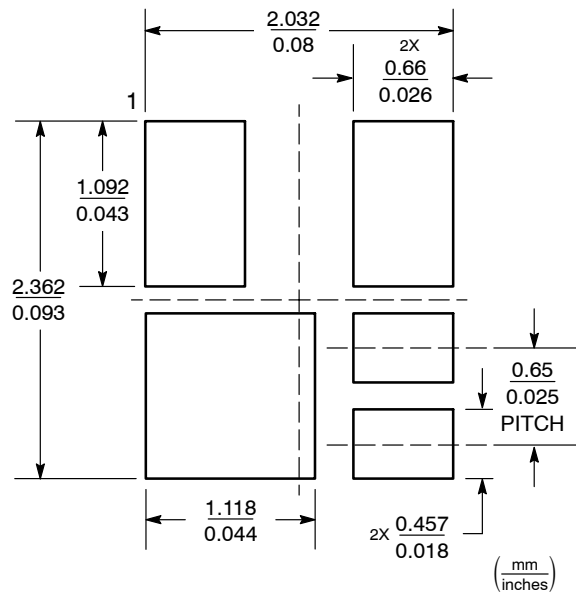
Styles 1 and 4



Style 2



Style 3



Style 5

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON03078D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	ChipFET	PAGE 2 OF 2

onsemi and **onsemi** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales