

Dual, N-Channel, Digital FET

FDC6301N

General Description

These dual N-Channel logic level enhancement mode field effect transistors are produced using onsemi's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. This device has been designed especially for low voltage applications as a replacement for digital transistors. Since bias resistors are not required, these N-Channel FET's can replace several digital transistors, with a variety of bias resistors.

Features

- 25 V, 0.22 A Continuous, 0.5 A Peak
 - $R_{DS(on)} = 5 \Omega @ V_{GS} = 2.7 V$
 - $R_{DS(on)} = 4 \Omega @ V_{GS} = 4.5 V$
- Very Low Level Gate Drive Requirements Allowing Direct Operation in 3 V Circuits. $V_{GS(th)} < 1.5 V$
- Gate-Source Zener for ESD Ruggedness. >6 kV Human Body Model
- This is a Pb-Free and Halide Free Device

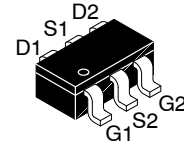
ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter		Ratings	Unit
V _{DSS} , V _{CC}	Drain–Source Voltage, Power Supply Voltage		25	V
V _{GSS} , V _{IN}	Gate–Source Voltage, V _{IN}		–0.5 to + 8	V
I _D , I _{OUT}	Drain / Output Current	– Continuous	0.22	A
		– Pulsed	0.5	
P _D	Maximum Power Dissipation	(Note 1a)	0.9	W
		(Note 1b)	0.7	
T _J , T _{STG}	Operating and Storage Temperature Range		–55 to +150	°C
ESD	Electrostatic Discharge Rating MIL–STD–883D Human Body Model (100 pF / 1500 Ω)		6.0	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

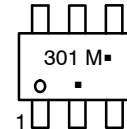
THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
R _{θJA}	Thermal Resistance, Junction-to-Ambient (Note 1a)	140	°C/W
R _{θJC}	Thermal Resistance, Junction-to-Case (Note 1)	60	°C/W



TSOT23 6-Lead
SUPERSOT™-6
CASE 419BL

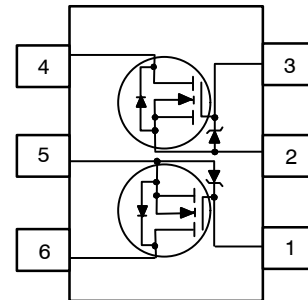
MARKING DIAGRAM



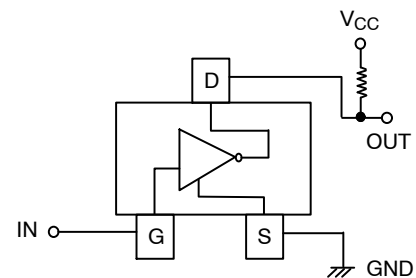
301 = Specific Device Code
M = Assembly Operation Month
▪ = Pb-Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT



INVERTER APPLICATION



ORDERING INFORMATION

Device	Package	Shipping†
FDC6301N	TSOT-23-6 (SUPERSOT™-6) (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](http://www.onsemi.com/BRD8011/D).

FDC6301N

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
BV _{DSS}	Drain–Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	25	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	–	25	–	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 20 V, V _{GS} = 0 V	–	–	1	μA
		V _{DS} = 20 V, V _{GS} = 0 V, T _J = 55°C	–	–	10	μA
I _{GSS}	Gate–Body Leakage Current	V _{GS} = 8 V, V _{DS} = 0 V	–	–	100	nA

ON CHARACTERISTICS (Note 2)

$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	–	–2.1	–	mV/°C
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	0.65	0.85	1.5	V
R _{DS(on)}	Static Drain–Source On–Resistance	V _{GS} = 2.7 V, I _D = 0.2 A V _{GS} = 2.7 V, I _D = 0.2 A, T _J = 125°C V _{GS} = 4.5 V, I _D = 0.4 A	– – –	3.8 6.3 3.1	5 9 4	Ω
I _{D(on)}	On–State Drain Current	V _{GS} = 10 V, V _{DS} = 10 V	0.2	–	–	A
g _{FS}	Forward Transconductance	V _{DS} = 5 V, I _D = 1.0 A	–	0.25	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 10 V, V _{GS} = 0 V, f = 1.0 MHz	–	9.5	–	pF
C _{oss}	Output Capacitance		–	6	–	pF
C _{rss}	Reverse Transfer Capacitance		–	1.3	–	pF

SWITCHING CHARACTERISTICS (Note 2)

t _{D(on)}	Turn–On Delay Time	V _{DD} = 6 V, I _D = 0.5 A, V _{GS} = 4.5 V, R _{GEN} = 50 Ω	–	5	10	ns
t _r	Turn–On Rise Time		–	4.5	10	ns
t _{D(off)}	Turn–Off Delay Time		–	4	8	ns
t _f	Turn–Off Fall Time		–	3.2	7	ns
Q _g	Total Gate Charge	V _{DS} = 5 V, I _D = 0.2 A, V _{GS} = 4.5 V	–	0.49	0.7	nC
Q _{gs}	Gate–Source Charge		–	0.22	–	nC
Q _{gd}	Gate–Drain Charge		–	0.07	–	nC

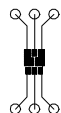
INVERTER ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I _{O(off)}	Zero Input Voltage Output Current	V _{CC} = 20 V, V _I = 0 V	–	–	1	μA
V _{I(off)}	Input Voltage	V _{CC} = 5 V, I _O = 10 μA	–	–	0.5	V
V _{I(on)}		V _O = 0.3 V, I _O = 0.005 A	1	–	–	V
R _{O(on)}	Output to Ground Resistance	V _I = 2.7 V, I _O = 0.2 A	–	3.8	5	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

- R_{θJA} is the sum of the junction–to–case and case–to–ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design. R_{θJA} shown below for single device operation on FR–4 in still air.



a. 140°C/W on a 0.125 in² pad of 2 oz. copper.



b. 180°C/W on a 0.005 in² pad of 2 oz. copper.

- Pulse Test: Pulse Width ≤ 300 μs, Duty cycle ≤ 2.0 %.

TYPICAL CHARACTERISTICS

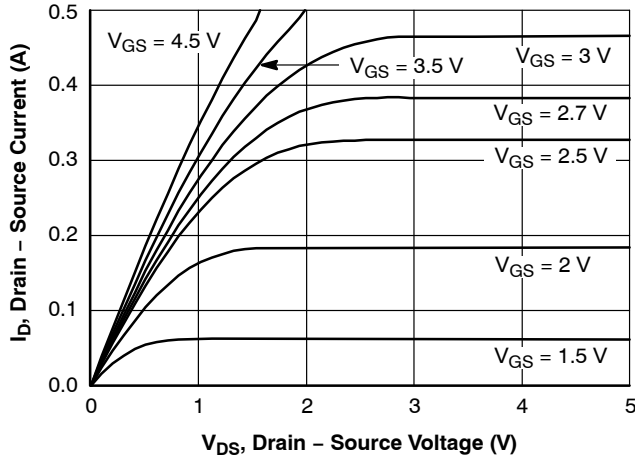


Figure 1. On Region Characteristics

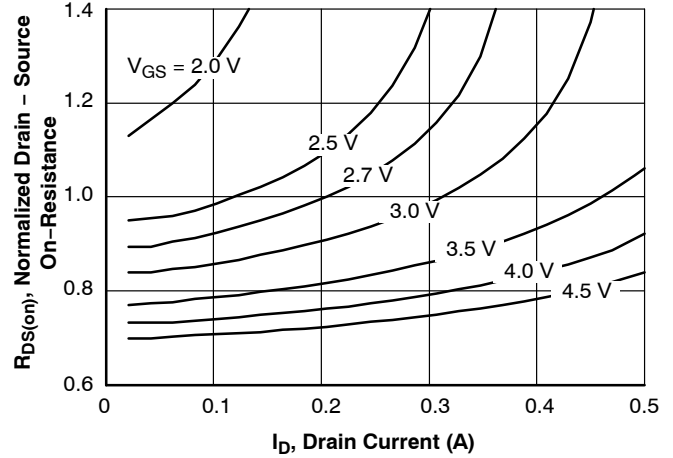


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

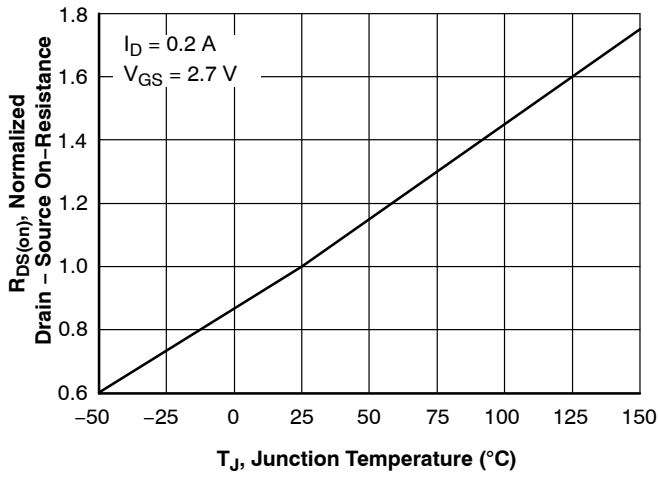


Figure 3. On Resistance Variation with Temperature

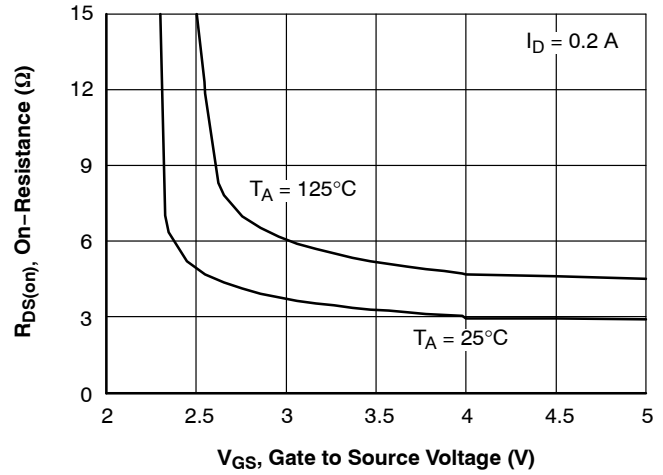


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

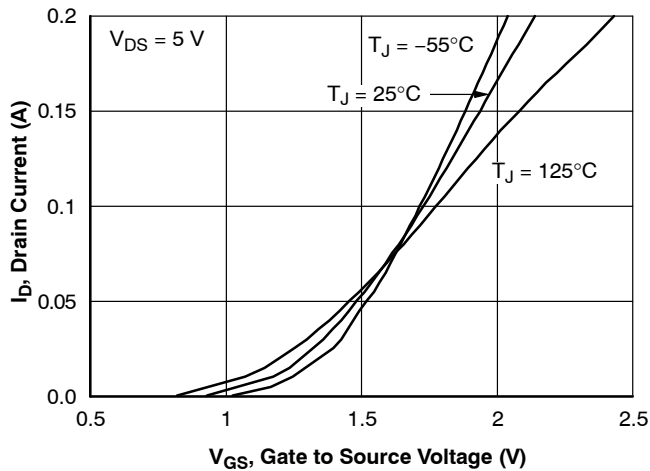


Figure 5. Transfer Characteristics

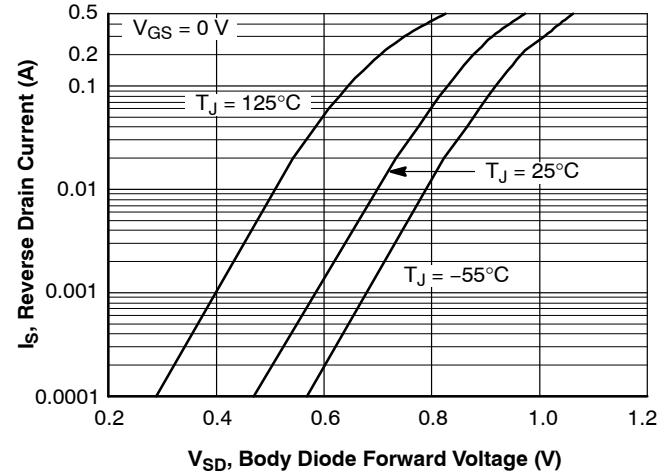


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS (continued)

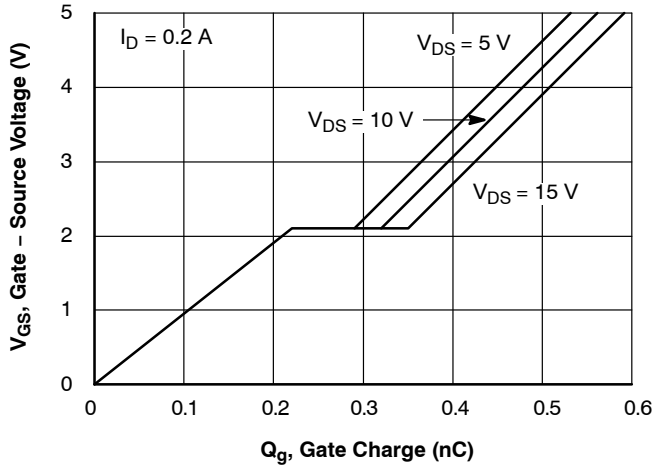


Figure 7. Gate Charge Characteristics

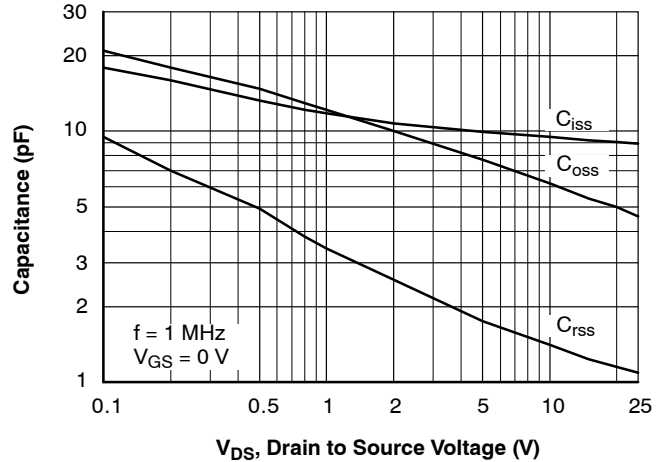


Figure 8. Capacitance Characteristics

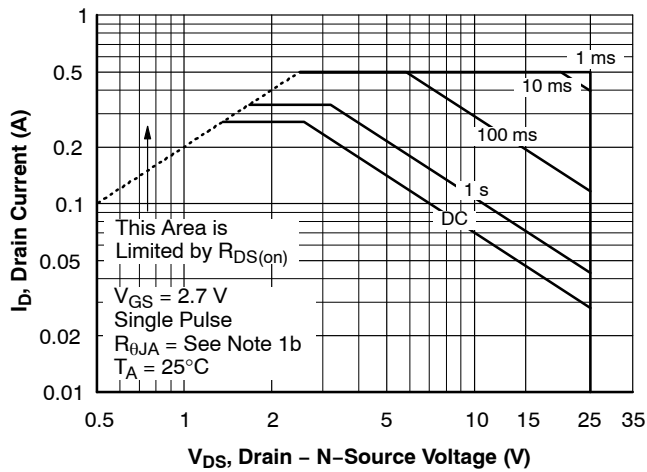


Figure 10. Maximum Safe Operating Area

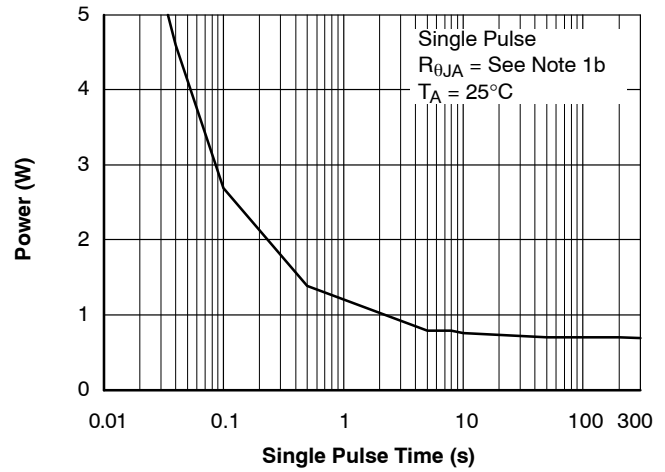


Figure 9. Single Pulse Maximum Power Dissipation

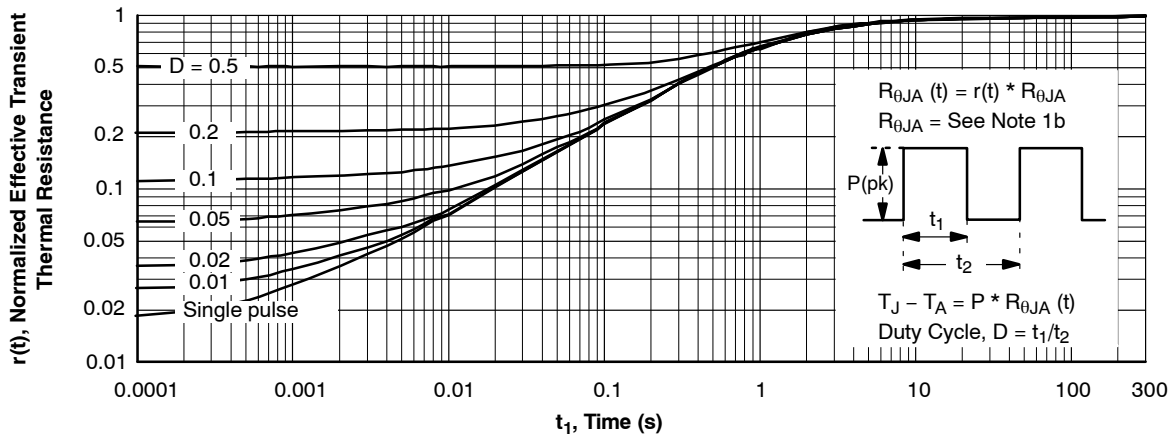


Figure 11. Transient Thermal Response Curve

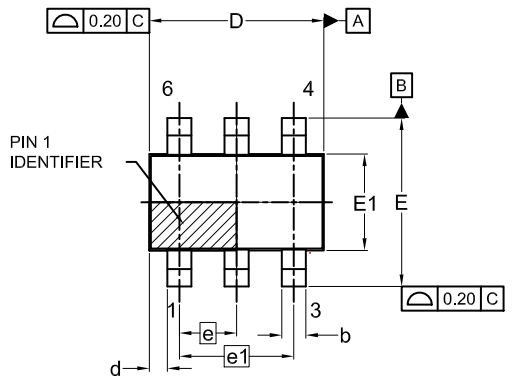
Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.



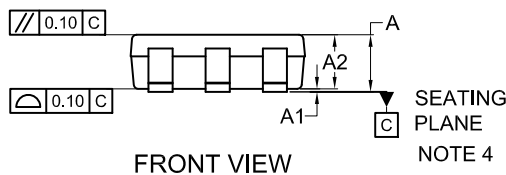
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SCALE 2:1

TSOT23 6-Lead
CASE 419BL
ISSUE A

DATE 31 AUG 2020



TOP VIEW



FRONT VIEW



DETAIL A



SIDE VIEW

SYMM
⌀



LAND PATTERN
RECOMMENDATION

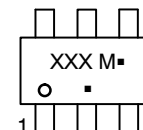
*FOR ADDITIONAL INFORMATION ON OUR
 PB-FREE STRATEGY AND SOLDERING DETAILS,
 PLEASE DOWNLOAD THE ON SEMICONDUCTOR
 SOLDERING AND MOUNTING TECHNIQUES
 REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25MM PER END. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	0.05	0.10
A2	0.70	0.85	1.00
A3	0.25 BSC		
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.80	2.95	3.10
d	0.30 REF		
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.95 BSC		
e1	1.90 BSC		
L1	0.60 REF		
L2	0.20	0.40	0.60
⌀	0°	---	10°

GENERIC
MARKING DIAGRAM*



XXX = Specific Device Code

M = Date Code

▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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