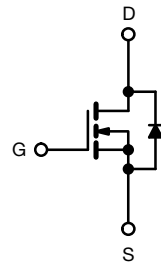
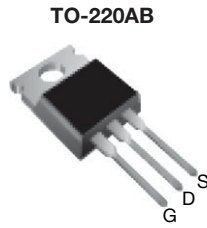


Power MOSFET



N-Channel MOSFET

FEATURES

- Dynamic dV/dt rating
- 175 °C operating temperature
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

PRODUCT SUMMARY	
V_{DS} (V)	60
$R_{DS(on)}$ (Ω)	$V_{GS} = 10$ V 0.028
Q_g (Max.) (nC)	67
Q_{gs} (nC)	18
Q_{gd} (nC)	25
Configuration	Single

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRFZ44PbF
Lead (Pb)-free and halogen-free	IRFZ44PbF-BE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	60	V
Gate-source voltage		V_{GS}	± 20	
Continuous drain current	V_{GS} at 10 V	I_D	$T_C = 25$ °C	50
			$T_C = 100$ °C	36
Pulsed drain current ^a		I_{DM}	200	A
Linear derating factor			1.0	
Single pulse avalanche energy ^b		E_{AS}	100	mJ
Maximum power dissipation		P_D	150	W
Peak diode recovery dV/dt ^c		dV/dt	4.5	V/ns
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) ^d			300	
Mounting torque	6-32 or M3 screw		10	lbf · in
			1.1	N · m

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- $V_{DD} = 25$ V, starting $T_J = 25$ °C, $L = 44$ μ H, $R_g = 25$ Ω , $I_{AS} = 51$ A (see fig. 12)
- $I_{SD} \leq 51$ A, $dI/dt \leq 250$ A/ μ s, $V_{DD} \leq V_{DS}$, $T_J \leq 175$ °C
- 1.6 mm from case
- Current limited by the package, (die current = 51 A)

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	62	°C/W
Case-to-sink, flat, greased surface	R_{thCS}	0.50	-	
Maximum junction-to-case (drain)	R_{thJC}	-	1.0	

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		60	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$		-	0.060	-	V/°C
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	V
Gate-source leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$		-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$		-	-	25	μA
		$V_{DS} = 48\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	250	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 31\text{ A}^b$	-	-	0.028	Ω
Forward transconductance	g_{fs}	$V_{DS} = 25\text{ V}, I_D = 31\text{ A}$		15	-	-	S
Dynamic							
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V},$ $V_{DS} = 25\text{ V},$ $f = 1.0\text{ MHz}$, see fig. 5		-	1900	-	pF
Output capacitance	C_{oss}			-	920	-	
Reverse transfer capacitance	C_{rss}			-	170	-	
Total gate charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 51\text{ A}, V_{DS} = 48\text{ V},$ see fig. 6 and 13 ^b	-	-	67	nC
Gate-source charge	Q_{gs}			-	-	18	
Gate-drain charge	Q_{gd}			-	-	25	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 30\text{ V}, I_D = 51\text{ A},$ $R_g = 9.1\text{ }\Omega, R_D = 0.55\text{ }\Omega$, see fig. 10 ^b		-	14	-	ns
Rise time	t_r			-	110	-	
Turn-off delay time	$t_{d(off)}$			-	45	-	
Fall time	t_f			-	92	-	
Internal drain inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.5	-	nH
Internal source inductance	L_S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	50	A
Pulsed diode forward current ^a	I_{SM}			-	-	200	
Body diode voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 51\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	2.5	V
Body diode reverse recovery time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = 51\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		-	120	180	ns
Body diode reverse recovery charge	Q_{rr}			-	0.53	0.80	nC
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
 b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

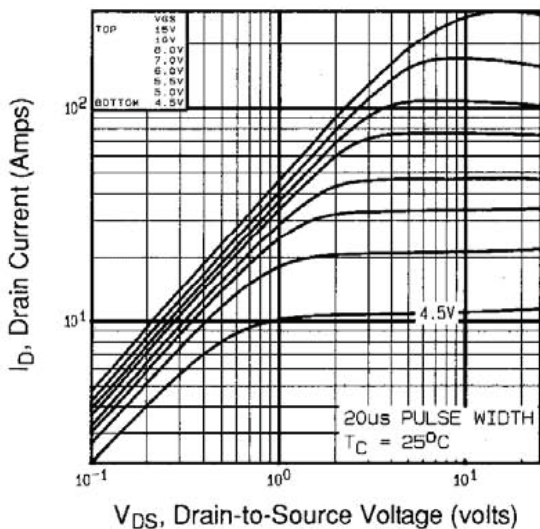


Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^\circ\text{C}$

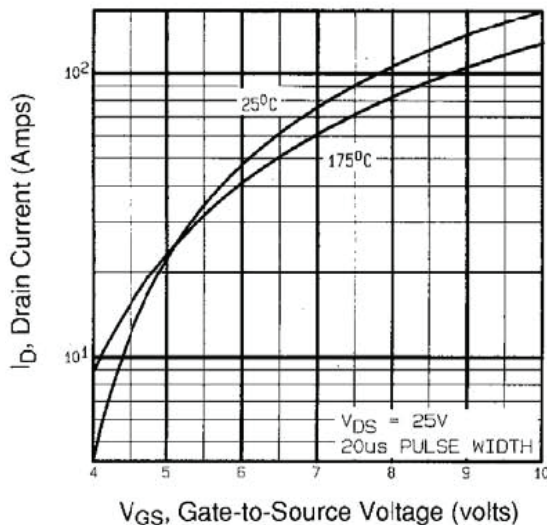


Fig. 3 - Typical Transfer Characteristics

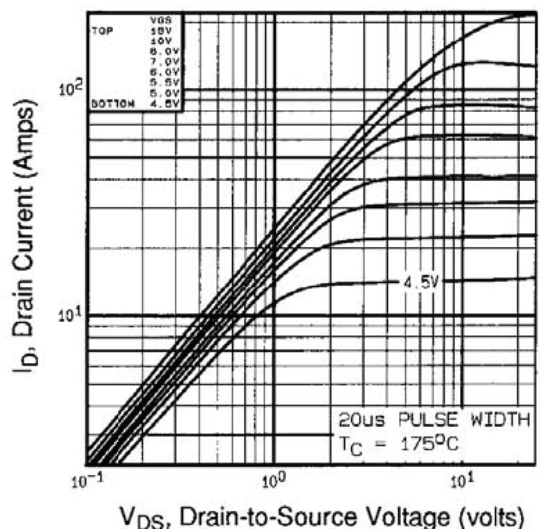


Fig. 2 - Typical Output Characteristics, $T_C = 175\text{ }^\circ\text{C}$

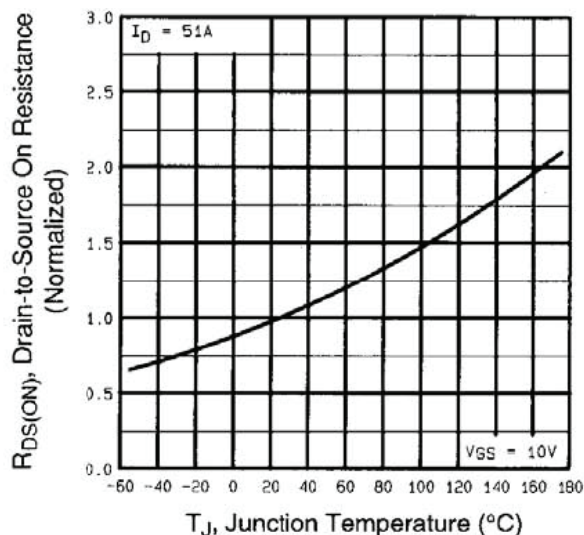


Fig. 4 - Normalized On-Resistance vs. Temperature

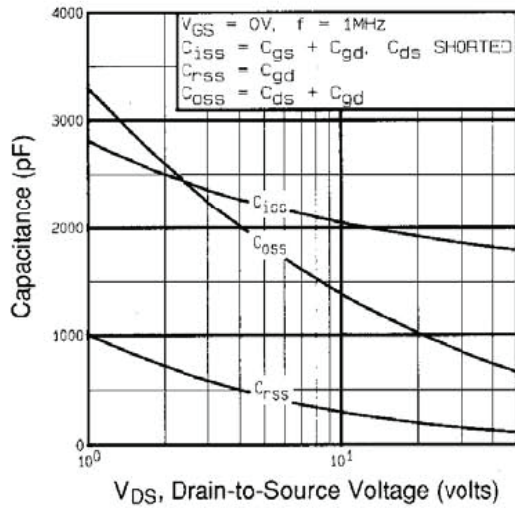


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

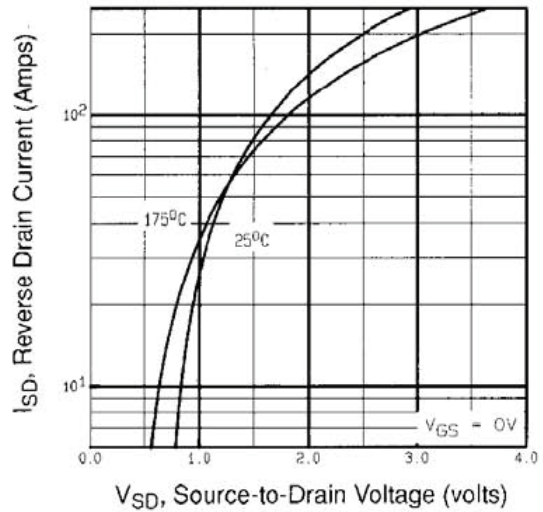


Fig. 7 - Typical Source-Drain Diode Forward Voltage

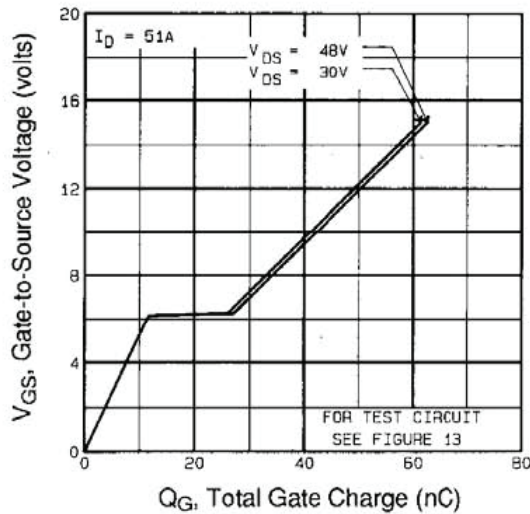


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

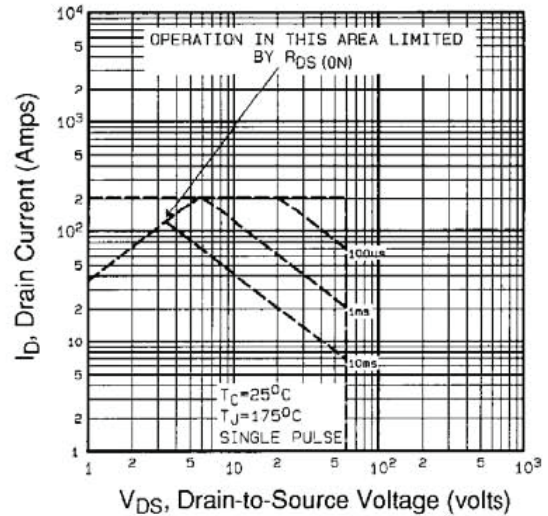


Fig. 8 - Maximum Safe Operating Area

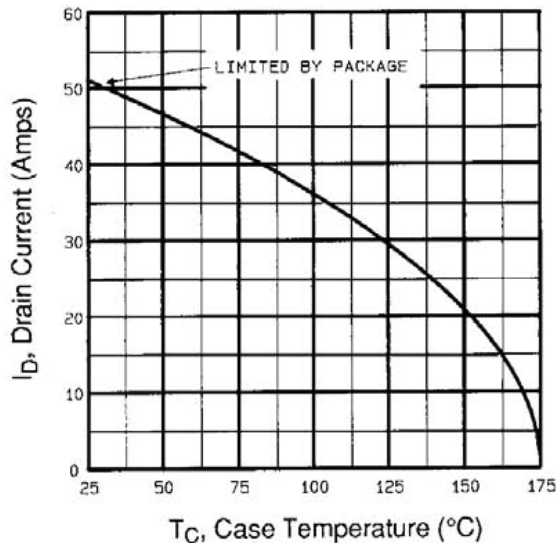


Fig. 9 - Maximum Drain Current vs. Case Temperature

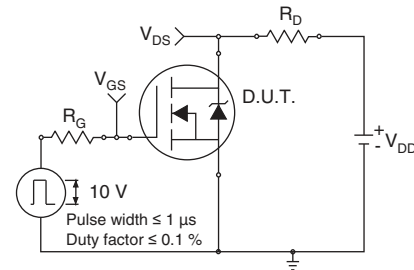


Fig. 10a - Switching Time Test Circuit

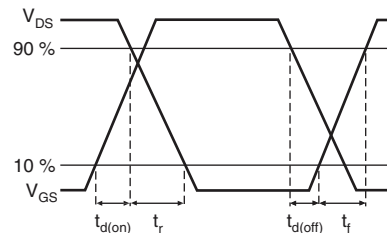


Fig. 10b - Switching Time Waveforms

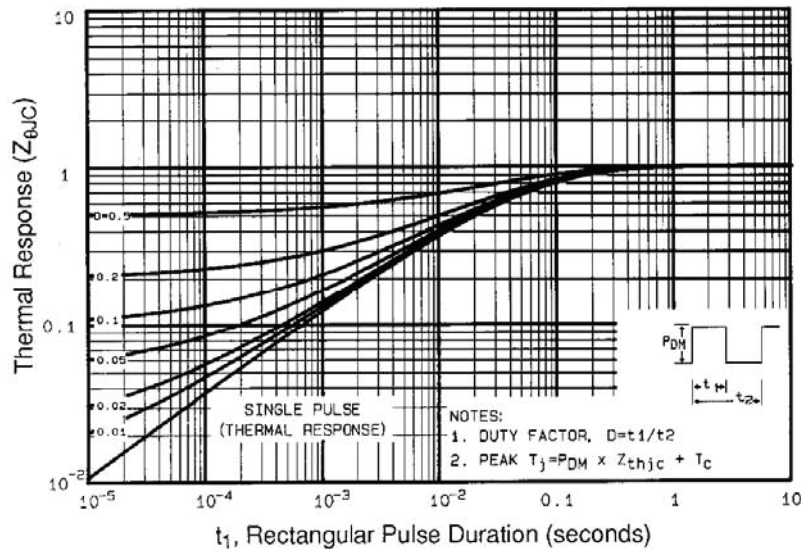


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

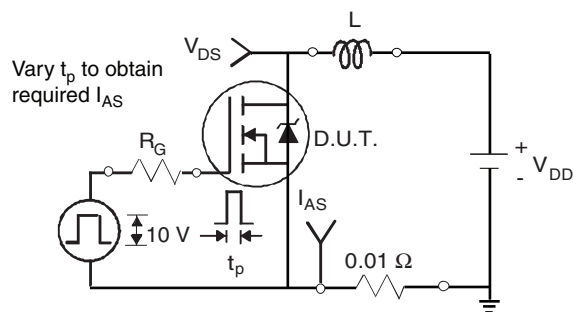


Fig. 12a - Unclamped Inductive Test Circuit

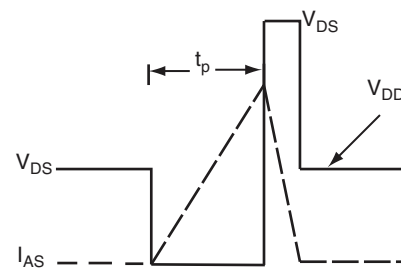


Fig. 12b - Unclamped Inductive Waveforms

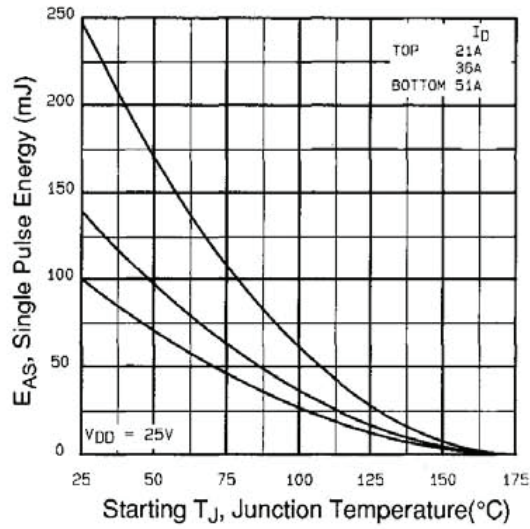


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

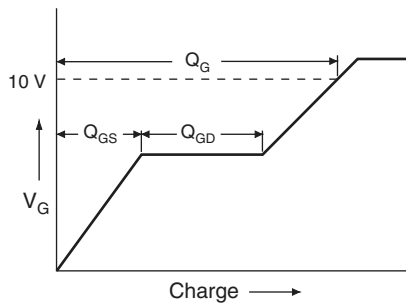


Fig. 13a - Basic Gate Charge Waveform

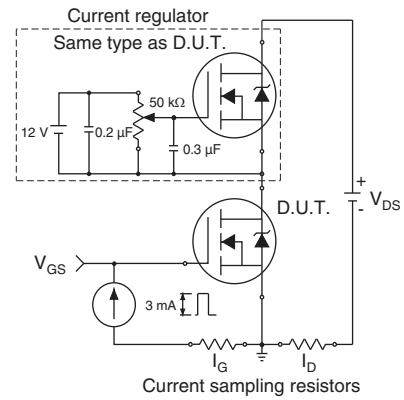
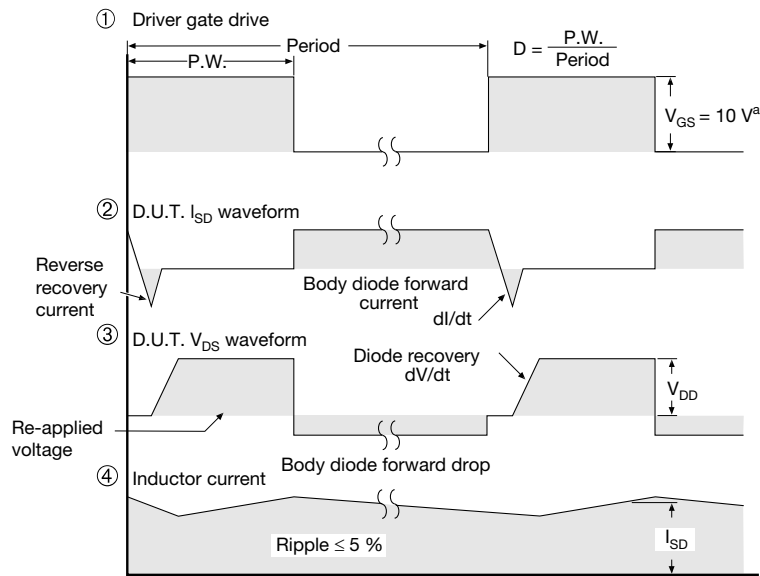
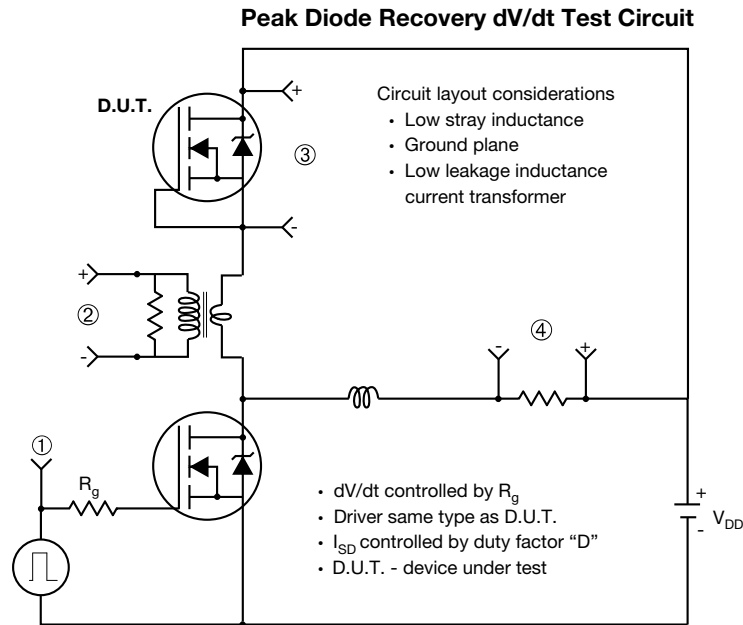


Fig. 13b - Gate Charge Test



Note

a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel

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