

# 74LVC1G79-Q100

Single D-type flip-flop; positive-edge trigger

Rev. 5 — 9 September 2025

Product data sheet

## 1. General description

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The 74LVC1G79-Q100 is a single positive-edge triggered D-type flip-flop. Data at the D-input that meets the set-up and hold time requirements on the LOW-to-HIGH clock transition will be stored in the flip-flop and appear at the Q output. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial power down applications using I<sub>OFF</sub>. The I<sub>OFF</sub> circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

## 2. Features and benefits

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- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and -40 °C to +125 °C
- Wide supply voltage range from 1.65 V to 5.5 V
- Overvoltage tolerant inputs to 5.5 V
- High noise immunity
- CMOS low power dissipation
- ±24 mA output drive (V<sub>CC</sub> = 3.0 V)
- Direct interface with TTL levels
- Latch-up performance exceeds 250 mA
- I<sub>OFF</sub> circuitry provides partial Power-down mode operation
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8C (2.7 V to 3.6 V)
  - JESD36 (4.5 V to 5.5 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
<a href="#">74LVC1G79GW-Q100</a>	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	<a href="#">SOT353-1</a>
<a href="#">74LVC1G79GV-Q100</a>	-40 °C to +125 °C	SC-74A	plastic surface-mounted package; 5 leads	<a href="#">SOT753</a>
<a href="#">74LVC1G79GZ-Q100</a>	-40 °C to +125 °C	XSON5	plastic thermal enhanced extremely thin small outline package with side-wettable flanks (SWF); no leads; 5 terminals; body 1.1 × 0.85 × 0.5 mm	<a href="#">SOT8065-1</a>

### 4. Marking

Table 2. Marking codes

Type number	Marking[1]
74LVC1G79GW-Q100	VP
74LVC1G79GV-Q100	V79
74LVC1G79GZ-Q100	VP

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

### 5. Functional diagram

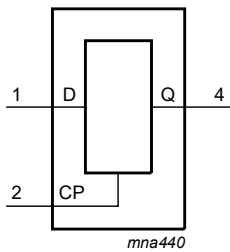


Fig. 1. Logic symbol

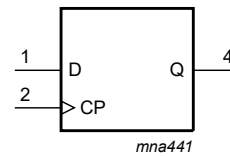


Fig. 2. IEC logic symbol

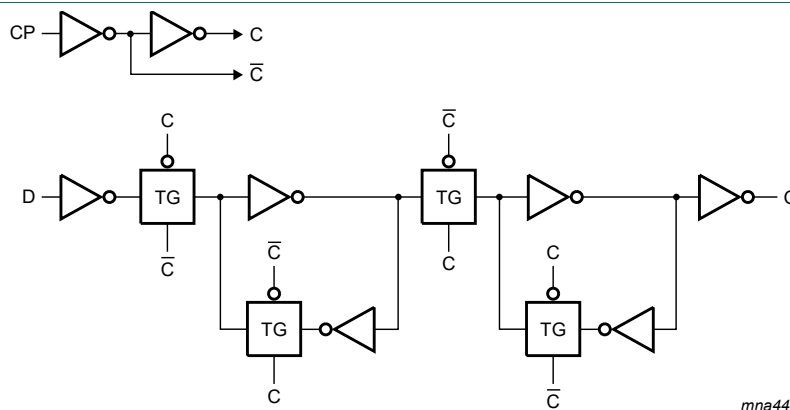
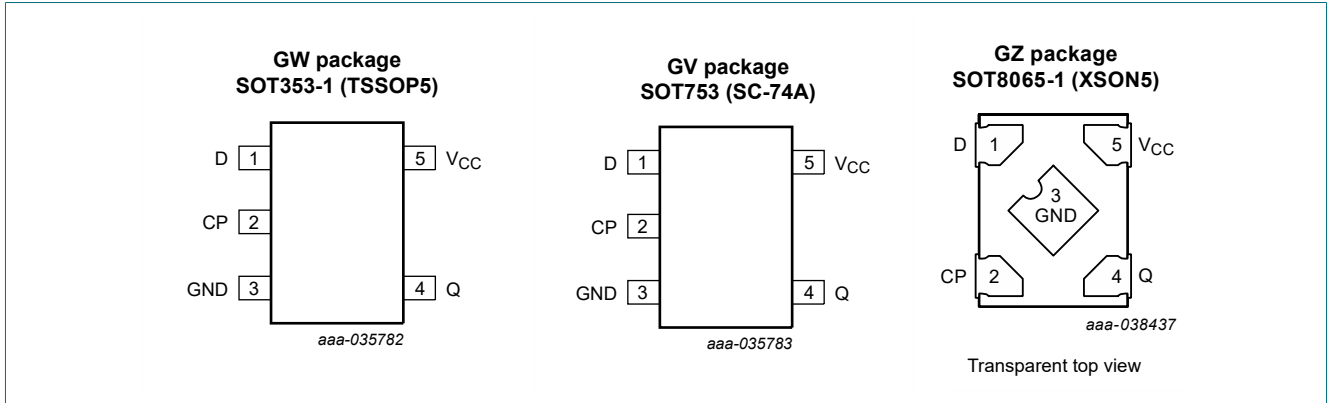


Fig. 3. Logic diagram

## 6. Pinning information

### 6.1. Pinning



### 6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
D	1	data input
CP	2	clock pulse input
GND	3	ground (0 V)
Q	4	data output
V <sub>CC</sub>	5	supply voltage

## 7. Functional description

Table 4. Function table

*H = HIGH voltage level; L = LOW voltage level; ↑ = LOW-to-HIGH CP transition; X = don't care; q = lower case letter indicates the state of referenced input, one set-up time prior to the LOW-to-HIGH CP transition.*

Input		Output
CP	D	Q
↑	L	L
↑	H	H
L	X	q

## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+6.5	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$V_I$	input voltage		-0.5	+6.5	V
$I_{OK}$	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	$\pm 50$	mA
$V_O$	output voltage	Active mode	-0.5	$V_{CC} + 0.5$	V
		Power-down mode; $V_{CC} = 0$ V	-0.5	+6.5	V
$I_O$	output current	$V_O = 0$ V to $V_{CC}$	-	$\pm 50$	mA
$I_{CC}$	supply current		-	100	mA
$I_{GND}$	ground current		-100	-	mA
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to $+125$ °C	-	250	mW
$T_{stg}$	storage temperature		-65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT353-1 (TSSOP5) package:  $P_{tot}$  derates linearly with 3.3 mW/K above 74 °C.

For SOT753 (SC-74A) package:  $P_{tot}$  derates linearly with 3.8 mW/K above 85 °C.

For SOT8065-1 (XSON5) package:  $P_{tot}$  derates linearly with 3.2 mW/K above 72 °C.

## 9. Recommended operating conditions

**Table 6. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		1.65	-	5.5	V
$V_I$	input voltage		0	-	5.5	V
$V_O$	output voltage	Active mode	0	-	$V_{CC}$	V
		Power-down mode; $V_{CC} = 0$ V	0	-	5.5	V
$T_{amb}$	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65$ V to $2.7$ V	-	-	20	ns/V
		$V_{CC} = 2.7$ V to $5.5$ V	-	-	10	ns/V

## 10. Static characteristics

**Table 7. Static characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
<b>T<sub>amb</sub> = -40 °C to +85 °C</b>						
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>	-	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	-	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	V
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7 × V <sub>CC</sub>	-	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	-	-	0.35 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	V
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.3 × V <sub>CC</sub>	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 1.65 V to 5.5 V	V <sub>CC</sub> - 0.1	-	-	V
		I <sub>O</sub> = -4 mA; V <sub>CC</sub> = 1.65 V	1.2	-	-	V
		I <sub>O</sub> = -8 mA; V <sub>CC</sub> = 2.3 V	1.9	-	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V	2.2	-	-	V
		I <sub>O</sub> = -24 mA; V <sub>CC</sub> = 3.0 V	2.3	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.65 V to 5.5 V	-	-	0.1	V
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 1.65 V	-	-	0.45	V
		I <sub>O</sub> = 8 mA; V <sub>CC</sub> = 2.3 V	-	-	0.3	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	-	0.4	V
		I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	-	0.55	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	±0.1	±1	μA
		V <sub>CC</sub> = 0 V; V <sub>I</sub> or V <sub>O</sub> = 5.5 V	-	±0.1	±2	μA
I <sub>OFF</sub>	power-off leakage current	V <sub>CC</sub> = 0 V; V <sub>I</sub> or V <sub>O</sub> = 5.5 V	-	±0.1	±2	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 1.65 V to 5.5 V; I <sub>O</sub> = 0 A	-	0.1	4	μA
ΔI <sub>CC</sub>	additional supply current	per pin; V <sub>CC</sub> = 2.3 V to 5.5 V; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A	-	5	500	μA
C <sub>I</sub>	input capacitance	V <sub>CC</sub> = 3.3 V; V <sub>I</sub> = GND to V <sub>CC</sub>	-	5	-	pF

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
<b>T<sub>amb</sub> = -40 °C to +125 °C</b>						
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>	-	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	-	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	-	-	V
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7 × V <sub>CC</sub>	-	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	-	-	0.35 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	-	0.8	V
		V <sub>CC</sub> = 4.5 V to 5.5 V	-	-	0.3 × V <sub>CC</sub>	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 1.65 V to 5.5 V	V <sub>CC</sub> - 0.1	-	-	V
		I <sub>O</sub> = -4 mA; V <sub>CC</sub> = 1.65 V	0.95	-	-	V
		I <sub>O</sub> = -8 mA; V <sub>CC</sub> = 2.3 V	1.7	-	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V	1.9	-	-	V
		I <sub>O</sub> = -24 mA; V <sub>CC</sub> = 3.0 V	2.0	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.65 V to 5.5 V	-	-	0.1	V
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 1.65 V	-	-	0.70	V
		I <sub>O</sub> = 8 mA; V <sub>CC</sub> = 2.3 V	-	-	0.45	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	-	0.60	V
		I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	-	0.80	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	±1	μA
		V <sub>CC</sub> = 0 V; V <sub>I</sub> or V <sub>O</sub> = 5.5 V	-	-	±2	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = 5.5 V or GND; V <sub>CC</sub> = 1.65 V to 5.5 V; I <sub>O</sub> = 0 A	-	-	4	μA
ΔI <sub>CC</sub>	additional supply current	per pin; V <sub>CC</sub> = 2.3 V to 5.5 V; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A	-	-	500	μA

[1] All typical values are measured at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.

## 11. Dynamic characteristics

**Table 8. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 6.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t <sub>pd</sub>	propagation delay	CP to Q; see Fig. 4 [2]						
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.0	3.6	9.9	1.0	12.5	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.5	2.3	7.0	0.5	9.0	ns
		V <sub>CC</sub> = 2.7 V	0.5	2.6	6.0	0.5	8.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	0.5	2.2	5.0	0.5	6.5	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.5	1.7	3.8	0.5	5.0	ns
t <sub>su</sub>	set-up time	D to CP; see Fig. 5						
		V <sub>CC</sub> = 1.65 V to 1.95 V	2.5	1.4	-	2.5	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	0.9	-	1.7	-	ns
		V <sub>CC</sub> = 2.7 V	1.7	0.9	-	1.7	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.3	0.6	-	1.2	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	1.2	0.6	-	1.2	-	ns
t <sub>h</sub>	hold time	D to CP; see Fig. 5						
		V <sub>CC</sub> = 1.65 V to 1.95 V	0	-0.7	-	0	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	0	-0.4	-	0	-	ns
		V <sub>CC</sub> = 2.7 V	+0.5	-0.3	-	0.5	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	+0.5	-0.3	-	0.5	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	+0.5	-0.2	-	0.5	-	ns
t <sub>w</sub>	pulse width	CP HIGH or LOW; see Fig. 5						
		V <sub>CC</sub> = 1.65 V to 1.95 V	3.0	1.1	-	3.0	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	2.5	0.7	-	2.5	-	ns
		V <sub>CC</sub> = 2.7 V	2.5	0.6	-	2.5	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	2.5	0.6	-	2.5	-	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	0.5	-	2.0	-	ns
f <sub>max</sub>	maximum frequency	CP; see Fig. 5						
		V <sub>CC</sub> = 1.65 V to 1.95 V	160	250	-	160	-	MHz
		V <sub>CC</sub> = 2.3 V to 2.7 V	160	300	-	160	-	MHz
		V <sub>CC</sub> = 2.7 V	160	350	-	160	-	MHz
		V <sub>CC</sub> = 3.0 V to 3.6 V	160	450	-	160	-	MHz
		V <sub>CC</sub> = 4.5 V to 5.5 V	200	500	-	200	-	MHz
C <sub>PD</sub>	power dissipation capacitance	V <sub>I</sub> = GND to V <sub>CC</sub> ; V <sub>CC</sub> = 3.3 V [3]	-	17	-	-	-	pF

[1] Typical values are measured at T<sub>amb</sub> = 25 °C and V<sub>CC</sub> = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.

[2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.

[3] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz; f<sub>o</sub> = output frequency in MHz; C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V; N = number of inputs switching;  $\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

11.1. Waveforms and test circuit

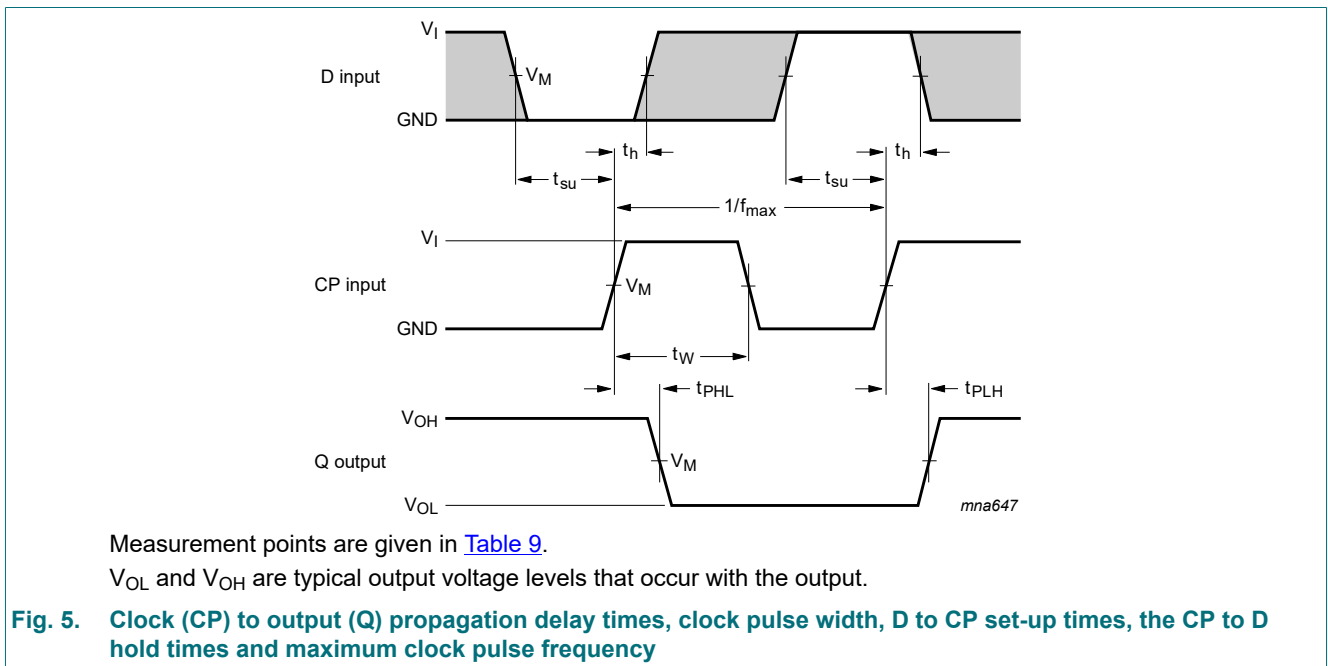
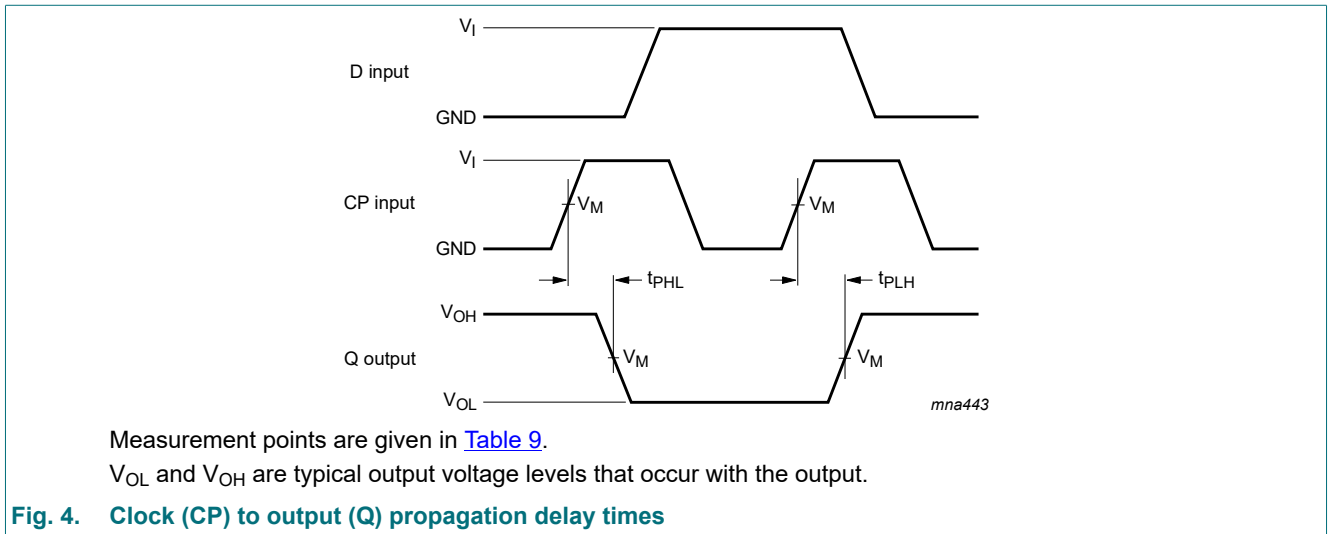
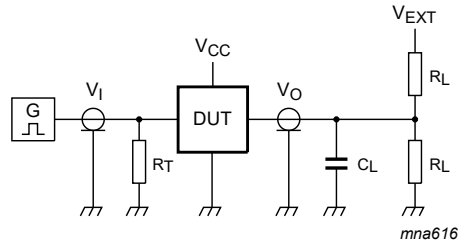


Table 9. Measurement points

Supply voltage	Input	Output
$V_{CC}$	$V_M$	$V_M$
1.65 V to 1.95 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.3 V to 2.7 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$



Test data is given in [Table 10](#).

Definitions for test circuit:

$R_L$  = Load resistance;

$C_L$  = Load capacitance including jig and probe capacitance;

$R_T$  = Termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator;

$V_{EXT}$  = External voltage for measuring switching times.

**Fig. 6. Test circuit for measuring switching times**

**Table 10. Test data**

Supply voltage	Input		Load		$V_{EXT}$
$V_{CC}$	$V_I$	$t_r = t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$
1.65 V to 1.95 V	$V_{CC}$	$\leq 2.0$ ns	30 pF	1 k $\Omega$	open
2.3 V to 2.7 V	$V_{CC}$	$\leq 2.0$ ns	30 pF	500 $\Omega$	open
2.7 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open
3.0 V to 3.6 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open
4.5 V to 5.5 V	$V_{CC}$	$\leq 2.5$ ns	50 pF	500 $\Omega$	open

## 12. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm

SOT353-1

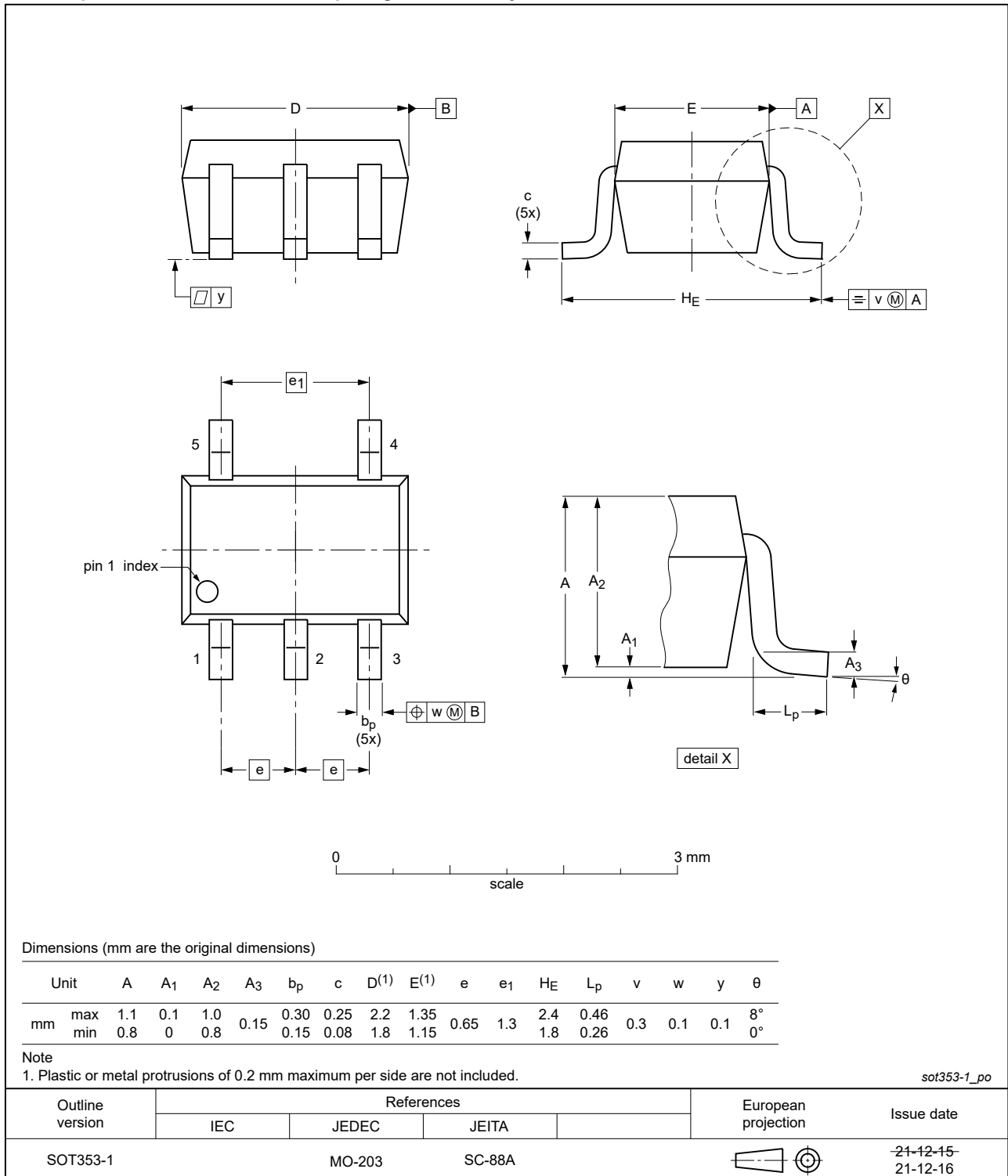


Fig. 7. Package outline SOT353-1 (TSSOP5)

Plastic surface-mounted package; 5 leads

SOT753

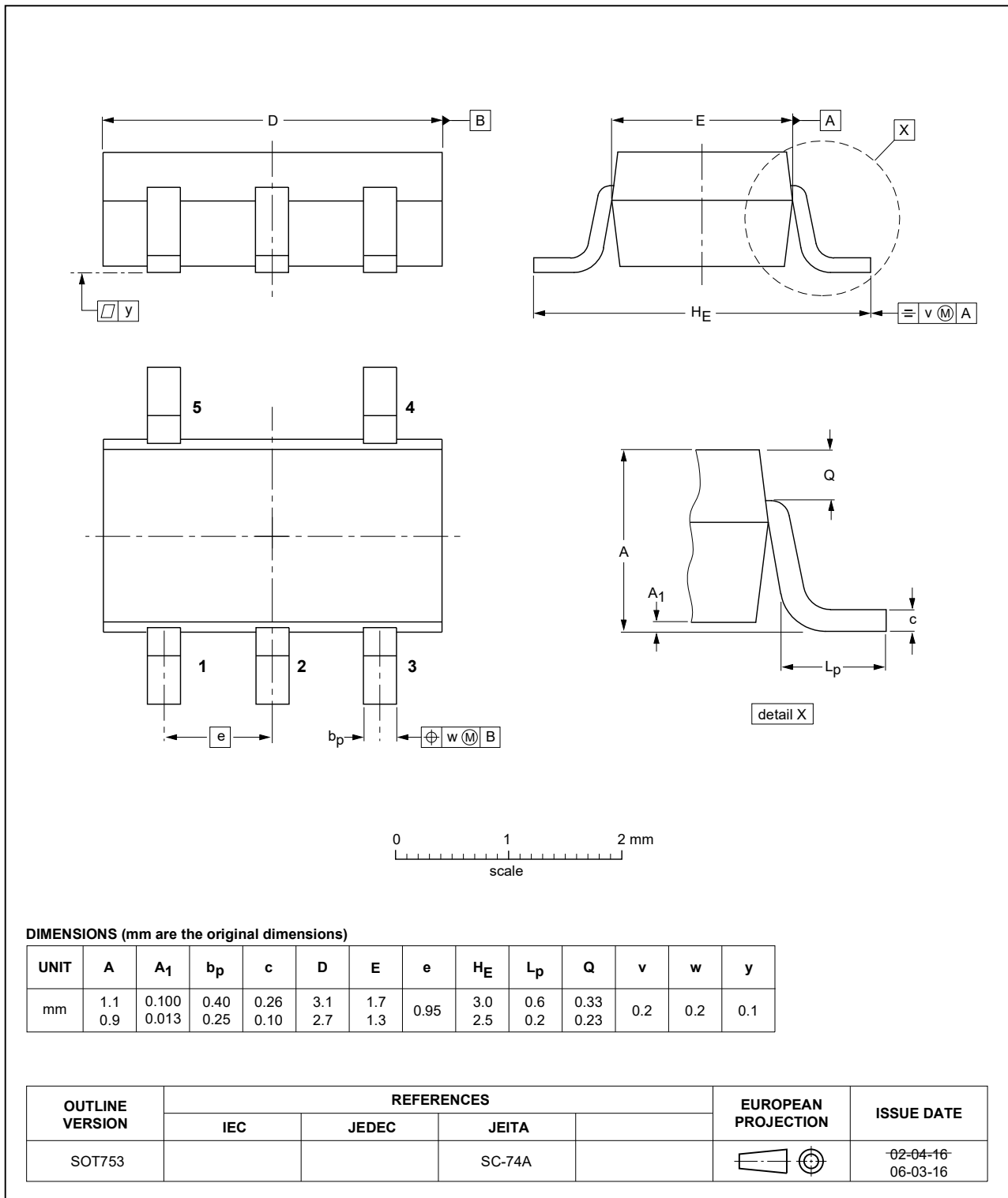


Fig. 8. Package outline SOT753 (SC-74A)

**XSON5:** Plastic thermal enhanced extremely thin small outline package with side-wettable flanks (SWF); no leads; 5 terminals; body 1.1 × 0.85 × 0.5 mm

SOT8065-1

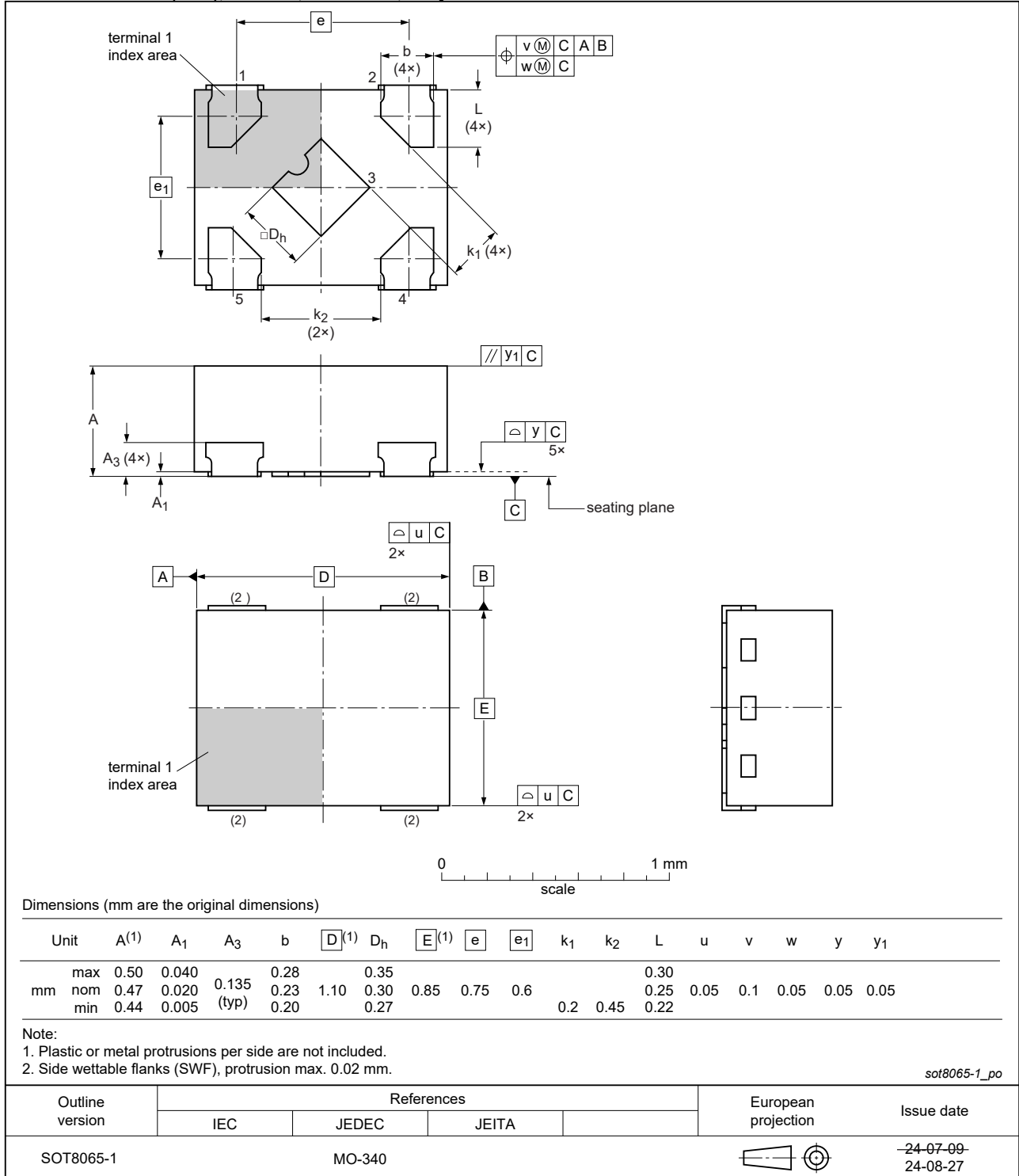


Fig. 9. Package outline SOT8065-1 (XSON5)

## 13. Abbreviations

Table 11. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC1G79_Q100 v.5	20250909	Product data sheet	-	74LVC1G79_Q100 v.4
Modifications:	<ul style="list-style-type: none"> <li>Type number 74VLC1G79GZ-Q100 (SOT8065-1/XSON5) added.</li> </ul>			
74LVC1G79_Q100 v.4	20230818	Product data sheet	-	74LVC1G79_Q100 v.3
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Section 2</a>: ESD specification updated according to the latest JEDEC standard.</li> </ul>			
74LVC1G79_Q100 v.3	20220201	Product data sheet	-	74LVC1G79_Q100 v.2
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li><a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li> <li><a href="#">Table 5</a>: Derating values for <math>P_{tot}</math> total power dissipation updated.</li> <li><a href="#">Fig. 7</a>: Package outline drawing SOT353-1 (TSSOP5) has changed.</li> </ul>			
74LVC1G79_Q100 v.2	20161212	Product data sheet	-	74LVC1G79_Q100 v.1
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Table 7</a>: The maximum limits for leakage current and supply current have changed.</li> </ul>			
74LVC1G79_Q100 v.1	20150512	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
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