

The wake-up timer IC allows for intermittent system operation by periodically waking up the system.

The S-35720 Series compares the timer value and the value set to the SET0 pin and the SET1 pin, and outputs a wake-up signal (interrupt signal) when the values match each other.

The timer of the S-35720 is a 24-bit binary-up counter.

4 types of wake-up time (interrupt time) can be selected depending on the SET0 pin and the SET1 pin settings.

## ■ Features

- |                                                   |                                                                                                 |
|---------------------------------------------------|-------------------------------------------------------------------------------------------------|
| • Wake-up function (Alarm interrupt function):    | Settable wake-up time (interrupt time)                                                          |
| • Low current consumption:                        | 0.2 $\mu$ A typ. (Quartz crystal: $C_L = 6.0$ pF, $V_{DD} = 3.0$ V, $T_a = +25^\circ\text{C}$ ) |
| • Wide range of operation voltage:                | 1.8 V to 5.5 V                                                                                  |
| • Built-in 32.768 kHz crystal oscillation circuit |                                                                                                 |
| • Operation temperature range:                    | $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$                                                |
| • Lead-free (Sn 100%), halogen-free               |                                                                                                 |

## ■ Applications

- IoT communications device
- Monitoring device
- Security device
- Battery system
- Energy harvesting system

## ■ Package

- TMSOP-8

## ■ Block Diagram

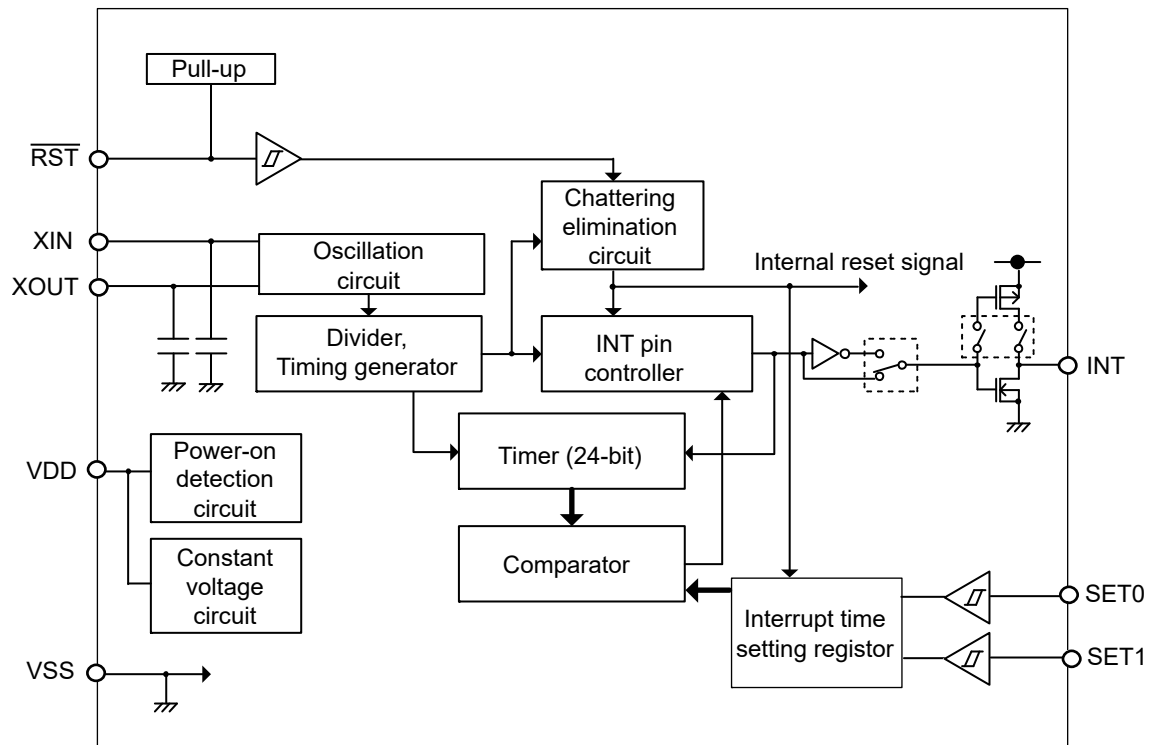
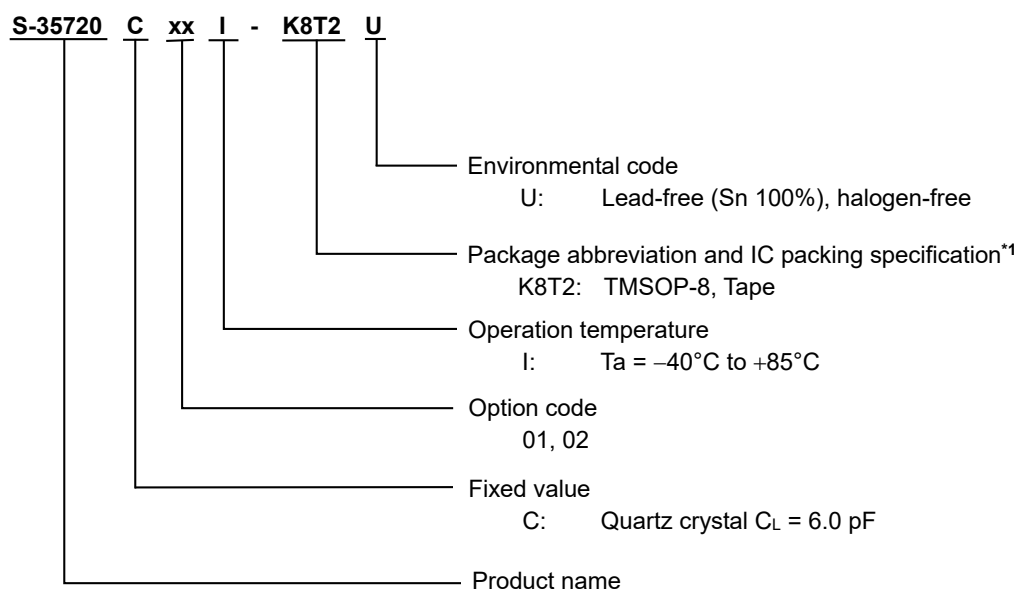


Figure 1

## ■ Product Name Structure

### 1. Product name



\*1. Refer to the tape drawing.

### 2. Package

Table 1 Package Drawing Codes

| Package Name | Dimension    | Tape         | Reel         |
|--------------|--------------|--------------|--------------|
| TMSOP-8      | FM008-A-P-SD | FM008-A-C-SD | FM008-A-R-SD |

### 3. Product name list

Table 2

| Product Name      | $\overline{\text{RST}}$ Pin | INT Pin Output Form   | Time-out Type                     | SET0 Pin, SET1 Pin Settings (SET0, SET1) |      |      |      |
|-------------------|-----------------------------|-----------------------|-----------------------------------|------------------------------------------|------|------|------|
|                   |                             |                       |                                   | 0, 0                                     | 0, 1 | 1, 0 | 1, 1 |
| S-35720C01I-K8T2U | With pull-up resistor       | Nch open-drain output | One-shot loop time-out (7.8 ms*1) | 60 s                                     | 10 s | 30 s | 1 s  |
| S-35720C02I-K8T2U | With pull-up resistor       | CMOS output           | One-shot loop time-out (125 ms*1) | 60 s                                     | 10 s | 30 s | 1 s  |

\*1. Values of pulse width. Refer to "■ INT Pin Interrupt Signal Output" for the details.

## ■ Pin Configuration

### 1. TMSOP-8

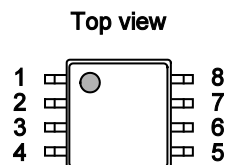


Figure 2

Table 3 List of Pins

| Pin No. | Symbol | Description                           | I/O    | Configuration                                                  |
|---------|--------|---------------------------------------|--------|----------------------------------------------------------------|
| 1       | RST    | Input pin for reset signal            | Input  | CMOS input (With pull-up resistor)                             |
| 2       | XOUT   | Connection pins for quartz crystal    | —      | —                                                              |
| 3       | XIN    |                                       |        |                                                                |
| 4       | VSS    | GND pin                               | —      | —                                                              |
| 5       | INT    | Output pin for interrupt signal       | Output | S-35720C01I: Nch open-drain output<br>S-35720C02I: CMOS output |
| 6       | SET0   | Input pins for interrupt time setting | Input  | CMOS input                                                     |
| 7       | SET1   |                                       |        |                                                                |
| 8       | VDD    | Pin for positive power supply         | —      | —                                                              |

## ■ Pin Functions

### 1. SET0, SET1 (Input for interrupt time setting) pins

These pins input the interrupt time setting signal. After the  $\overline{\text{RST}}$  pin changes from "L" to "H", the S-35720 Series takes the values set to the SET0 pin and the SET1 pin. As a result, even if the SET0 pin and the SET1 pin settings are changed during timer count-up action, the interrupt time does not change.

4 types of interrupt time can be selected depending on the SET0 pin and the SET1 pin settings.

### 2. $\overline{\text{RST}}$ (Input for reset signal) pin

This pin inputs the reset signal. The timer is reset when inputting "L" to the  $\overline{\text{RST}}$  pin, and the timer starts the operation when inputting "H". The  $\overline{\text{RST}}$  pin has a built-in chattering elimination circuit. Regarding the chattering elimination circuit, refer to "■ Chattering Elimination of RST Pin".

Besides, S-35720C01I and S-35720C02I are the products with pull-up resistor.

### 3. INT (Output for interrupt signal) pin

This pin outputs an interrupt signal. The interrupt signal is output when the time set to the SET0 pin and the SET1 pin comes. The interrupt signal output (time-out type) is one-shot loop time-out. Regarding the operation of the interrupt signal output, refer to "■ INT Pin Interrupt Signal Output".

Besides, S-35720C01I is the Nch open-drain output product, and S-35720C02I is the CMOS output product.

### 4. XIN, XOUT (Connection for quartz crystal) pins

Connect a quartz crystal between the XIN pin and the XOUT pin.

### 5. VDD (Positive power supply) pin

Connect this pin with a positive power supply.

Regarding the values of voltage to be supplied, refer to "■ Recommended Operation Conditions".

### 6. VSS pin

Connect this pin to GND.

## ■ Equivalent Circuits of Pins

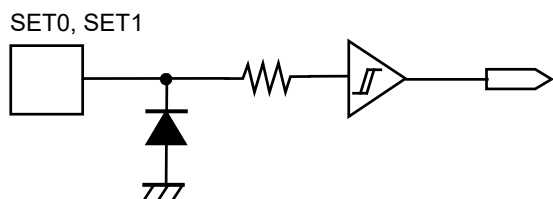


Figure 3 SET0 Pin, SET1 Pin

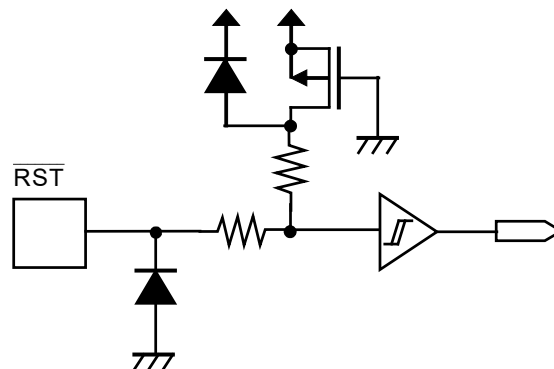


Figure 4  $\overline{\text{RST}}$  Pin (S-35720C01I, S-35720C02I / With Pull-up Resistor)

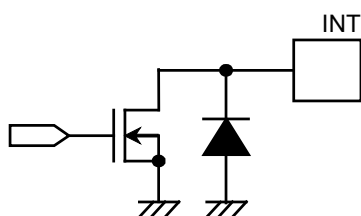


Figure 5 INT Pin (S-35720C01I / Nch Open-drain Output)

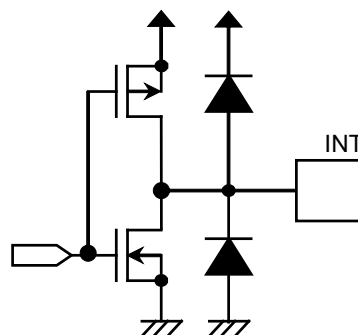


Figure 6 INT Pin (S-35720C02I / CMOS Output)

## ■ Absolute Maximum Ratings

Table 4

| Item                                        | Symbol    | Applied Pin       | Absolute Maximum Rating                            | Unit |
|---------------------------------------------|-----------|-------------------|----------------------------------------------------|------|
| Power supply voltage                        | $V_{DD}$  | –                 | $V_{SS} - 0.3$ to $V_{SS} + 6.5$                   | V    |
| Input voltage                               | $V_{IN}$  | SET0, SET1        | $V_{SS} - 0.3$ to $V_{SS} + 6.5$                   | V    |
|                                             |           | RST               | $V_{SS} - 0.3$ to $V_{DD} + 0.3 \leq V_{SS} + 6.5$ | V    |
| Output voltage                              | $V_{OUT}$ | INT <sup>*1</sup> | $V_{SS} - 0.3$ to $V_{SS} + 6.5$                   | V    |
|                                             |           | INT <sup>*2</sup> | $V_{SS} - 0.3$ to $V_{DD} + 0.3 \leq V_{SS} + 6.5$ | V    |
| Operation ambient temperature <sup>*3</sup> | $T_{opr}$ | –                 | –40 to +85                                         | °C   |
| Storage temperature                         | $T_{stg}$ | –                 | –55 to +150                                        | °C   |

\*1. S-35720C01I (Nch open-drain output)

\*2. S-35720C02I (CMOS output)

\*3. Conditions with no condensation or frost. Condensation or frost causes short-circuiting between pins, resulting in a malfunction.

**Caution** The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

## ■ Recommended Operation Conditions

Table 5

(V<sub>SS</sub> = 0 V)

| Item                           | Symbol   | Condition           | Min. | Typ. | Max. | Unit |
|--------------------------------|----------|---------------------|------|------|------|------|
| Operation power supply voltage | $V_{DD}$ | Ta = –40°C to +85°C | 1.8  | –    | 5.5  | V    |

## ■ Oscillation Characteristics

Table 6

(Ta = +25°C, V<sub>DD</sub> = 3.0 V, V<sub>SS</sub> = 0 V unless otherwise specified)(Quartz crystal (NX3215SD, C<sub>L</sub> = 6.0 pF) manufactured by Nihon Dempa Kogyo Co., Ltd.)

| Item                                       | Symbol      | Condition         | Min. | Typ. | Max. | Unit |
|--------------------------------------------|-------------|-------------------|------|------|------|------|
| Oscillation start voltage                  | $V_{STA}$   | Within 10 seconds | 1.8  | –    | 5.5  | V    |
| Oscillation start time                     | $t_{STA}$   | –                 | –    | –    | 1    | s    |
| IC-to-IC frequency deviation <sup>*1</sup> | $\delta IC$ | –                 | –20  | –    | +20  | ppm  |

\*1. Reference value

## ■ DC Electrical Characteristics

Table 7

(Ta = -40°C to +85°C, V<sub>SS</sub> = 0 V unless otherwise specified)  
(Quartz crystal (NX3215SD, C<sub>L</sub> = 6.0 pF) manufactured by Nihon Dempa Kogyo Co., Ltd.)

| Item                              | Symbol           | Applied Pin     | Condition                                                                    | Min.                  | Typ. | Max.                  | Unit |
|-----------------------------------|------------------|-----------------|------------------------------------------------------------------------------|-----------------------|------|-----------------------|------|
| Current consumption 1             | I <sub>DD1</sub> | —               | V <sub>DD</sub> = 3.0 V,<br>RST pin = V <sub>DD</sub> ,<br>INT pin = no load | —                     | 0.2  | 0.35                  | μA   |
| High level input leakage current  | I <sub>IZH</sub> | SET0, SET1, RST | V <sub>IN</sub> = V <sub>DD</sub>                                            | -0.5                  | —    | 0.5                   | μA   |
| Low level input leakage current   | I <sub>IZL</sub> | SET0, SET1      | V <sub>IN</sub> = V <sub>SS</sub>                                            | -0.5                  | —    | 0.5                   | μA   |
| High level output leakage current | I <sub>OZH</sub> | INT*1           | V <sub>OUT</sub> = V <sub>DD</sub>                                           | -0.5                  | —    | 0.5                   | μA   |
| Low level output leakage current  | I <sub>OZL</sub> | INT*2           | V <sub>OUT</sub> = V <sub>SS</sub>                                           | -0.5                  | —    | 0.5                   | μA   |
| High level input voltage          | V <sub>IH</sub>  | SET0, SET1, RST | —                                                                            | 0.7 × V <sub>DD</sub> | —    | V <sub>SS</sub> + 5.5 | V    |
| Low level input voltage           | V <sub>IL</sub>  | SET0, SET1, RST | —                                                                            | V <sub>SS</sub> - 0.3 | —    | 0.3 × V <sub>DD</sub> | V    |
| High level output voltage         | V <sub>OH</sub>  | INT             | I <sub>OH</sub> = -0.4 mA                                                    | 0.8 × V <sub>DD</sub> | —    | —                     | V    |
| Low level output voltage          | V <sub>OL</sub>  | INT             | I <sub>OL</sub> = 2.0 mA                                                     | —                     | —    | 0.4                   | V    |
| Low level input current           | I <sub>IL</sub>  | RST             | V <sub>DD</sub> = 3.0 V, V <sub>IN</sub> = V <sub>SS</sub>                   | -100                  | -30  | -5                    | μA   |

\*1. S-35720C01I (Nch open-drain output)

\*2. S-35720C02I (CMOS output)

## ■ INT Pin Interrupt Signal Output

The  $\overline{\text{RST}}$  pin of the S-35720 Series has a built-in chattering elimination circuit. Therefore, after the  $\overline{\text{RST}}$  pin changes from "L" to "H", a delay occurs until the timer starts the count-up action. Furthermore, an internal circuit delay occurs until the first interrupt signal occurs. Since the maximum delay time after the  $\overline{\text{RST}}$  pin changes from "L" to "H" is approximately 700 ms, the timing for the occurrence of the first interrupt signal is delayed.

After the  $\overline{\text{RST}}$  pin changes from "L" to "H", the S-35720 Series takes the values set to the SET0 pin and the SET1 pin. As a result, even if the SET0 pin and the SET1 pin settings are changed during timer count-up action, the interrupt time does not change.

### 1. One-shot loop time-out

One-shot loop time-out is a type to output the "L" pulse interrupt signal repeatedly from the INT pin.

After the  $\overline{\text{RST}}$  pin changes from "L" to "H", the timer starts the operation. Then, the INT pin outputs "L" pulse when the timer value matches the value set to the SET0 pin and the SET1 pin<sup>\*1</sup>. After that, the S-35720 Series resets the timer automatically, and restarts a count-up action.

If "L" is input to the  $\overline{\text{RST}}$  pin before the timer value matches the value set to the SET0 pin and the SET1 pin<sup>\*1</sup>, the timer is reset.

<sup>\*1</sup>. 4 types of interrupt time can be selected depending on the SET0 pin and the SET1 pin settings.

**Remark** The above description is the example of S-35720C01I (Nch open-drain output).

In S-35720C02I (CMOS output), the INT pin output is the inverse logic of S-35720C01I.

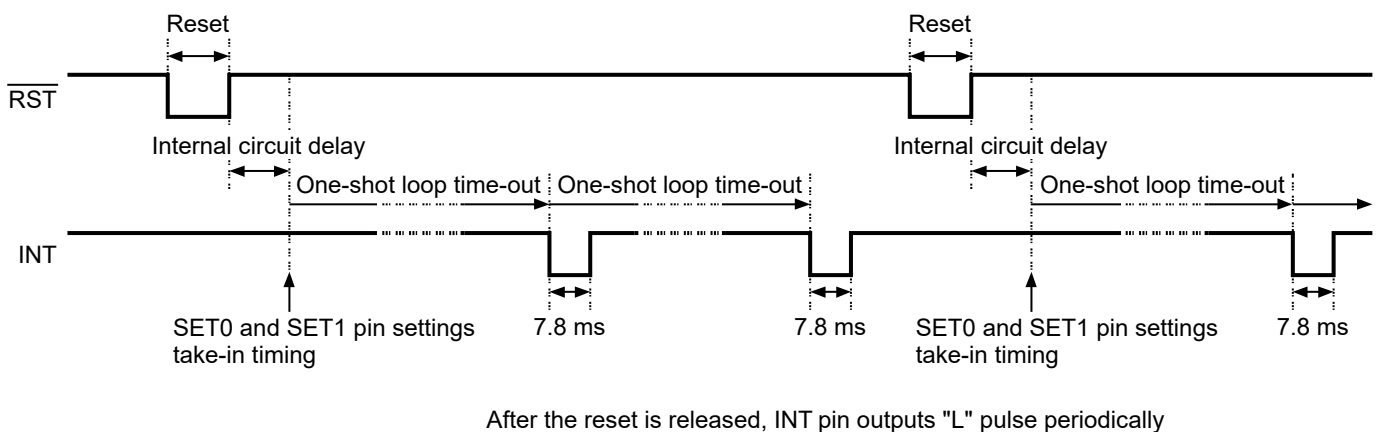


Figure 7 Output Timing of One-shot Loop Time-out (S-35720C01I / Nch Open-drain Output)

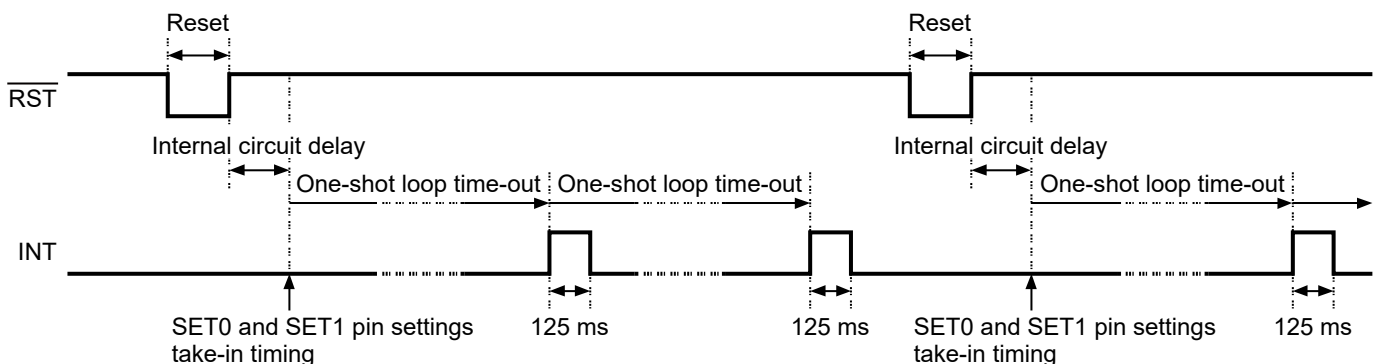
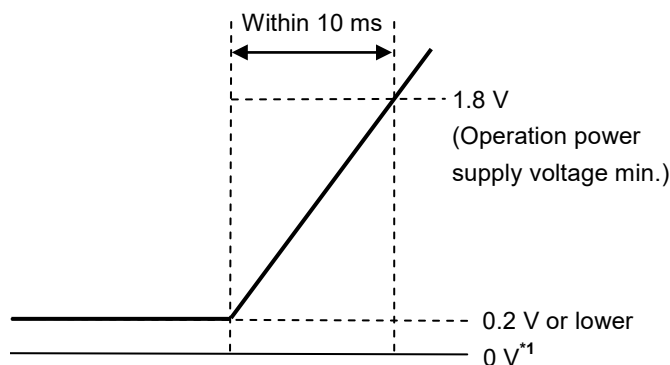


Figure 8 Output Timing of One-shot Loop Time-out (S-35720C02I / CMOS Output)

## ■ Power-on Detection Circuit

In order for the power-on detection circuit to operate normally, raise the power supply voltage of the IC from 0.2 V or lower so that it reaches 1.8 V of the operation power supply voltage minimum value within 10 ms, as shown in **Figure 9**.



\*1. 0 V means that there is no potential difference between the VDD pin and the VSS pin of the S-35720 Series.

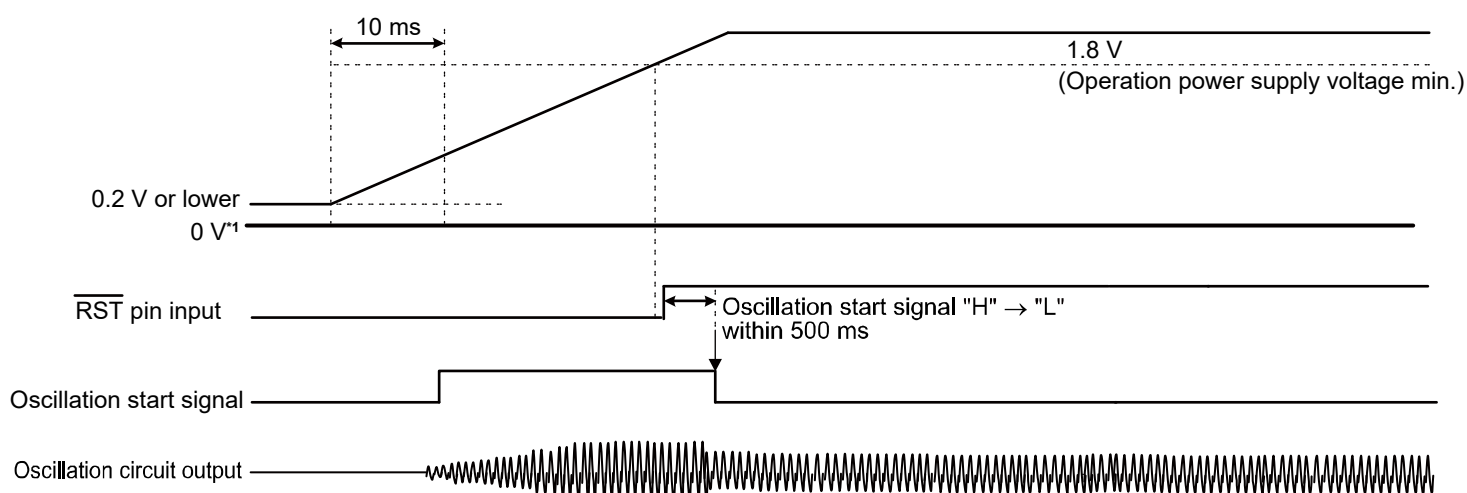
**Figure 9 How to Raise the Power Supply Voltage**

If the power supply voltage of the S-35720 Series cannot be raised under the above conditions, the power-on detection circuit may not operate normally and an oscillation may not start. In such case, perform the operations shown in "1. When power supply voltage is raised at RST pin = "L" " and "2. When power supply voltage is raised at RST pin = "H" ".

### 1. When power supply voltage is raised at $\overline{\text{RST}}$ pin = "L"

Set the  $\overline{\text{RST}}$  pin to "L" until the power supply voltage reaches 1.8 V or higher. While the  $\overline{\text{RST}}$  pin is set to "L", the oscillation start signal becomes "H", and the crystal oscillation circuit normally oscillates. If the RST pin is set to "H" after the power supply voltage reaches 1.8 V, the oscillation start signal becomes "L" within 500 ms, and the oscillation status is maintained.

The current consumption increases by 30  $\mu\text{A}$  typ. while the  $\overline{\text{RST}}$  pin is set to "L".

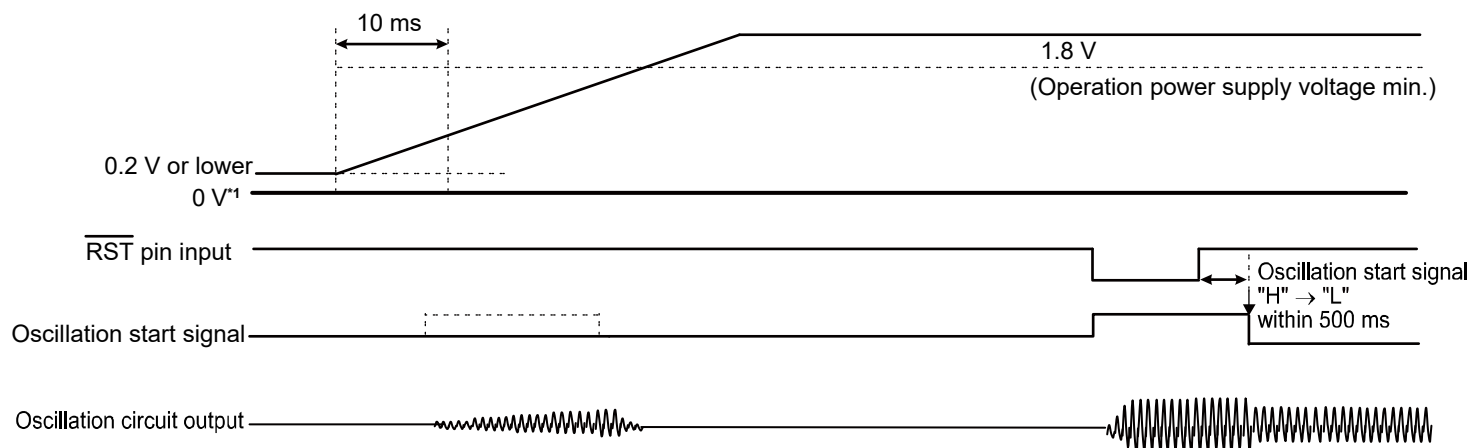


\*1. 0 V means that there is no potential difference between the VDD pin and the VSS pin of the S-35720 Series.

**Figure 10 When Power Supply Voltage is Raised at  $\overline{\text{RST}}$  Pin = "L"**

## 2. When power supply voltage is raised at $\overline{\text{RST}}$ pin = "H"

Set the  $\overline{\text{RST}}$  pin to "L" after the power supply voltage reaches 1.8 V or higher. If the  $\overline{\text{RST}}$  pin is set to "L" for 500 ms or longer, the oscillation start signal becomes "H", and the crystal oscillation circuit normally oscillates. After that, if the  $\overline{\text{RST}}$  pin is set to "H", the oscillation start signal becomes "L" within 500 ms, and the oscillation status is maintained. The current consumption increases by 30  $\mu\text{A}$  typ. while the  $\overline{\text{RST}}$  pin is set to "L".



\*1. 0 V means that there is no potential difference between the VDD pin and the VSS pin of the S-35720 Series.

**Figure 11 When Power Supply Voltage is Raised at  $\overline{\text{RST}}$  Pin = "H"**

The  $\overline{\text{RST}}$  pin has a built-in chattering elimination circuit.

Regarding the chattering elimination of the  $\overline{\text{RST}}$  pin, refer to "■ Chattering Elimination of  $\overline{\text{RST}}$  Pin".

## ■ Chattering Elimination of $\overline{\text{RST}}$ Pin

The  $\overline{\text{RST}}$  pin has a built-in chattering elimination circuit, and the output logic is active "L".

Sampling is carried out 3 times at a clock period of 8 Hz and the  $\overline{\text{RST}}$  pin input signal is verified. If all of the sampling results are "L", the counter is reset, if all the results are "H", a count-up action is started.

The chattering elimination circuit can eliminate the pulse width of 2 periods (approximately 0.25 seconds) of the clock (8 Hz). To determine the  $\overline{\text{RST}}$  pin "L" or "H" input, maintain the  $\overline{\text{RST}}$  pin "L" or "H" input during the period longer than 3.5 periods (0.438 seconds) of clock (8 Hz). This is because, for example, if the  $\overline{\text{RST}}$  pin "L" or "H" input is 0.375 seconds, the input may not be determined depending on the clock timing.

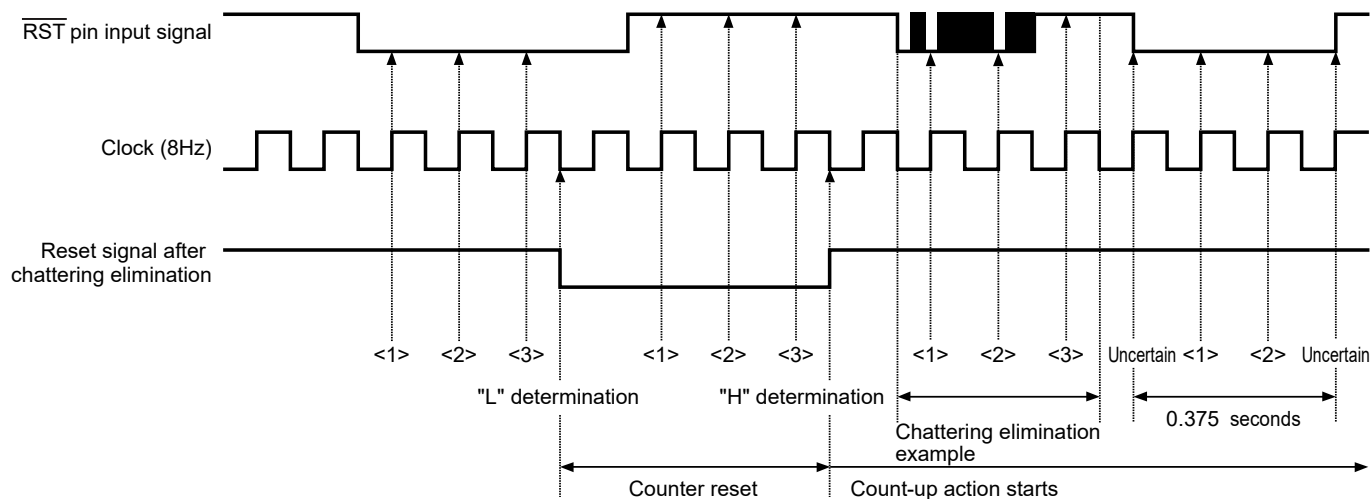
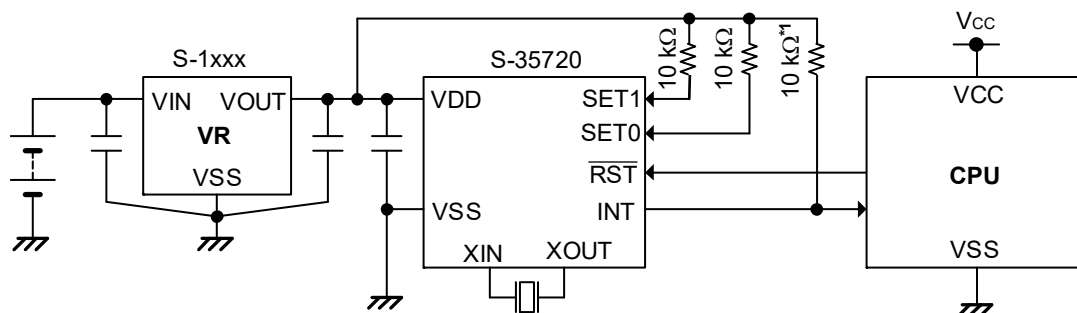


Figure 12 Example: Timing Chart of Chattering Elimination

## ■ Example of Application Circuit



\*1. This resistor is unnecessary in S-35720C02I (CMOS output).

Figure 13

**Caution** The above connection diagram does not guarantee operation. Set the constants after performing sufficient evaluation using the actual application.

## ■ Configuration of Crystal Oscillation Circuit

Since the S-35720 Series has built-in capacitors ( $C_g$  and  $C_d$ ), adjustment of oscillation frequency is unnecessary. However, the crystal oscillation circuit is sensitive to external noise and parasitic capacitance ( $C_P$ ), these effects may become a factor to worsen the clock accuracy. Therefore, the following steps are recommended for optimizing the configuration of crystal oscillation circuit.

- Locate the bypass capacitor adjacent to the power supply pin of the S-35720 Series.
- Place the S-35720 Series and the quartz crystal as close to each other as possible, and shorten the wiring.
- Increase the insulation resistance between pins and the board wiring patterns of XIN and XOUT.
- Do not place any signal or power lines close to the crystal oscillation circuit.
- Locate the GND layer immediately below the crystal oscillation circuit.

(In the case of a multi-layer board, only the layer farthest from the crystal oscillation circuit should be located as the GND layer. Do not locate a circuit pattern on the intermediate layers.)

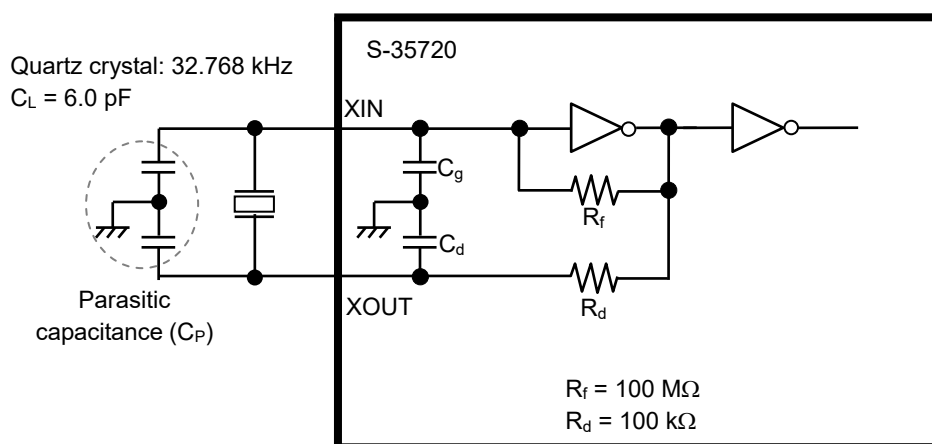


Figure 14 Configuration of Crystal Oscillation Circuit

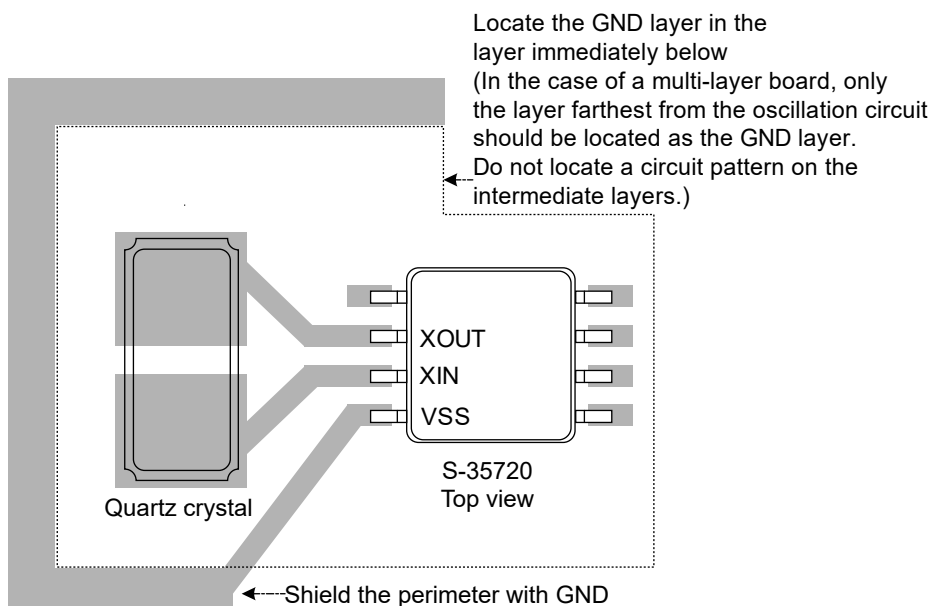


Figure 15 Example of Recommended Connection Pattern Diagram

**Caution** Oscillation characteristics are subject to the variation of each component such as board parasitic capacitance, parasitic resistance, quartz crystal, and external capacitor. When configuring crystal oscillation circuit, pay sufficient attention for them.

**■ Cautions When Using Quartz Crystal**

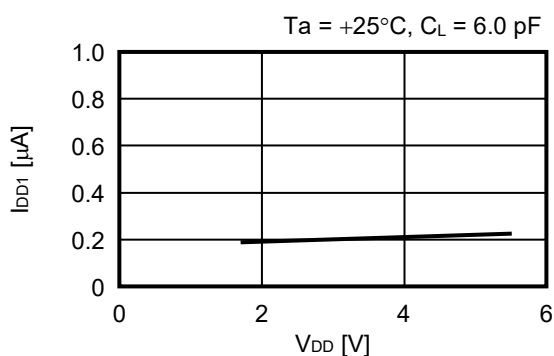
Request a matching evaluation between the IC and a quartz crystal to the quartz crystal maker.

**■ Precautions**

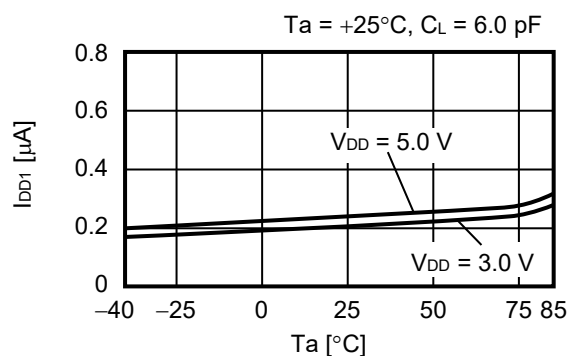
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

## ■ Characteristics (Typical Data)

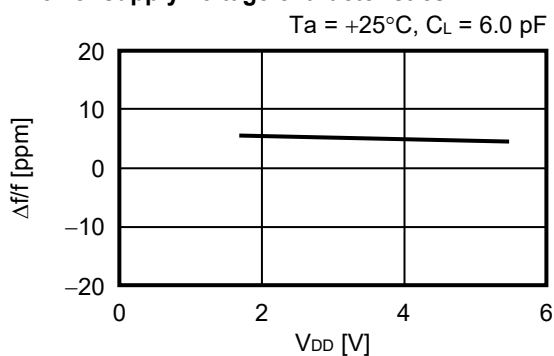
### 1. Current consumption 1 vs. Power supply voltage characteristics



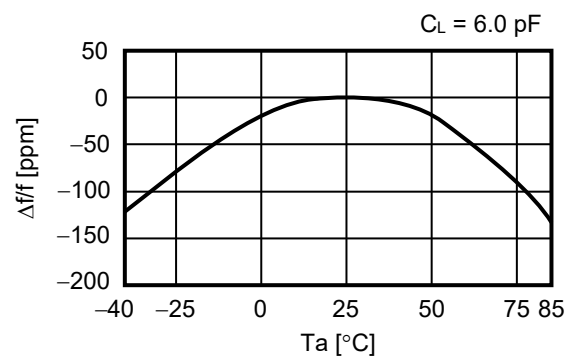
### 2. Current consumption 1 vs. Temperature characteristics



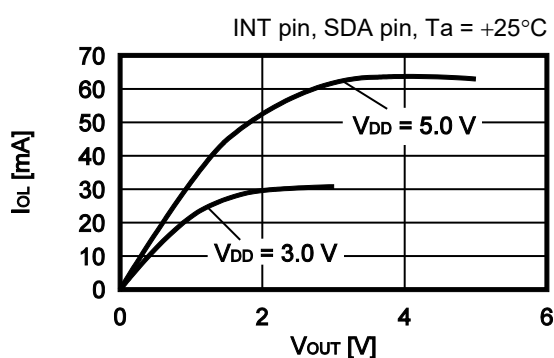
### 3. Oscillation frequency vs. Power supply voltage characteristics



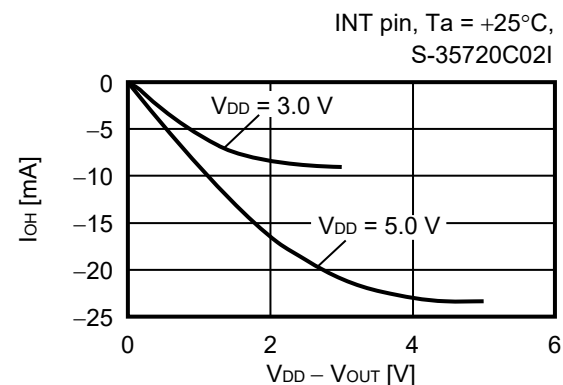
### 4. Oscillation frequency vs. Temperature characteristics



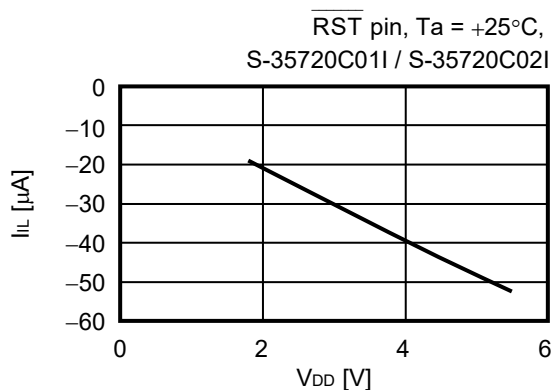
### 5. Low level output current vs. Output voltage characteristics

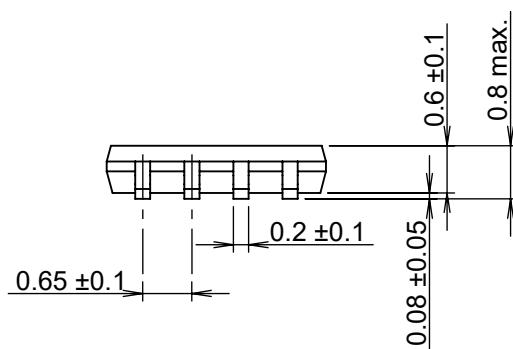
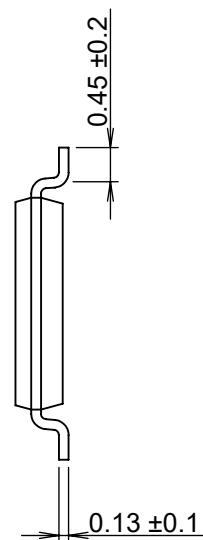
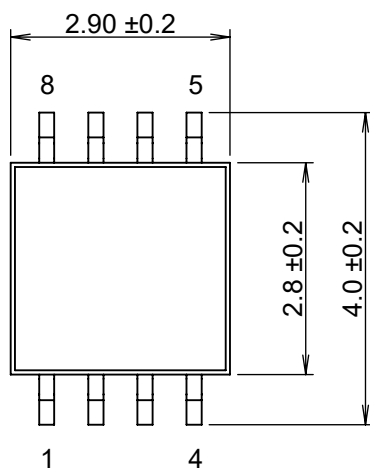


### 6. High level output current vs. $V_{DD} - V_{OUT}$ characteristics



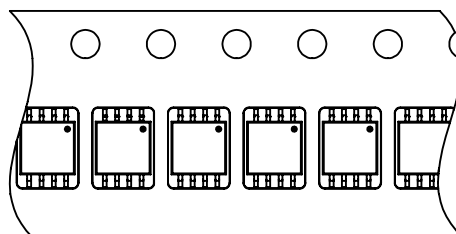
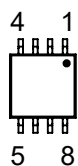
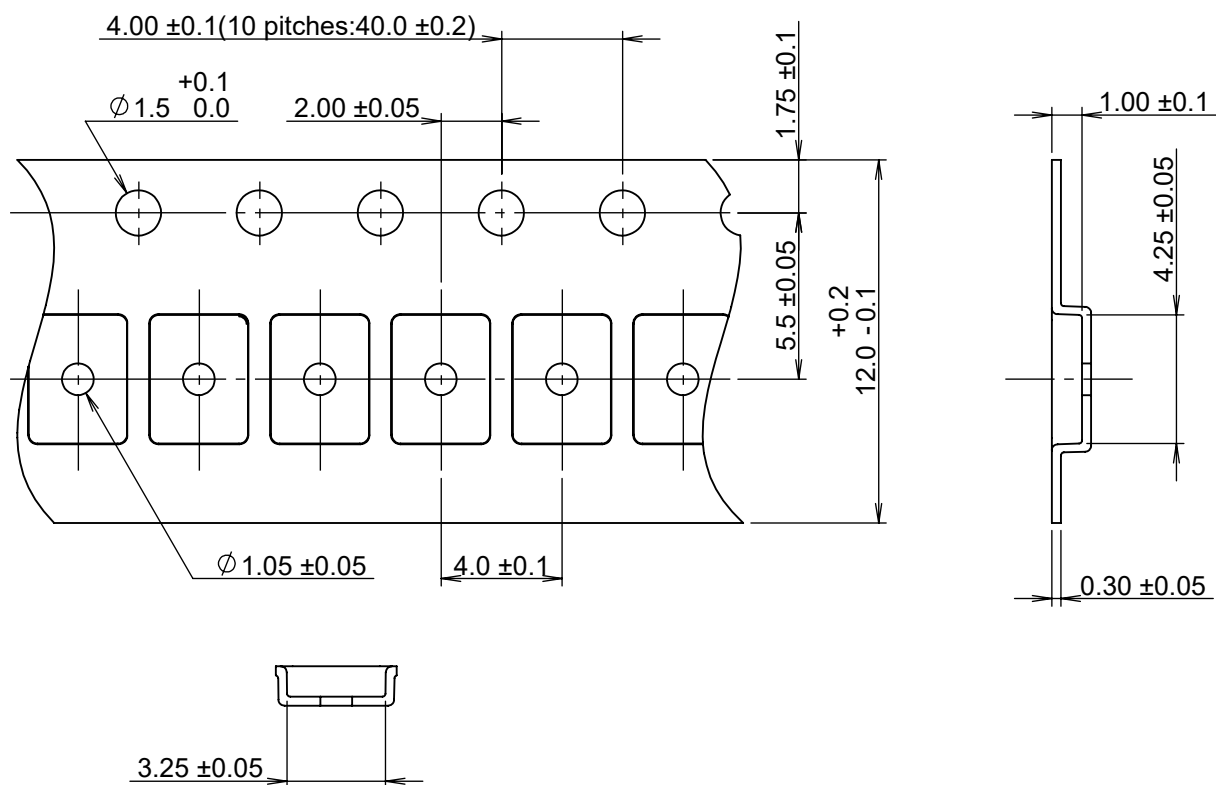
### 7. Low level input current vs. Power supply voltage characteristics





No.FM008-A-P-SD-1.2

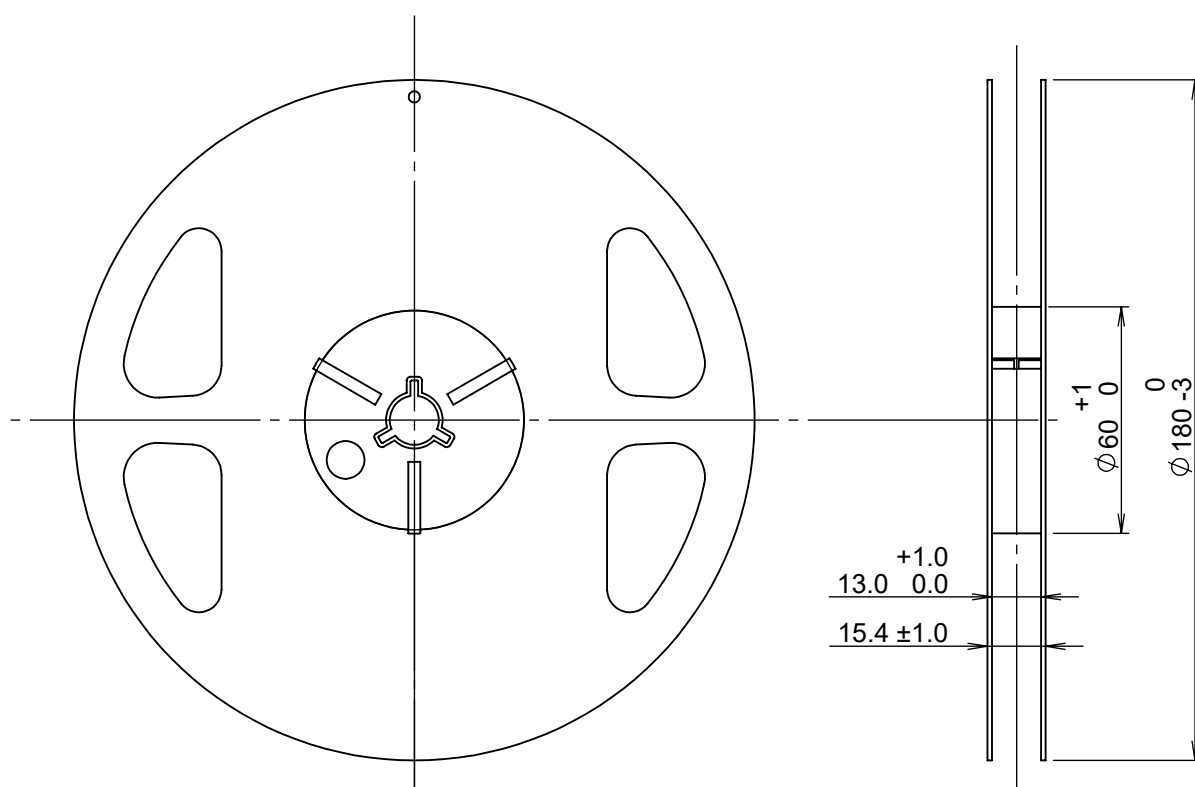
|            |                         |
|------------|-------------------------|
| TITLE      | TMSOP8-A-PKG Dimensions |
| No.        | FM008-A-P-SD-1.2        |
| ANGLE      |                         |
| UNIT       | mm                      |
|            |                         |
| ABLIC Inc. |                         |



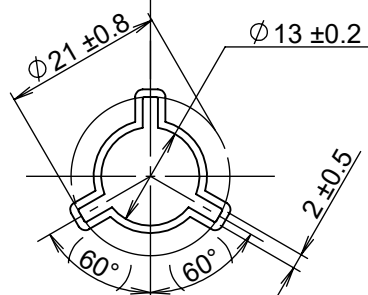
Feed direction

No. FM008-A-C-SD-3.0

|            |                       |
|------------|-----------------------|
| TITLE      | TMSOP8-A-Carrier Tape |
| No.        | FM008-A-C-SD-3.0      |
| ANGLE      |                       |
| UNIT       | mm                    |
|            |                       |
| ABLIC Inc. |                       |



Enlarged drawing in the central part



No. FM008-A-R-SD-2.0

|            |                  |      |       |
|------------|------------------|------|-------|
| TITLE      | TMSOP8-A-Reel    |      |       |
| No.        | FM008-A-R-SD-2.0 |      |       |
| ANGLE      |                  | QTY. | 4,000 |
| UNIT       | mm               |      |       |
|            |                  |      |       |
| ABLIC Inc. |                  |      |       |

## Disclaimers (Handling Precautions)

1. All the information described herein (product data, specifications, figures, tables, programs, algorithms and application circuit examples, etc.) is current as of publishing date of this document and is subject to change without notice.
2. The circuit examples and the usages described herein are for reference only, and do not guarantee the success of any specific mass-production design.  
ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the reasons other than the products described herein (hereinafter "the products") or infringement of third-party intellectual property right and any other right due to the use of the information described herein.
3. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the incorrect information described herein.
4. Be careful to use the products within their ranges described herein. Pay special attention for use to the absolute maximum ratings, operation voltage range and electrical characteristics, etc.  
ABLIC Inc. is not liable for any losses, damages, claims or demands caused by failures and / or accidents, etc. due to the use of the products outside their specified ranges.
5. Before using the products, confirm their applications, and the laws and regulations of the region or country where they are used and verify suitability, safety and other factors for the intended use.
6. When exporting the products, comply with the Foreign Exchange and Foreign Trade Act and all other export-related laws, and follow the required procedures.
7. The products are strictly prohibited from using, providing or exporting for the purposes of the development of weapons of mass destruction or military use. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by any provision or export to the person or entity who intends to develop, manufacture, use or store nuclear, biological or chemical weapons or missiles, or use any other military purposes.
8. The products are not designed to be used as part of any device or equipment that may affect the human body, human life, or assets (such as medical equipment, disaster prevention systems, security systems, combustion control systems, infrastructure control systems, vehicle equipment, traffic systems, in-vehicle equipment, aviation equipment, aerospace equipment, and nuclear-related equipment), excluding when specified for in-vehicle use or other uses by ABLIC, Inc. Do not apply the products to the above listed devices and equipments.  
ABLIC Inc. is not liable for any losses, damages, claims or demands caused by unauthorized or unspecified use of the products.
9. In general, semiconductor products may fail or malfunction with some probability. The user of the products should therefore take responsibility to give thorough consideration to safety design including redundancy, fire spread prevention measures, and malfunction prevention to prevent accidents causing injury or death, fires and social damage, etc. that may ensue from the products' failure or malfunction.  
The entire system in which the products are used must be sufficiently evaluated and judged whether the products are allowed to apply for the system on customer's own responsibility.
10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.
12. When disposing of the products, comply with the laws and ordinances of the country or region where they are used.
13. The information described herein contains copyright information and know-how of ABLIC Inc. The information described herein does not convey any license under any intellectual property rights or any other rights belonging to ABLIC Inc. or a third party. Reproduction or copying of the information from this document or any part of this document described herein for the purpose of disclosing it to a third-party is strictly prohibited without the express permission of ABLIC Inc.
14. For more details on the information described herein or any other questions, please contact ABLIC Inc.'s sales representative.
15. This Disclaimers have been delivered in a text using the Japanese language, which text, despite any translations into the English language and the Chinese language, shall be controlling.

2.4-2019.07