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June 2016

FDC021N30

N-Channel PowerTrench[®] MOSFET

30 V, 6.1 A, 26 mΩ

Features

- Max $r_{DS(on)}$ = 26 mΩ at $V_{GS} = 10$ V, $I_D = 6.1$ A
- Max $r_{DS(on)}$ = 33 mΩ at $V_{GS} = 4.5$ V, $I_D = 5.3$ A
- High Performance Trench Technology for Extremely Low $r_{DS(on)}$
- High Power and Current Handling Capability in a Widely Used Surface Mount Package
- Fast Switching Speed
- RoHS Compliant

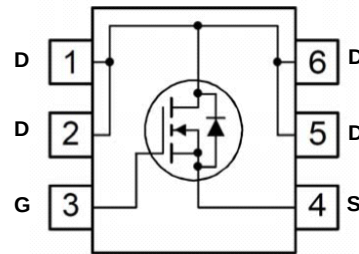
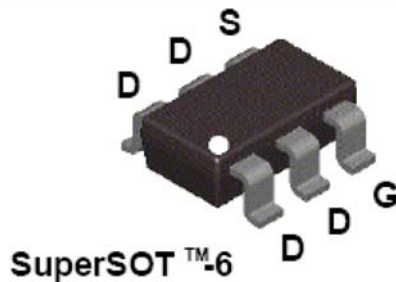


General Description

This N-Channel PowerTrench MOSFET is produced using Fairchild's advanced PowerTrench[®] process that has been especially tailored to minimize on-state resistance and yet maintain low gate charge for superior switching performance.

Applications

- Load Switch
- Battery Protection
- Power Management



MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage (Note 3)	± 20	V
I_D	-Continuous $T_A = 25^\circ\text{C}$ (Note 1a)	6.1	A
	-Pulsed (Note 4)	62	
P_D	Power Dissipation (Note 1a)	1.6	W
	Power Dissipation (Note 1b)	0.7	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	78	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	175	$^\circ\text{C/W}$

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
21N	FDC021N30	SSOT-6 TM	7"	8 mm	3000 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to 25°C		16		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\ \text{V}$, $V_{GS} = 0\ \text{V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = 20\ \text{V}$, $V_{DS} = 0\ \text{V}$			100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\ \mu\text{A}$	1.0	1.8	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to 25°C		-5		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}$, $I_D = 6.1\ \text{A}$		19	26	m Ω
		$V_{GS} = 4.5\ \text{V}$, $I_D = 5.3\ \text{A}$		23	33	
		$V_{GS} = 10\ \text{V}$, $I_D = 6.1\ \text{A}$, $T_J = 125^\circ\text{C}$		26	37	
g_{FS}	Forward Transconductance	$V_{DS} = 5\ \text{V}$, $I_D = 6.1\ \text{A}$		30		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 15\ \text{V}$, $V_{GS} = 0\ \text{V}$, $f = 1\ \text{MHz}$		510	710	pF
C_{oss}	Output Capacitance			170	240	pF
C_{rss}	Reverse Transfer Capacitance			22	30	pF
R_g	Gate Resistance		0.1	1.3	2.6	Ω

Switching Characteristics

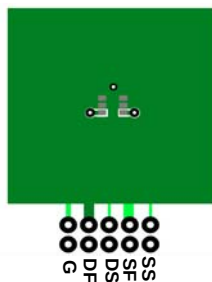
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\ \text{V}$, $I_D = 6.1\ \text{A}$, $V_{GS} = 10\ \text{V}$, $R_{GEN} = 6\ \Omega$		6	12	ns
t_r	Rise Time			2	10	ns
$t_{d(off)}$	Turn-Off Delay Time			13	24	ns
t_f	Fall Time			2	10	ns
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\ \text{V}$ to $10\ \text{V}$	$V_{DD} = 15\ \text{V}$, $I_D = 6.1\ \text{A}$	7.7	10.8	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\ \text{V}$ to $4.5\ \text{V}$		3.7	5.2	nC
Q_{gs}	Gate to Source Charge			1.4		nC
Q_{gd}	Gate to Drain "Miller" Charge			1.1		nC

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}$, $I_S = 6.1\ \text{A}$ (Note 2)		0.8	1.2	V
t_{rr}	Reverse Recovery Time	$I_F = 6.1\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$		14	25	ns
Q_{rr}	Reverse Recovery Charge			3	10	nC

Notes:

- 1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.
 $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. $78\ ^\circ\text{C}/\text{W}$ when mounted on
a $1\ \text{in}^2$ pad of 2 oz. copper



b. $175\ ^\circ\text{C}/\text{W}$ when mounted on
a minimum pad of 2 oz. copper

2: Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%.

3: As an N-ch device, the negative V_{GS} rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

4: Pulsed I_D please refer to Fig 11 SOA graph for more details.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

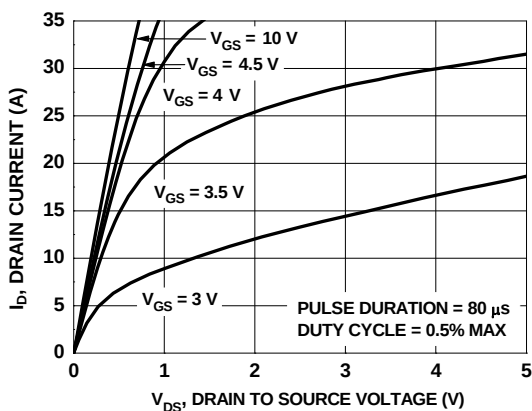


Figure 1. On-Region Characteristics

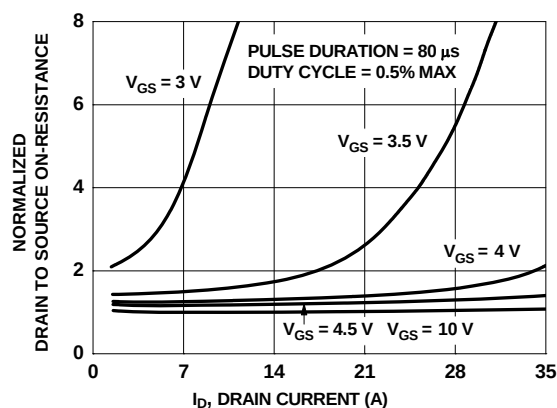


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

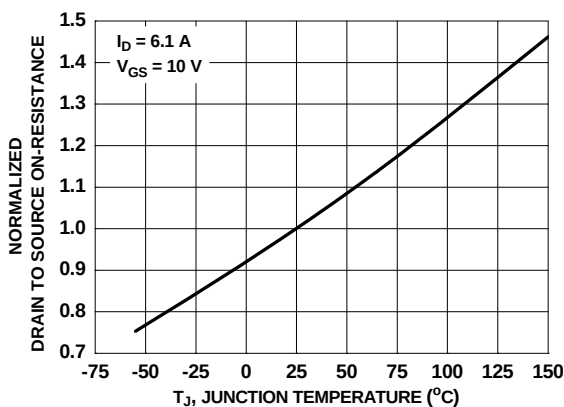


Figure 3. Normalized On-Resistance vs. Junction Temperature

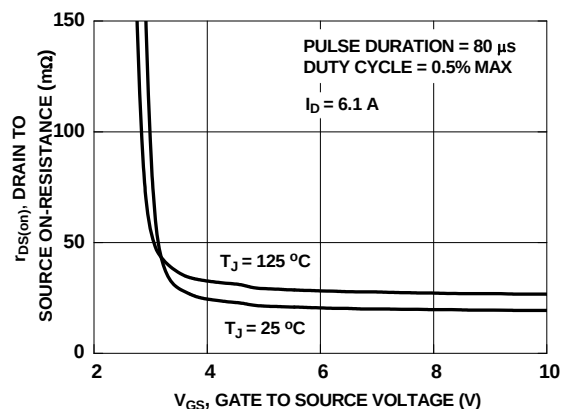


Figure 4. On-Resistance vs. Gate to Source Voltage

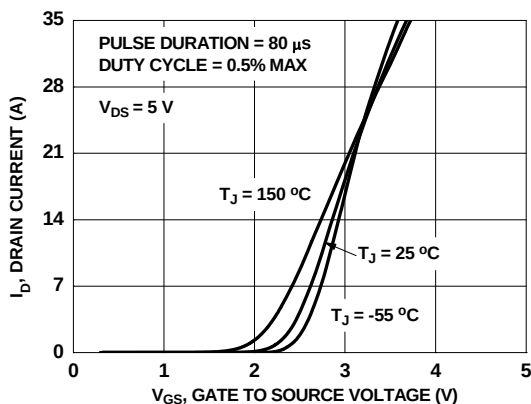


Figure 5. Transfer Characteristics

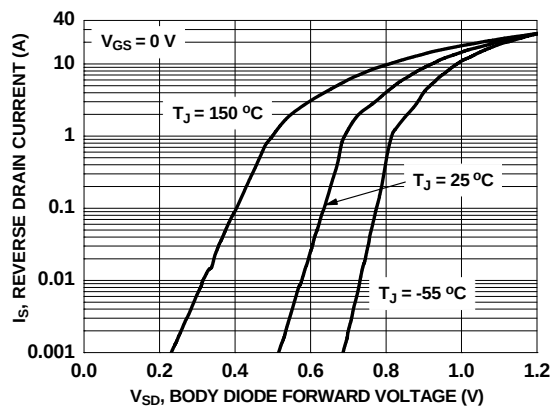


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

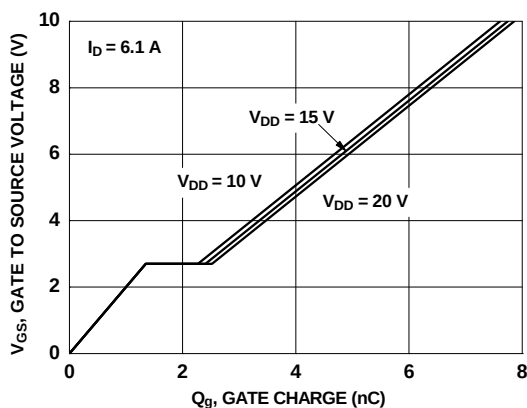


Figure 7. Gate Charge Characteristics

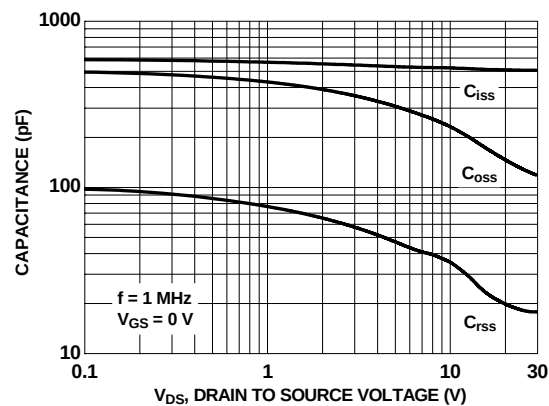


Figure 8. Capacitance vs. Drain to Source Voltage

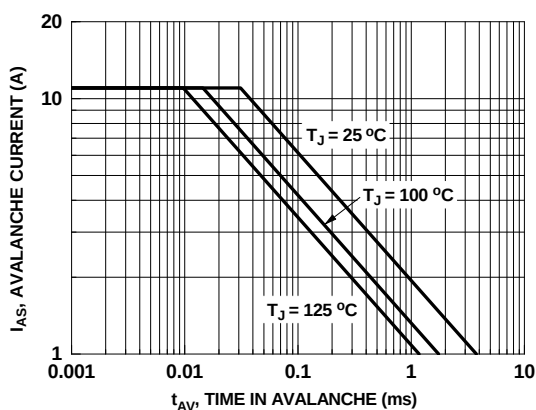


Figure 9. Unclamped Inductive Switching Capability

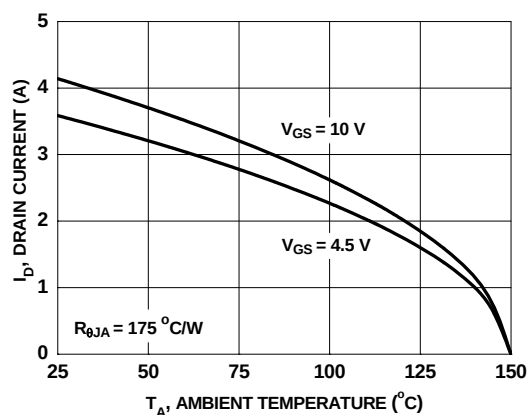


Figure 10. Maximum Continuous Drain Current vs. Ambient Temperature

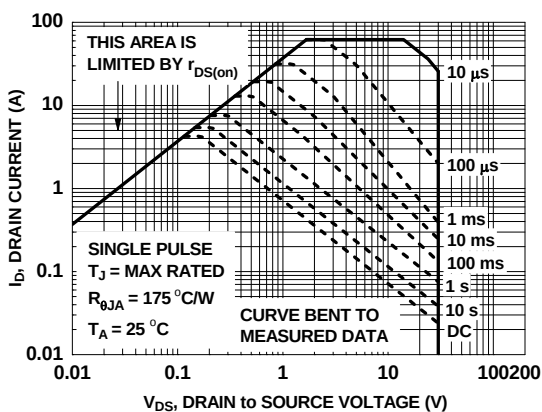


Figure 11. Forward Bias Safe Operating Area

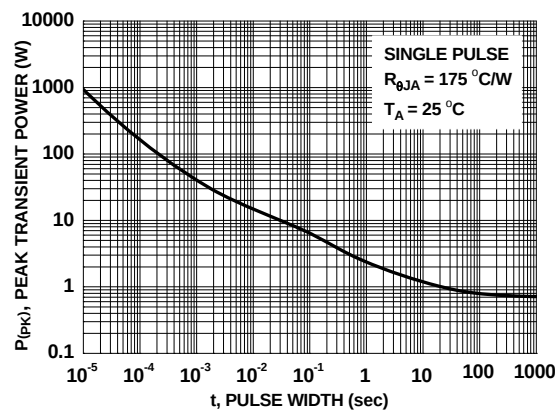


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

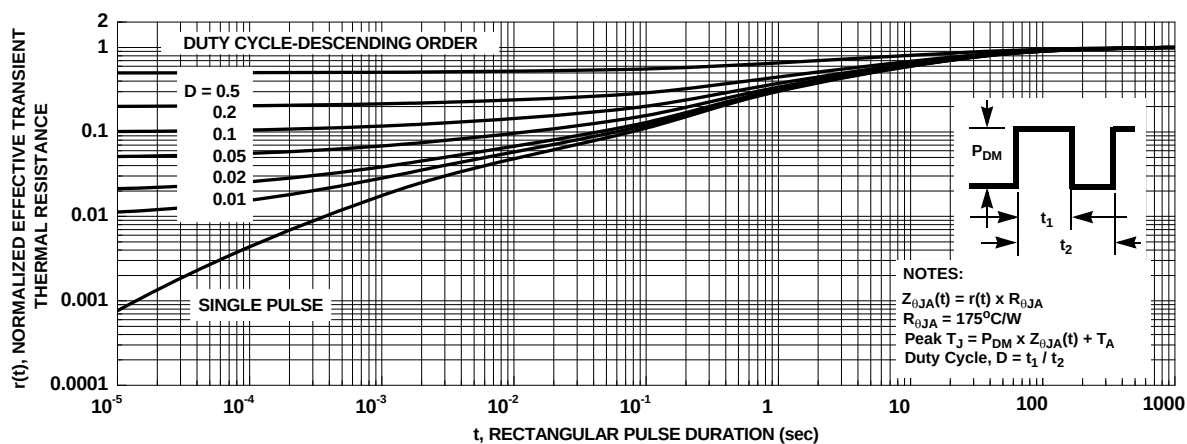
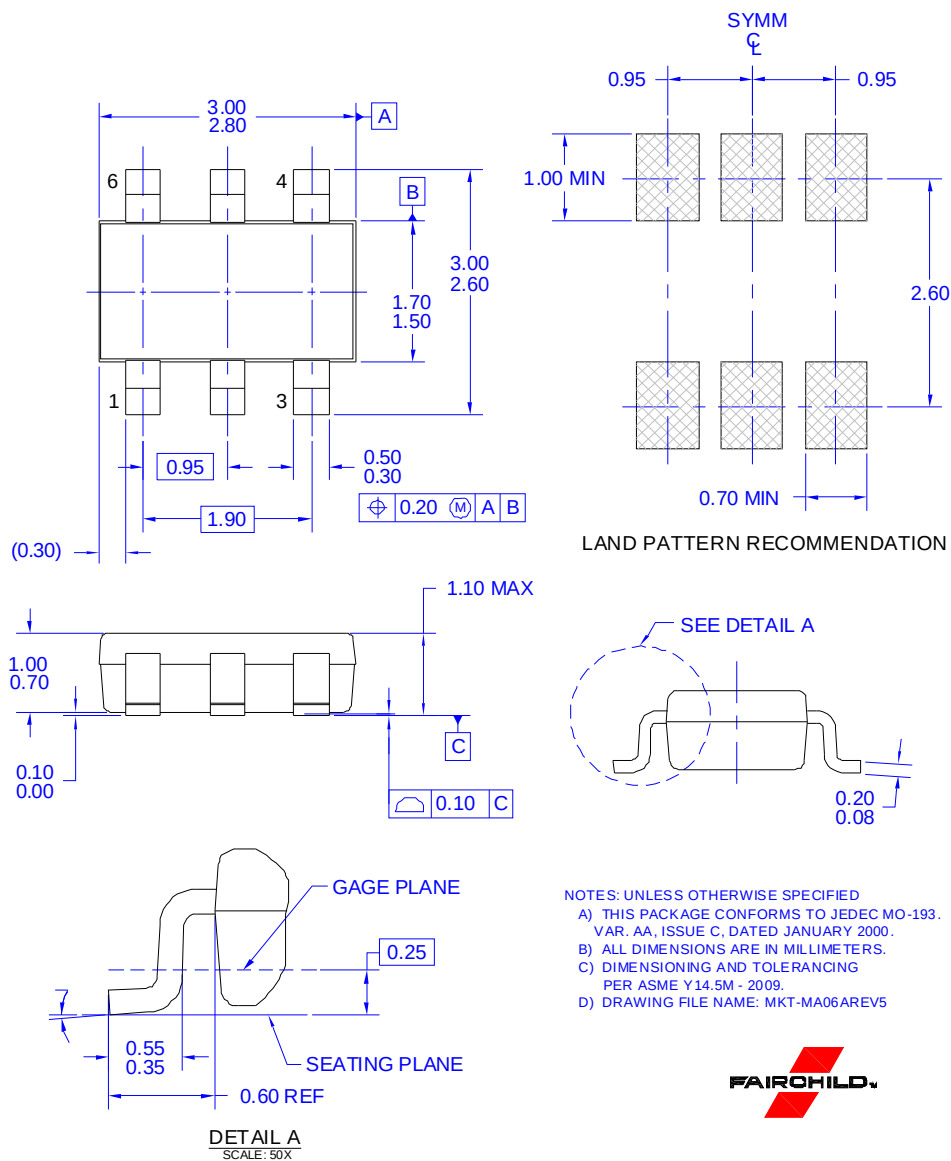


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

Dimensional Outline and Pad Layout



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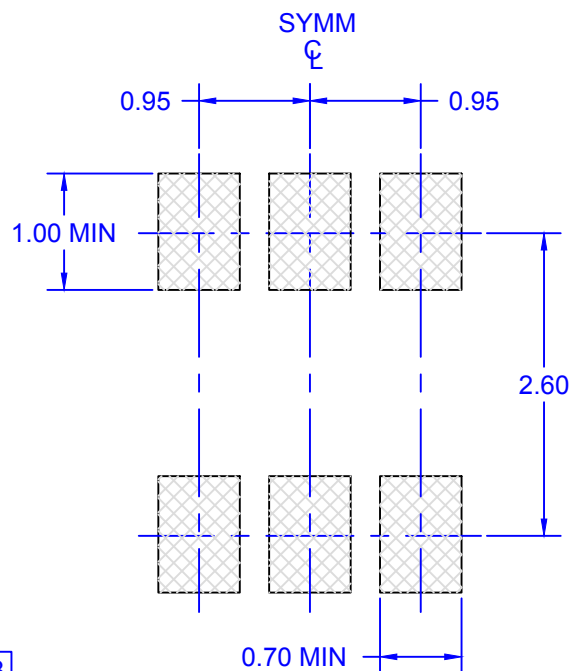
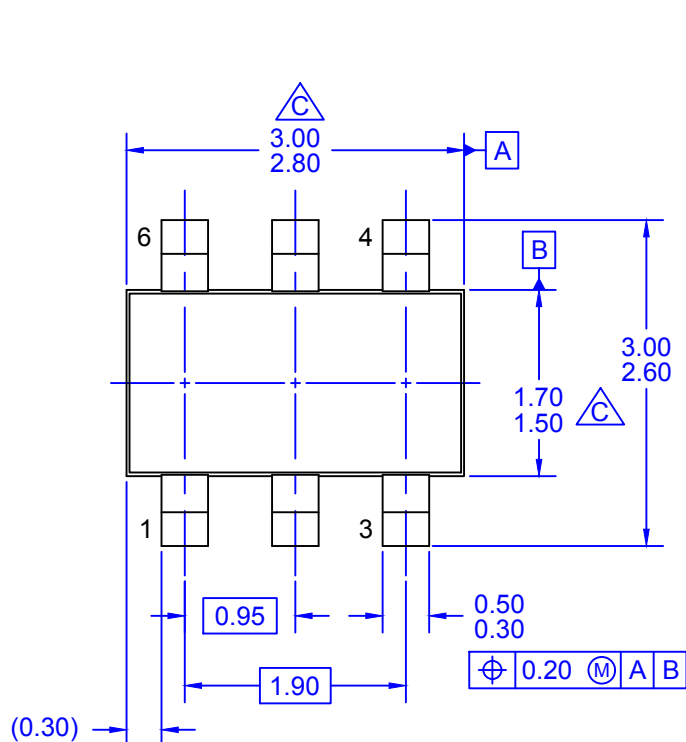
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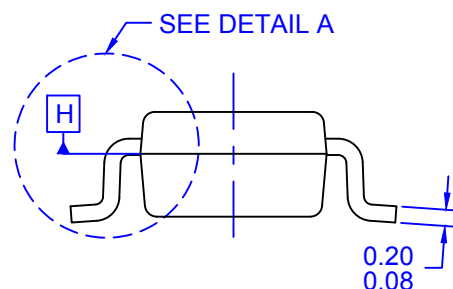
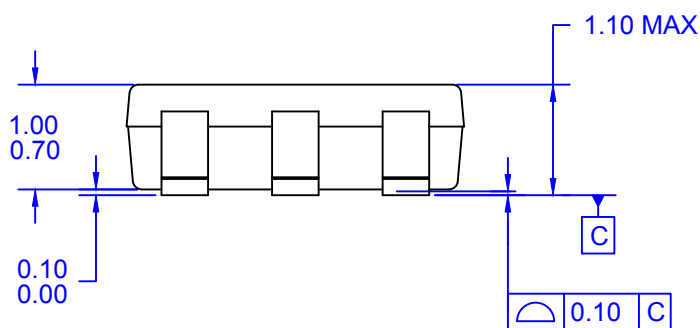
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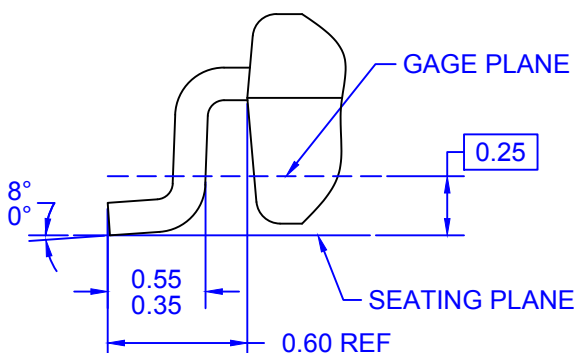
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