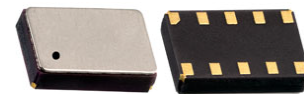


Real Time Clock Module with I²C Bus

AB-RTCMC-32.768kHz-B5ZE-S3



RoHS/RoHS II compliant



3.7 x 2.5 x 0.9 mm

Moisture Sensitivity Level: MSL=1

FEATURES:

- RTC module with built-in crystal oscillating at 32.768 kHz
- 1 MHz Fast-mode Plus (Fm+) two-wire I2C interface
- Wide Interface operating voltage: 1.6 – 5.5 V
- Wide clock operating voltage: 1.2 – 5.5 V
- Ultra low power consumption: 130 nA typ @ 3.0V / 25°C
- Provides year, month, day, weekday, hours, minutes, seconds
- Freely programmable Alarm and Timer functions with interrupt capability
- Low voltage detector, internal power on reset
- Battery backup input pin and switch-over circuit
- INT_1 can be programmed either as interrupt or clock output (open-drain)
- Programmable clock output for peripheral devices (32.768 kHz, 16.384 kHz, 8192 Hz, 4096 Hz, 1024 Hz, 32 Hz and 1 Hz)
- Programmable offset register for frequency adjustment
- I2C slave address: read D1h, write D0h
- Small and compact package size: 3.7 x 2.5 x 0.9 mm. RoHS-compliant and 100% leadfree

APPLICATIONS:

- Wide range in communication & measuring equipment
- Commercial & Industrial applications
- Automotive electronics applications
- Wireless communications
- PDA and Palm Pilots
- Credit Cards with Security Technology

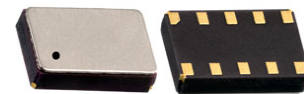
STANDARD SPECIFICATIONS:

Absolute Maximum Ratings

Parameters	Min.	Typ.	Max.	Units	Notes
Supply Voltage (V_{DD})	-0.5		+6.5	V	
Battery Supply voltage (V_{BACKUP})	-0.5		+6.5	V	
Input Voltage (V_I)	-0.5		+6.5	V	
Output Voltage (V_O)	-0.5		+6.5	V	
Supply Current (I_{DD})	-50		+50	mA	
DC Input Current (I_I)	-10		+10	mA	
DC Output Current (I_O)	-10		+10	mA	
Operating Temperature Range (T_{OPR})	-40		+85	°C	
Storage Temperature (T_{STO})	-55		+125	°C	Stored as bare product

Frequency Characteristics

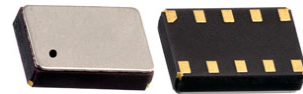
Parameters	Min.	Typ.	Max.	Units	Notes
Frequency Accuracy ($\Delta F/F$)		± 10	± 20	ppm	$T_{AMB} = +25^\circ\text{C}$; $V_{DD} = 3.0\text{V}$
Frequency vs Voltage ($\Delta F/V$)		± 0.8	± 1.5	ppm/V	$T_{AMB} = +25^\circ\text{C}$; $V_{DD} = 1.8 \sim 5.5\text{V}$
Frequency vs Temperature ($\Delta F/T_{OPR}$)	$-0.035\text{ppm}/^\circ\text{C}^2 (T_{OPR} - T_O)^2 \pm 10\%$			ppm	$T_{REF} = +25^\circ\text{C}$; $V_{DD} = 3.0\text{V}$
Turnover Temperature (T_O)	+20	+25	+30	°C	
Aging (fir st year)	-3		+3	ppm	$T_{AMB} = +25^\circ\text{C}$
Oscillator Start-up Time (T_{START})		350	500	ms	$T_{AMB} = +25^\circ\text{C}$
CLKOUT duty cycle	40	50	60	%	$T_{AMB} = +25^\circ\text{C}$



Static Characteristics

$V_{DD} = 1.2V$ to $5.5V$; $V_{SS} = 0V$; $T_{AMB} = -40^{\circ}C$ to $+85^{\circ}C$; $f_{OSC} = 32.768kHz$; unless otherwise specified

Parameters		Min.	Typ.	Max.	Units	Notes
Supply Voltage (V_{DD})	For clock data integrity I ² C bus inactive	1.2		5.5	V	
	I ² C bus active	1.6		5.5		
	Power management function active	1.8		5.5		
Slew Rate (SR)	Of V_{DD}			± 0.5	V/ms	
Battery Supply Voltage (V_{BACKUP})	Power management function active	1.8		5.5	V	
Current Consumption (I_{DD}) I ² C bus active	$f_{SCL} = 1000kHz$ $V_{DD} = 3.0V$		100	200	μA	
	$f_{SCL} = 100kHz$ $V_{DD} = 3.0V$		50	100	μA	
Current Consumption (I_{DDO}) 1)	$V_{DD} = 3.0V$		130	180	nA	I ² C bus inactive ($f_{SCL} = 0Hz$) Interrupts disabled CLKOUT disabled Power management fct. disabled (PM[2:0] = 111) $T_{amb} = +25^{\circ}C$
	$V_{DD} = 2.0V$		110	160	nA	
Current Consumption (I_{DDO}) 1)	$V_{DD} = 2.0$ to $5.0V$			500	nA	I ² C bus inactive ($f_{SCL} = 0Hz$) Interrupts disabled CLKOUT disabled Power management fct. disabled (PM[2:0] = 111) $T_{amb} = -40 \sim +85^{\circ}C$
Current Consumption (I_{DD32k}) ²⁾	V_{BACKUP} or $V_{DD} = 3.0V$		1200		nA	I ² C bus inactive ($f_{SCL} = 0Hz$) Interrupts disabled CLKOUT enabled (32.768kHz) Power management fct. enabled (PM[2:0] = 000) $T_{amb} = +25^{\circ}C$
Current Consumption (I_{DD32k}) ²⁾	V_{BACKUP} or $V_{DD} = 2.0$ to $5.0V$			3600	nA	I ² C bus inactive ($f_{SCL} = 0Hz$) Interrupts disabled CLKOUT enabled (32.768kHz) Power management fct. enabled (PM[2:0] = 000) $T_{amb} = -40 \sim +85^{\circ}C$
Battery Leakage Current ($I_{L(bat)}$)	V_{DD} active; $V_{BACKUP} = 3.0V$		50	100	nA	



(Continued)

$V_{DD} = 1.2\text{ V to } 5.5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{AMB} = -40^{\circ}\text{C to } +85^{\circ}\text{C}$; $f_{OSC} = 32.768\text{ kHz}$; unless otherwise specified

Parameters	Min.	Typ.	Max.	Units	Notes
Power Management					
Battery Switch Threshold Voltage ($V_{th(sw)bat}$)	2.28	2.5	2.7	V	
Inputs ³⁾					
LOW Level Input Voltage (V_{IL})			30% V_{DD}	V	
HIGH Level Input Voltage (V_{IH})	70% V_{DD}			V	
Input Voltage (V_I)	-0.5		$V_{DD}+0.5$	V	
Input Leakage Current(I_L)	$V_I = V_{DD} \text{ or } V_{SS}$	0		nA	
	Post ESD Event	-1	+1	μA	
Input Capacitance(C_I) ⁴⁾			7	pF	
Outputs					
Output Voltage (V_O)	On pin $\overline{\text{INT_1}}$, $\overline{\text{INT_2}}$, CLKOUT, SDA (refers to ext. pull-up voltage)	-0.5	+5.5	V	
LOW Level Output Voltage (V_{OL})		V_{SS}	0.4	V	
LOW Level Output Current (I_{OL}) ⁵⁾	Output sink current; On pin $\overline{\text{INT_1}}$, $\overline{\text{INT_2}}$, CLKOUT $V_{OL}=0.4\text{ V}$; $V_{DD}=5.0\text{ V}$	1.5		mA	
	On pin SDA $V_{OL}=0.4\text{ V}$; $V_{DD}=3.0\text{ V}$	20		mA	
Output Leakage Current (I_{LO})	$V_O = V_{DD} \text{ or } V_{SS}$	0		nA	
	Post ESD Event	-1	+1	μA	

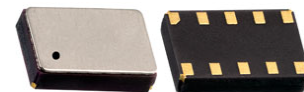
1) Timer source clock = 1/3600 Hz, level of pins SCL and SDA is V_{SS} or V_{DD} .

2) When the device is supplied via the V_{BACKUP} pin instead of the V_{DD} pin, the current values for I_{BACKUP} will be as specified for I_{DD} under the same conditions.

3) The I²C bus is 5V tolerant.

4) Implicit by design.

5) Tested on sample basis.



I²C Interface Dynamic Characteristics

Parameters	Symbol	Standard Mode		Fast Mode (FM)		Fast Mode Plus (FM+) ¹⁾		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Pin SCL								
SCL clock frequency ²⁾	f _{SCL}		100		400		1000	kHz
LOW period of SCL clock	t _{LOW}	4.7		1.3		0.5		μs
HIGH period of SCL clock	t _{HIGH}	4.0		1.6		0.26		μs
Pin SDA								
Data setup time	t _{SU,DAT}	250		100		50		ns
Data hold time	t _{HD,DAT}	0		0		0		ns
Pin SCL and SDA								
Bus free time between STOP and START condition	t _{BUF}	4.7		1.3		0.5		μs
Setup time for STOP condition	t _{SU,STO}	4.0		0.6		0.26		μs
Hold time (repeated) START condition	t _{HD,STA}	4.0		0.6		0.26		μs
Setup time for repeated START condition	t _{SU,STA}	4.7		0.6		0.26		μs
Rise time of both SDA and SCL signals ^{3) 4)}	t _r		1000	20+0.1C _b	300		120	ns
Fall time of both SDA and SCL signals ^{3) 4)}	t _f		300	20+0.1C _b	300		120	ns
Capacitive load for each bus line	C _b		400		400		550	pF
Data valid acknowledge time ⁵⁾	t _{VD,ACK}		3.45		0.9		0.45	μs
Data valid time ⁶⁾	t _{VD,DAT}		3.45		0.9		0.45	μs
Pulse width of spikes that must be suppressed by the input filter ⁷⁾	t _{SP}		50		50		50	ns

1) Fast mode plus guaranteed at 3.0 V < V_{DD} < 5.5 V.

2) The minimum SCL clock frequency is limited by the bus timeout feature, which resets the serial bus interface if either the SDA or SCL is held LOW for a minimum of 25 ms. The bus timeout feature must be disabled for DC operation.

3) A master device must internally provide a hold time of at least 300 ns for the SDA signal (refer to the V_{IL} of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.

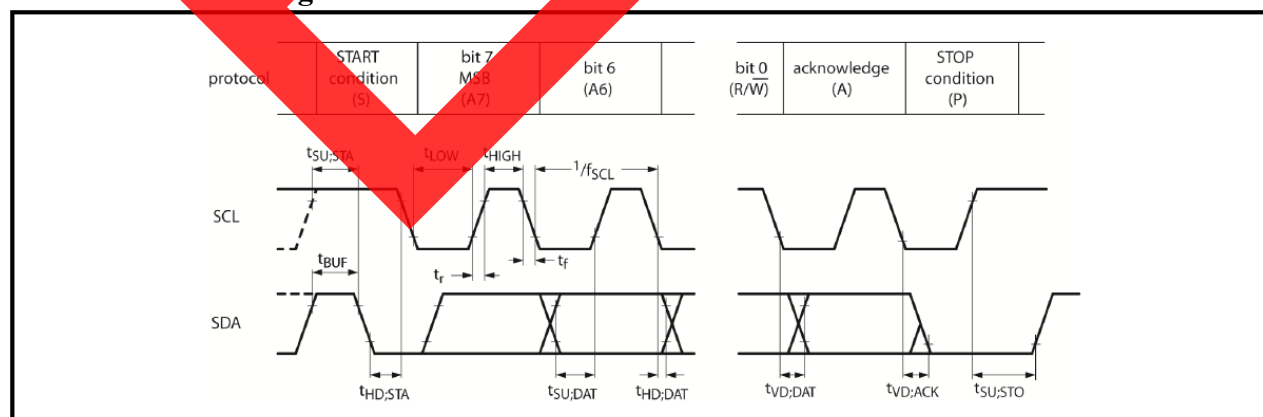
4) The maximum t_r for the SDA and SCL bus lines is 300 ns. The maximum fall time for the SDA output stage, t_f is 250 ns. This allows series protection resistors to be connected between the SDA pin, the SCL pin and the SDA/SCL bus lines without exceeding the maximum t_r

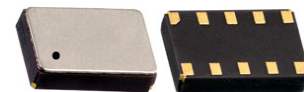
5) t_{VD;ACK} = time for acknowledgement signal from SCL LOW to SDA output LOW.

6) t_{VD;DAT} = minimum time for valid SDA output following SCL LOW.

7) Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns.

I²C Interface Timing Characteristics





PART IDENTIFICATIONS:

AB -RTCMC -32.768 kHz-B5ZE -S3-

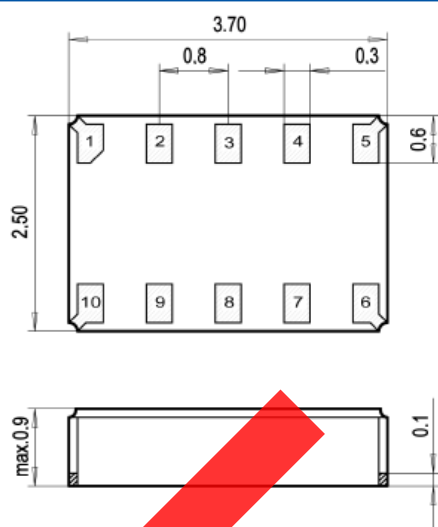


Packaging

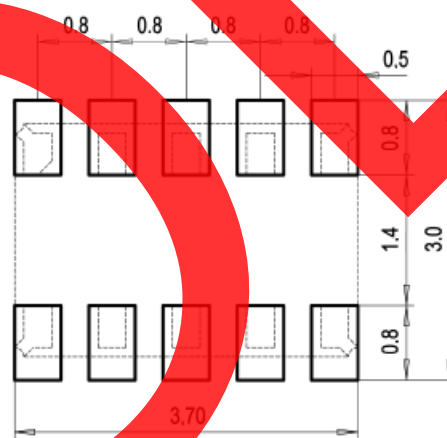
Blank: Bulk

T: 1000pcs/reel

OUTLINE DIMENSIONS:



Recommended Land Pattern

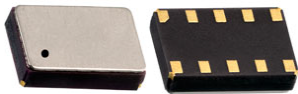


Dimensions: mm

PIN DESCRIPTIONS:

Pin No.	Pin Name	Function
1	V _{DD}	Power Supply Voltage
2	INT_1	Interrupt_1 Output pin
3	SCL	Serial Clock Input pin
4	SDA	Serial Data Input-Output pin
5	CLKOUT	Clock Output pin; open-drain; requires pull-up resistor
6	INT_2	Interrupt_2 Output pin
7	V _{SS}	Ground
8	V _{BACKUP}	Backup Supply Voltage
9	N.C.	Not Connected
10	N.C.	Not Connected

Real Time Clock Module with I²C Bus



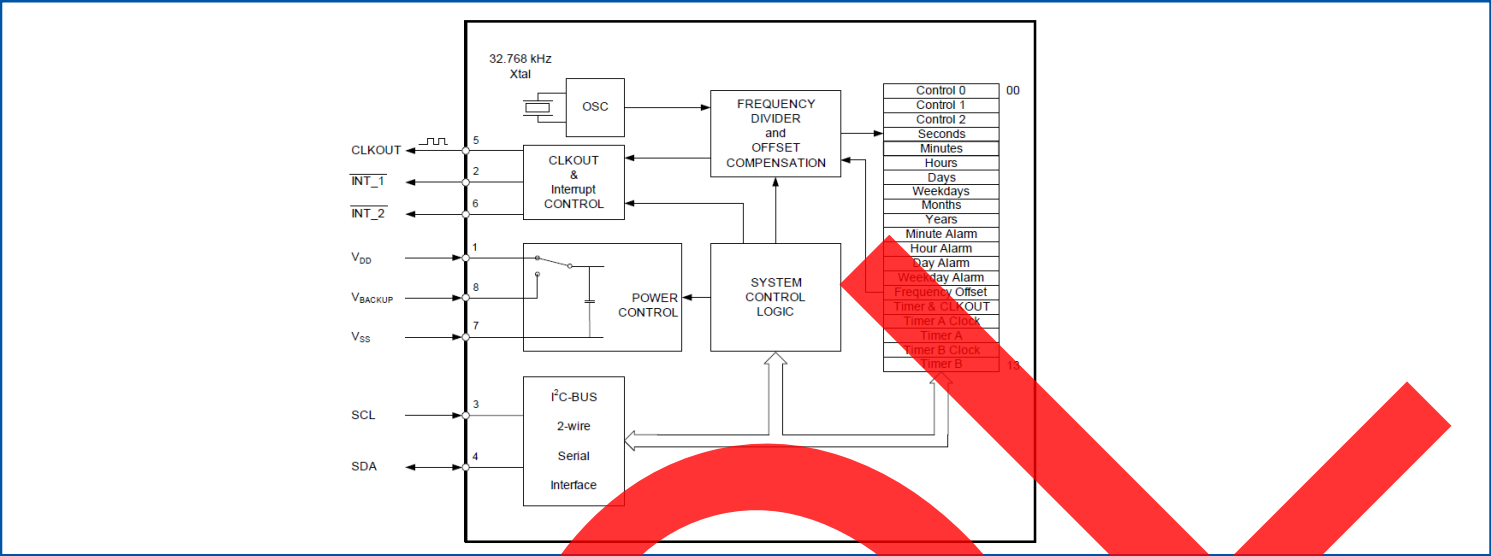
AB-RTCMC-32.768kHz-B5ZE-S3



RoHS/RoHS II compliant

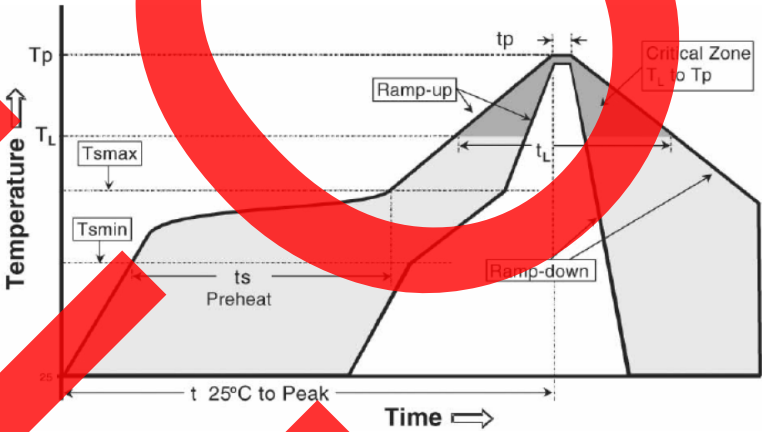
3.7 x 2.5 x 0.9 mm

BLOCK DIAGRAM:



RECOMMENDED REFLOW PROFILE:

Maximum Reflow Conditions in accordance with IPC/JEDEC J-STD-020C “Pb-free”



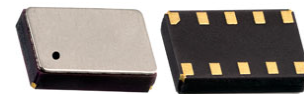
Temperature	Conditions	Units
Average Ramp-up Rate (T _{smx} to T _p)	3°C/second max	°C/s
Ramp Down Rate (T _{cool})	6°C/second max	°C/s
Time 25°C to Peak Temperature (T _{to-peak})	8 minutes max	m
Preheat		
Temperature Min (T _{smi})	150	°C
Temperature Max (T _{smx})	200	°C
Time T _{smi} to T _{smx} (ts)	60 ~ 180	sec
Time Above Liquidus		
Temperature Liquidus (T _L)	217	°C
Time above Liquidus (t _L)	60 ~ 150	sec
Peak Temperature		
Peak Temperature (T _p)	260	°C
Time within 5°C of Peak Temperature (t _p)	20 ~ 40	sec

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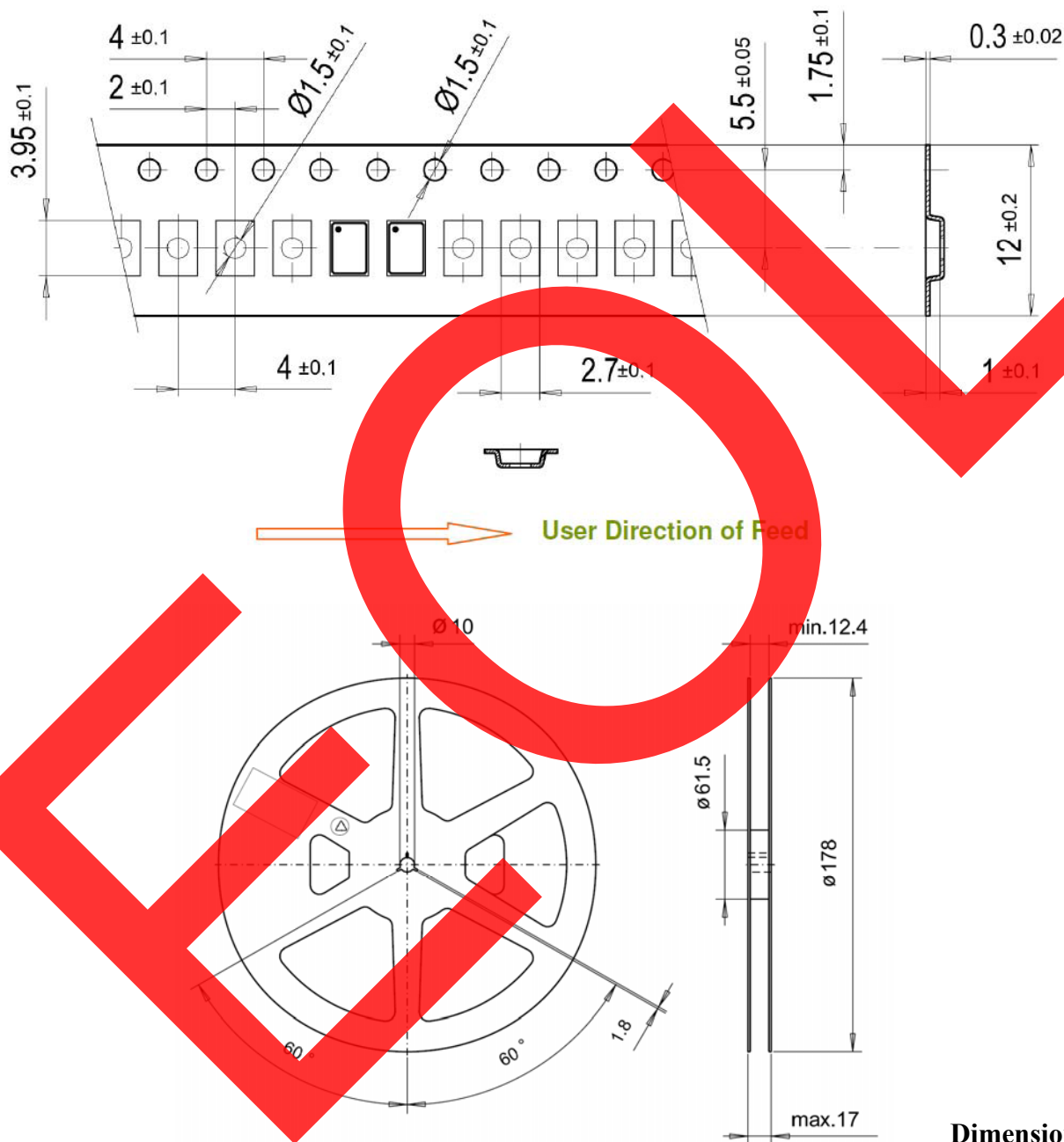
RoHS/RoHS II compliant



3.7 x 2.5 x 0.9 mm

TAPE & REEL:

T = 1000pcs/reel



Dimension: mm

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