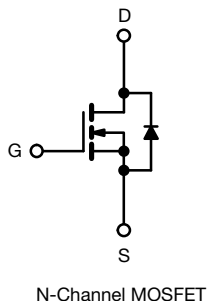
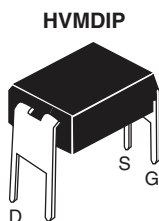


Power MOSFET



FEATURES

- Dynamic dV/dt rating
- For Automatic insertion
- End stackable
- 175 °C operating temperature
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



PRODUCT SUMMARY

V _{DS} (V)	60	
R _{DS(on)} (Ω)	V _{GS} = 10 V	0.10
Q _g (Max.) (nC)	25	
Q _{gs} (nC)	5.8	
Q _{gd} (nC)	11	
Configuration	Single	

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The 4 pin DIP package is a low cost machine-insertable case style which can be stacked in multiple combinations on standard 0.1" pin centers. The dual drain serves as a thermal link to the mounting surface for power dissipation levels up to 1 W.

ORDERING INFORMATION

Package	HVMDIP
Lead (Pb)-free	IRFD024PbF

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V _{DS}	60	V
Gate-source voltage	V _{GS}	± 20	
Continuous drain current	V _{GS} at 10 V	T _A = 25 °C	A
		T _A = 100 °C	
Pulsed drain current ^a	I _{DM}	20	
Linear derating factor		0.0083	W/°C
Single pulse avalanche energy ^b	E _{AS}	91	mJ
Maximum power dissipation	P _D	1.3	W
Peak diode recovery dV/dt ^c	dV/dt	4.5	V/ns
Operating junction and storage temperature range	T _J , T _{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) ^d	For 10 s	300	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- V_{DD} = 25 V, starting T_J = 25 °C, L = 16 mH, R_g = 25 Ω, I_{AS} = 2.5 A (see fig. 12)
- I_{SD} ≤ 17 A, dI/dt ≤ 140 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 175 °C
- 1.6 mm from case

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R _{thJA}	-	120	°C/W

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		60	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.061	-	V/°C
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V
Gate-source leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V		-	-	25	μA
		V _{DS} = 48 V, V _{GS} = 0 V, T _J = 150 °C		-	-	250	
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 1.5 A ^b	-	-	0.10	Ω
Forward transconductance	g _{fs}	V _{DS} = 25 V, I _D = 1.5 A ^b		0.90	-	-	S
Dynamic							
Input capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	640	-	pF
Output capacitance	C _{oss}			-	360	-	
Reverse transfer capacitance	C _{rss}			-	79	-	
Total gate charge	Q _g	V _{GS} = 10 V	I _D = 17 A, V _{DS} = 48 V, see fig. 6 and 13 ^b	-	-	25	nC
Gate-source charge	Q _{gs}			-	-	5.8	
Gate-drain charge	Q _{gd}			-	-	11	
Turn-on delay time	t _{d(on)}	V _{DD} = 30 V, I _D = 17 A, R _g = 18 Ω, R _D = 1.7Ω, see fig. 1 0 ^b		-	13	-	ns
Rise time	t _r			-	58	-	
Turn-off delay time	t _{d(off)}			-	25	-	
Fall time	t _f			-	42	-	
Internal drain inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.0	-	nH
Internal source inductance	L _S			-	6.0	-	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	2.5	A
Pulsed diode forward current ^a	I _{SM}			-	-	20	
Body diode voltage	V _{SD}	T _J = 25 °C, I _S = 2.5 A, V _{GS} = 0 V ^b		-	-	1.5	V
Body diode reverse recovery time	t _{rr}	T _J = 25 °C, I _F = 17 A, dI/dt = 100 A/μs ^b		-	80	180	ns
Body diode reverse recovery charge	Q _{rr}			-	0.29	0.64	μC
Forward turn-on time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$

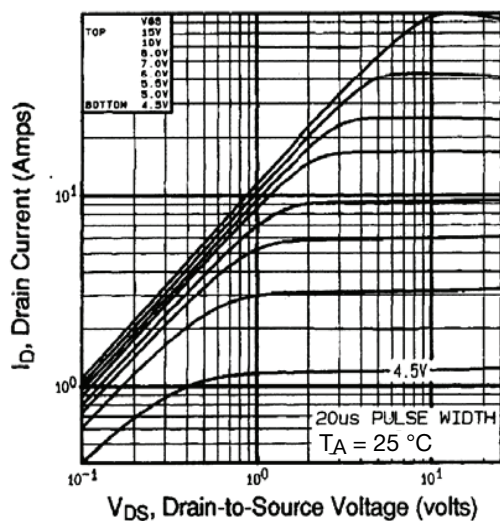
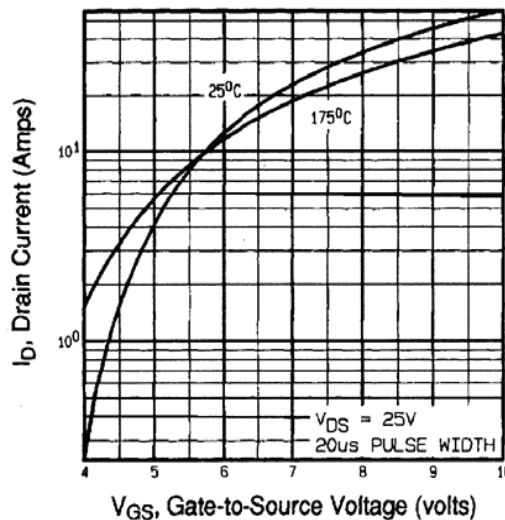
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics, $T_A = 25\text{ }^{\circ}\text{C}$


Fig. 2 - Typical Transfer Characteristics

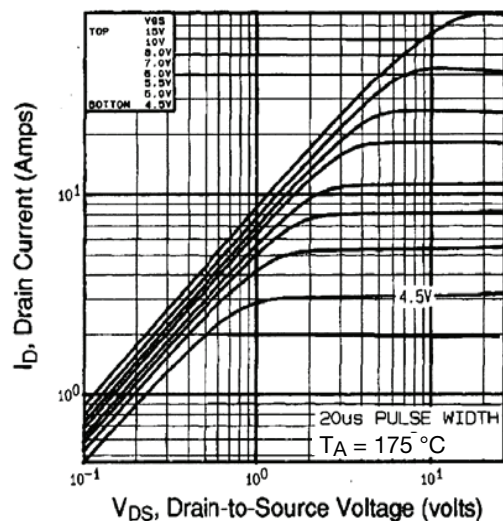
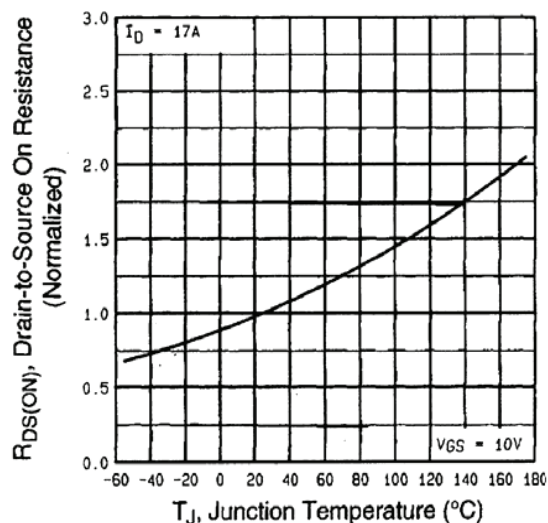
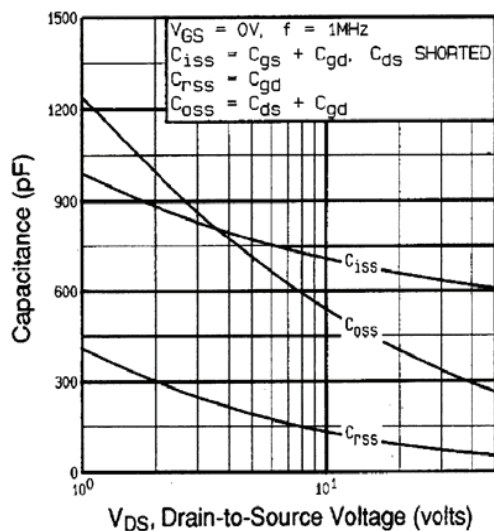
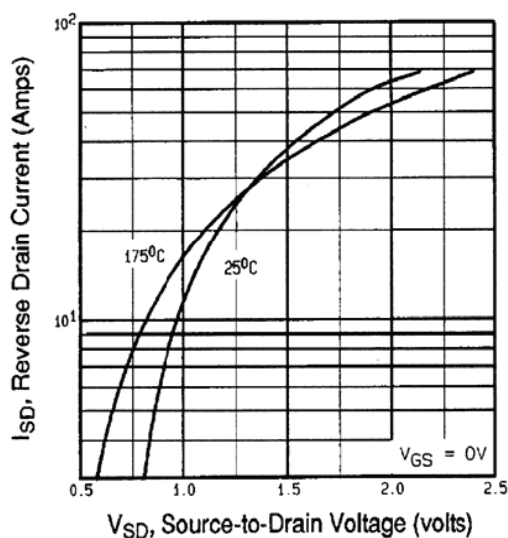
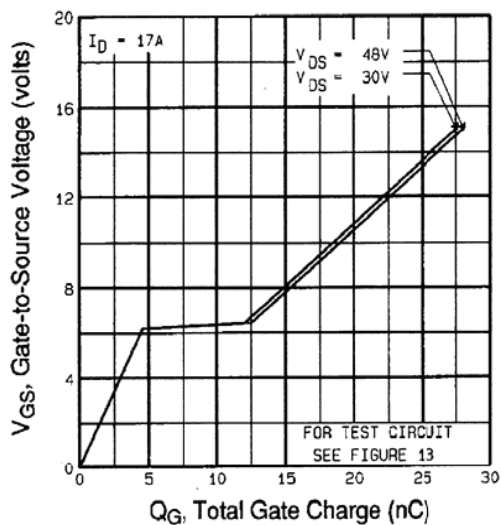
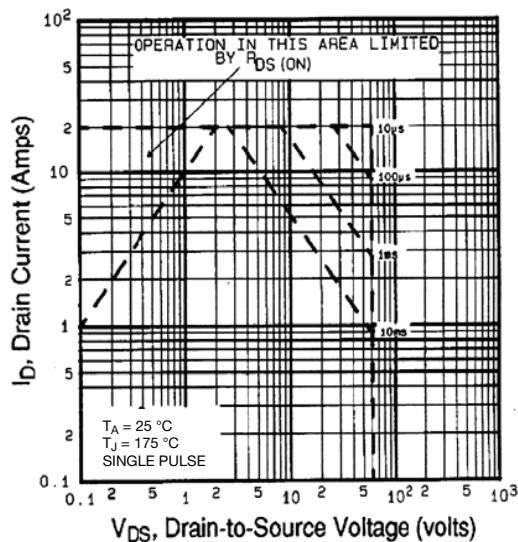
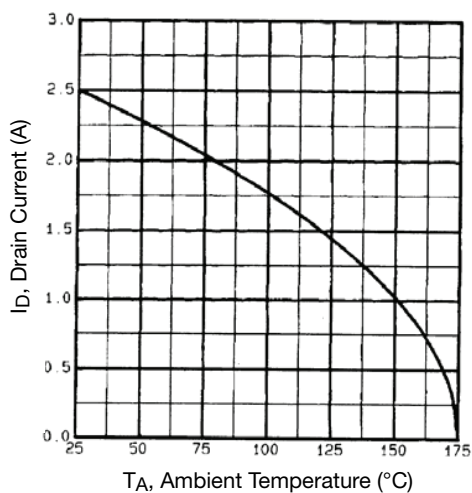
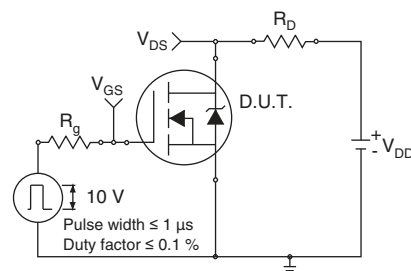
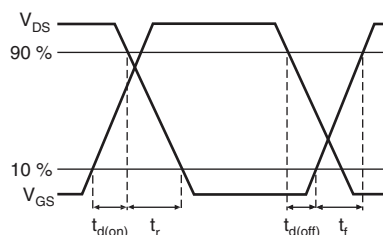
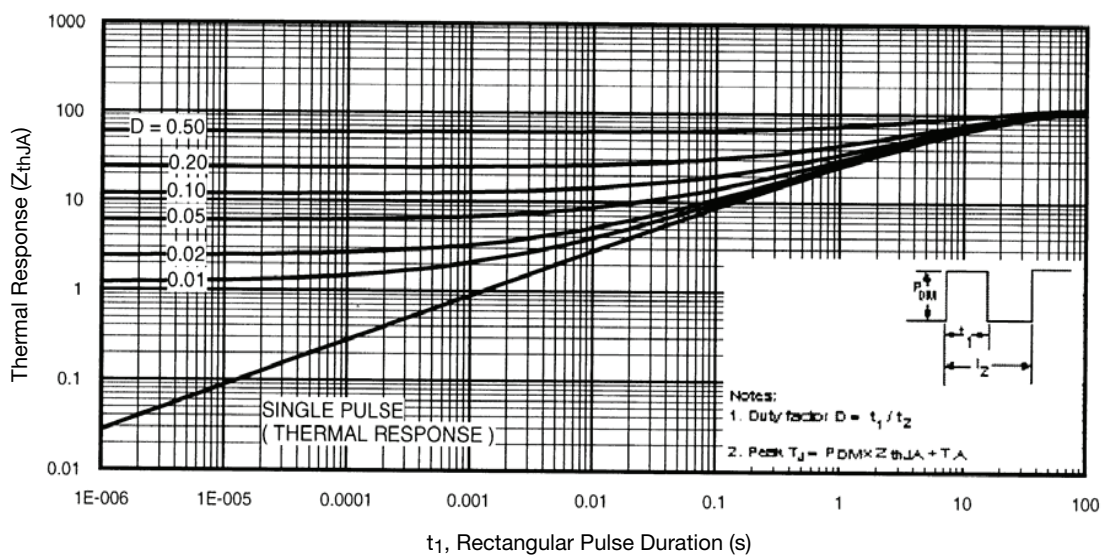
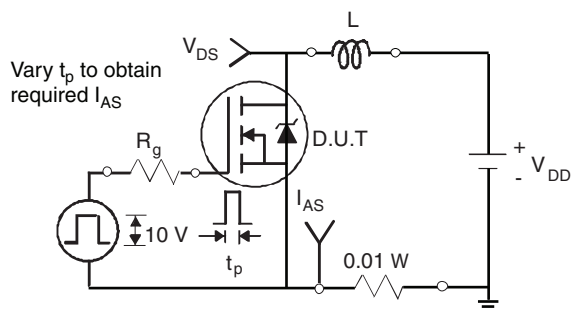
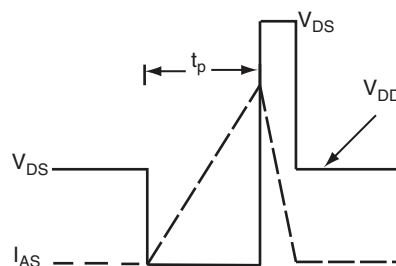
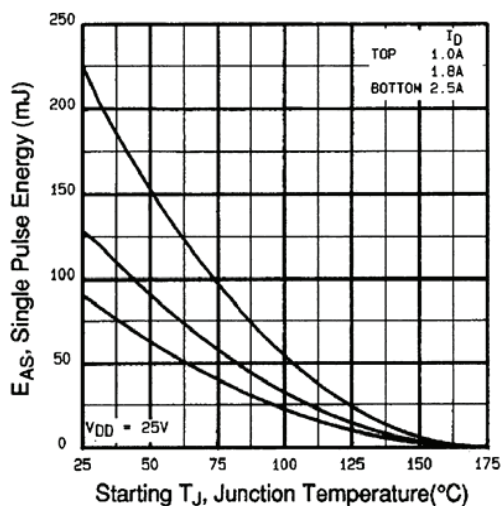
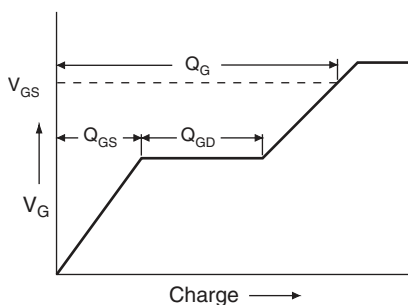
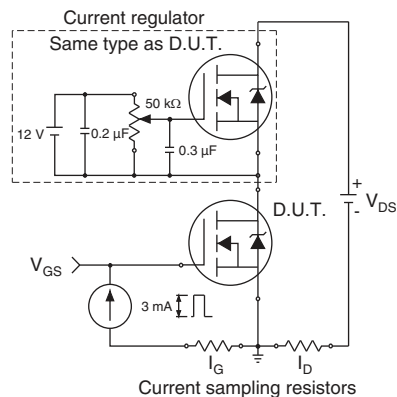
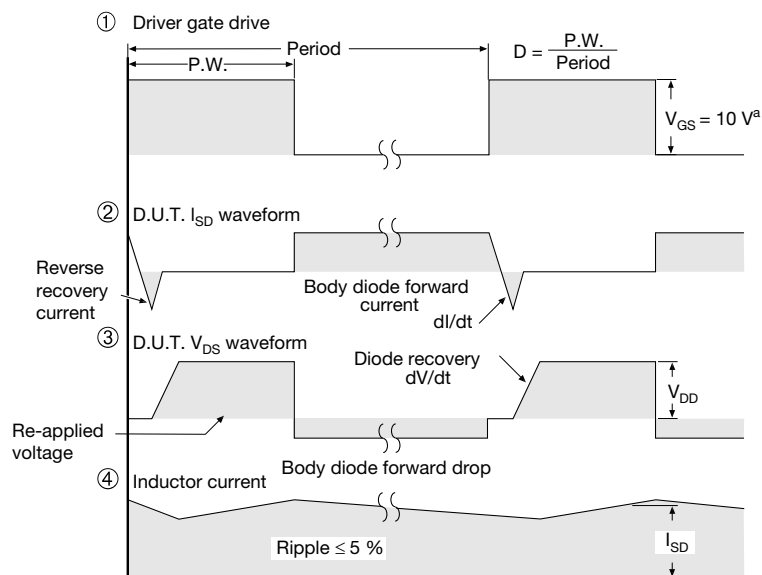
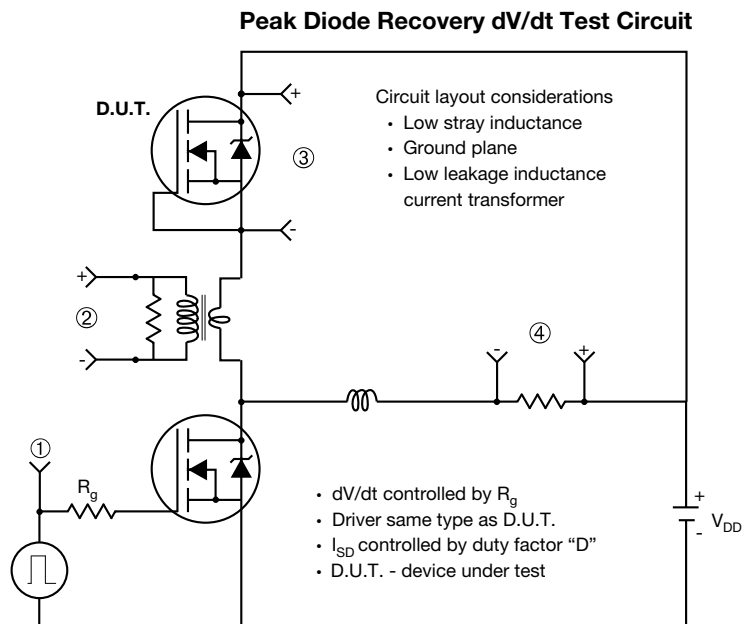

Fig. 1 - Typical Output Characteristics, $T_A = 175\text{ }^{\circ}\text{C}$


Fig. 3 - Normalized On-Resistance vs. Temperature


Fig. 4 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 6 - Typical Source-Drain Diode Forward Voltage

Fig. 5 - Typical Gate Charge vs. Gate-to-Source Voltage

Fig. 2 - Maximum Safe Operating Area


Fig. 7 - Maximum Drain Current vs. Ambient Temperature

Fig. 10a - Switching Time Test Circuit

Fig. 10b - Switching Time Waveforms

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Ambient


Fig. 12a - Unclamped Inductive Test Circuit

Fig. 12b - Unclamped Inductive Waveforms

Fig. 12c - Maximum Avalanche Energy vs. Drain Current

Fig. 13a - Basic Gate Charge Waveform

Fig. 13b - Gate Charge Test Circuit



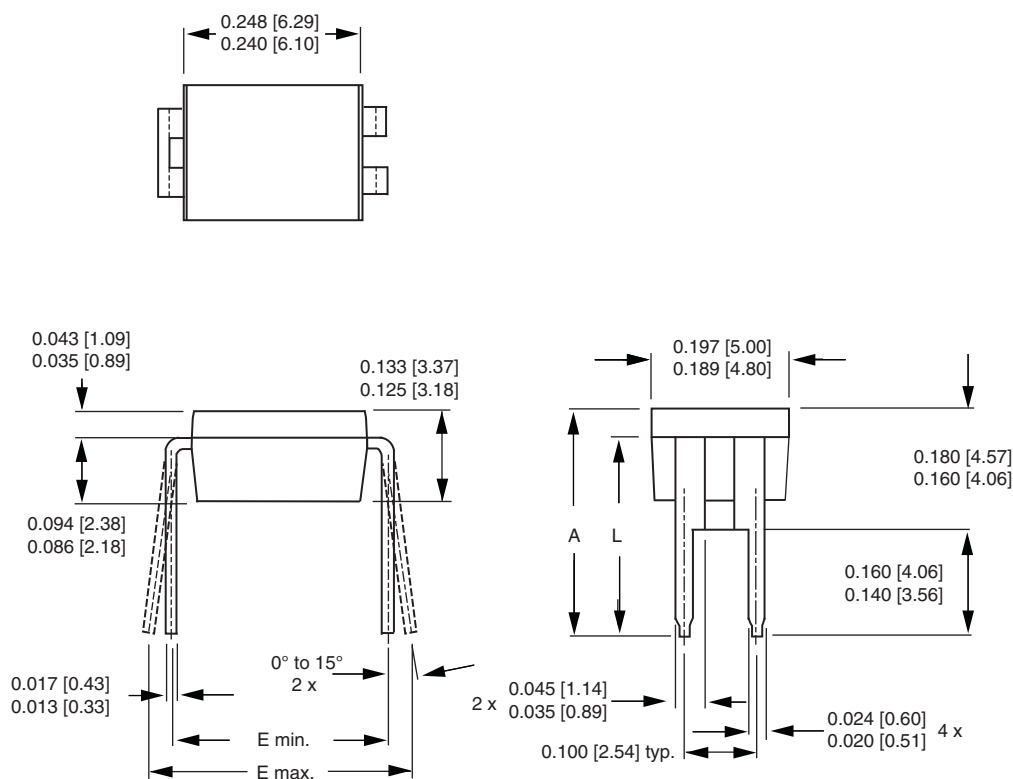
Note

a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel

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HVM DIP (High voltage)



DIM.	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.310	0.330	7.87	8.38
E	0.300	0.425	7.62	10.79
L	0.270	0.290	6.86	7.36

ECN: X10-0386-Rev. B, 06-Sep-10
DWG: 5974

Note

- Package length does not include mold flash, protrusions or gate burrs. Package width does not include interlead flash or protrusions.



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