

MOSFET – P-Channel, QFET®

-150 V, -36 A, 90 mΩ

FQA36P15

Description

This P-Channel enhancement mode power MOSFET is produced using onsemi's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

Features

- -36 A, -150 V, $R_{DS(on)} = 90 \text{ m}\Omega$ (Max.) @ $V_{GS} = -10 \text{ V}$, $I_D = -18 \text{ A}$
- Low Gate Charge (Typ. 81 nC)
- Low C_{RSS} (Typ. 110 pF)
- 100% Avalanche Tested
- 175 °C Maximum Junction Temperature Rating
- This Device is Pb-Free and is RoHS Compliant

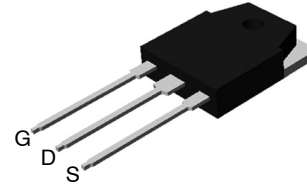
ABSOLUTE MAXIMUM RATINGS ($T_C = 25 \text{ }^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain-Source Voltage	-150	V
I_D	Drain Current – Continuous ($T_C = 25 \text{ }^\circ\text{C}$) – Continuous ($T_C = 100 \text{ }^\circ\text{C}$)	-36 -25.5	A
I_{DM}	Drain Current – Pulsed (Note 1)	-144	A
V_{GSS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	1400	mJ
I_{AR}	Avalanche Current (Note 1)	-36	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	29.4	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	-5.0	V/ns
P_D	Power Dissipation ($T_C = 25 \text{ }^\circ\text{C}$) – Derate Above 25 °C	294 1.96	W W/°C
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +175	°C
T_L	Maximum Lead Temperature for Soldering Purposes, 1/8" from Case for 5 seconds	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

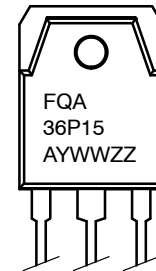
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. $L = 1.45 \text{ mH}$, $I_{AS} = -36 \text{ A}$, $V_{DD} = -50 \text{ V}$, $R_G = 25 \text{ }\Omega$, Starting $T_J = 25 \text{ }^\circ\text{C}$.
3. $I_{SD} \leq 36 \text{ A}$, $di/dt \leq 300 \text{ A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25 \text{ }^\circ\text{C}$.

V_{DSS}	$R_{DS(on)} \text{ MAX}$	$I_D \text{ MAX}$
-150 V	90 mΩ @ -10 V	-36 A



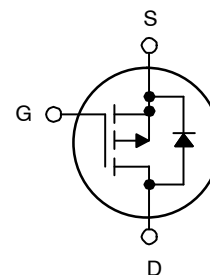
TO-3P-3LD / EIAJ SC-65, ISOLATED CASE 340BZ

MARKING DIAGRAM



FQA36P15 = Specific Device Code
A = Assembly Location
YWW = Date Code (Year & Week)
ZZ = Assembly Lot

P-CHANNEL MOSFET



ORDERING INFORMATION

Part Number	Package	Shipping
FQA36P15	TO-3P-3LD (Pb-Free)	450 Units / Tube

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.51	°C/W
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink, Typ.	0.24	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	40	°C/W

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-150	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$, Referenced to 25°C	-	-0.13	-	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -150\text{ V}, V_{GS} = 0\text{ V}$	-	-	-10	μA
		$V_{DS} = -120\text{ V}, T_C = 150^\circ\text{C}$	-	-	-100	
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = -25\text{ V}, V_{DS} = 0\text{ V}$	-	-	-100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = 25\text{ V}, V_{DS} = 0\text{ V}$	-	-	100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-2.0	-	-4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10\text{ V}, I_D = -18\text{ A}$	-	0.076	0.09	Ω
g_{FS}	Forward Transconductance	$V_{DS} = -40\text{ V}, I_D = -18\text{ A}$	-	19.5	-	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = -25\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	2550	3320	pF
C_{oss}	Output Capacitance		-	710	920	pF
C_{rss}	Reverse Transfer Capacitance		-	110	140	pF

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -75\text{ V}, I_D = -36\text{ A}, R_G = 25\text{ }\Omega$ (Note 4)	-	50	110	ns
t_r	Turn-On Rise Time		-	350	710	ns
$t_{d(off)}$	Turn-Off Delay Time		-	155	320	ns
t_f	Turn-Off Fall Time		-	150	310	ns
Q_g	Total Gate Charge	$V_{DS} = -120\text{ V}, I_D = -36\text{ A}, V_{GS} = -10\text{ V}$ (Note 4)	-	81	105	nC
Q_{gs}	Gate-Source Charge		-	19	-	nC
Q_{gd}	Gate-Drain Charge		-	42	-	nC

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I _S	Maximum Continuous Drain-Source Diode Forward Current		–	–	–36	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		–	–	–144	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = –36 A	–	–	–4.0	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = –36 A, dI _F /dt = 100 A/μs	–	198	–	ns
Q _{rr}	Reverse Recovery Charge		–	1.45	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.



TYPICAL PERFORMANCE CHARACTERISTICS

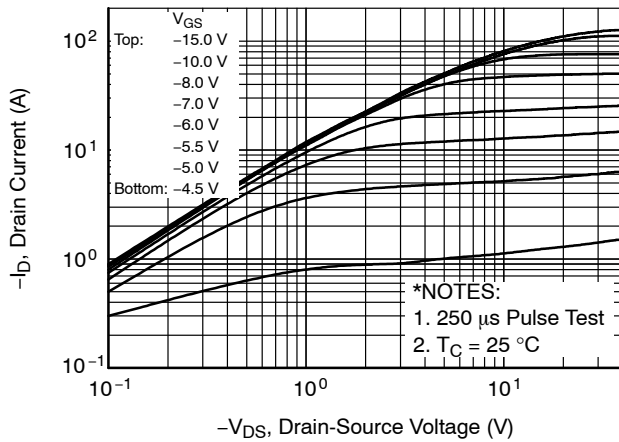


Figure 1. On-Region Characteristics

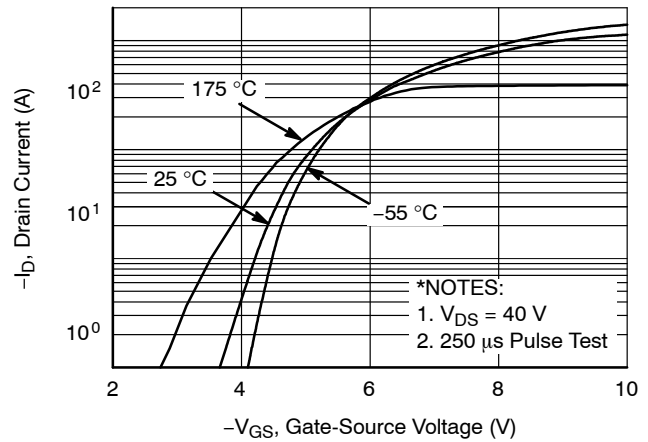


Figure 2. Transfer Characteristics

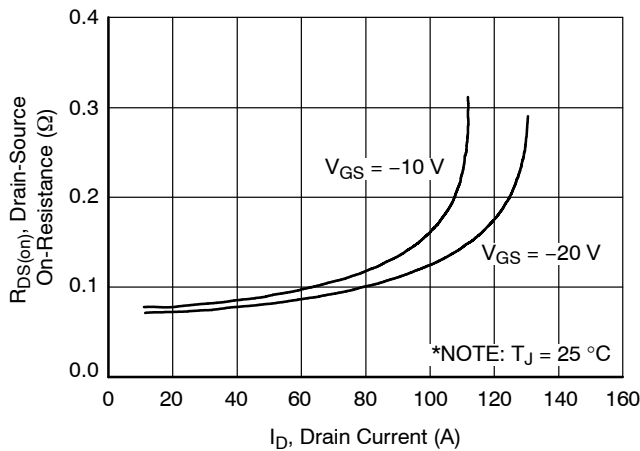


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

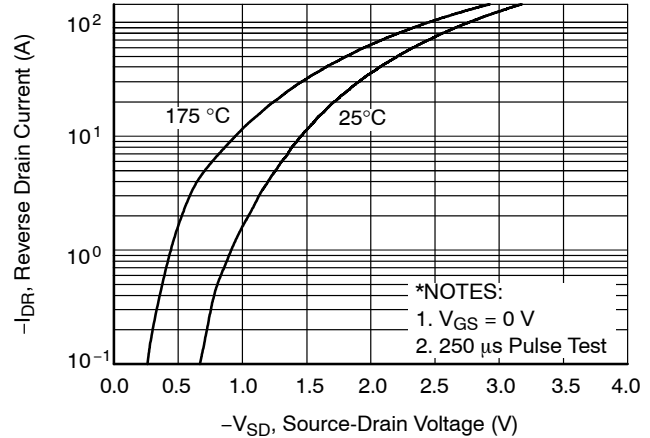


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

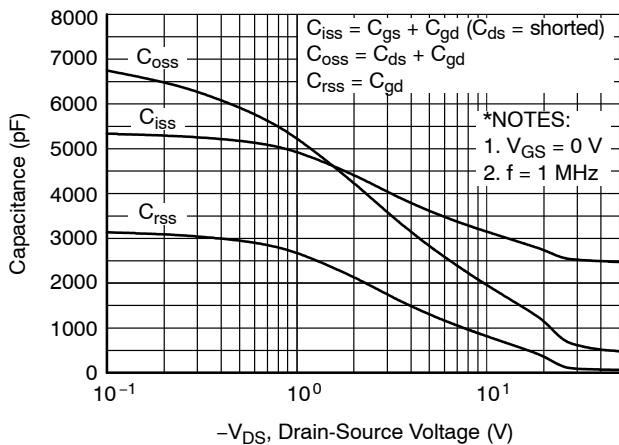


Figure 5. Capacitance Characteristics

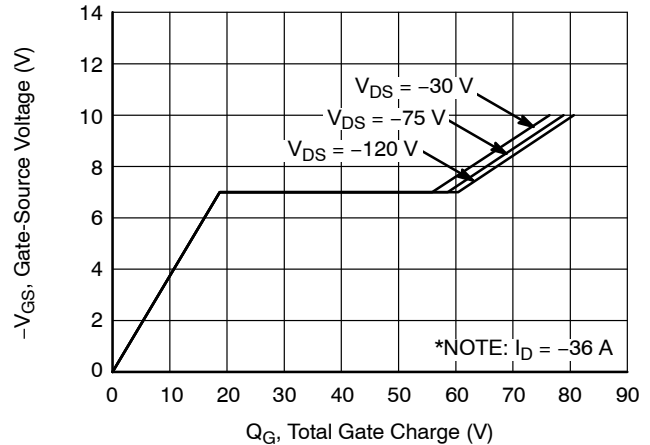


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

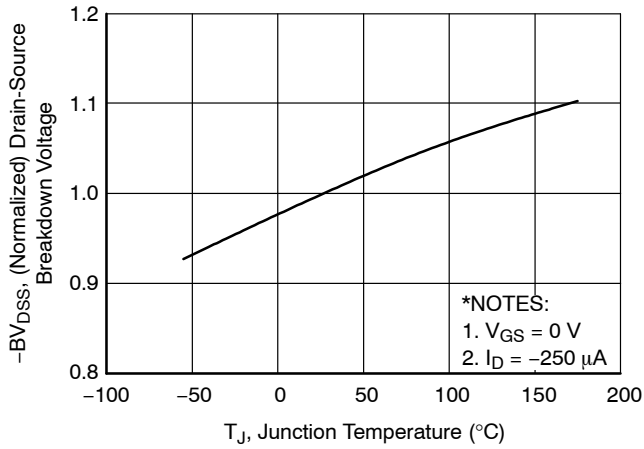


Figure 7. Breakdown Voltage Variation vs. Temperature

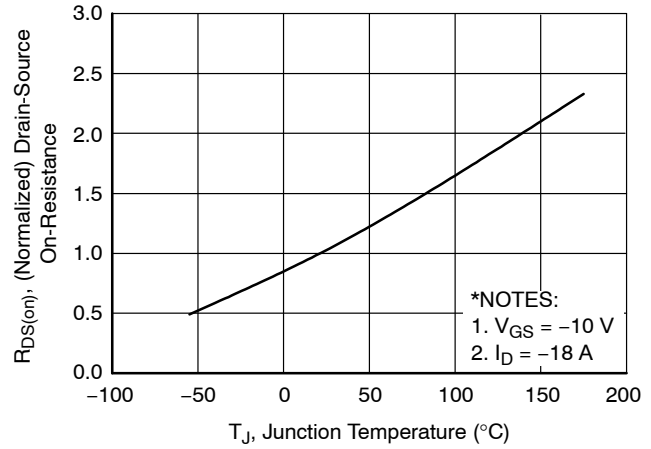


Figure 8. On-Resistance Variation vs. Temperature

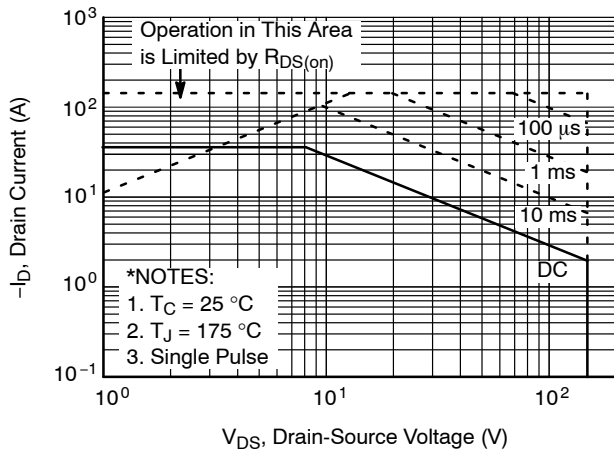


Figure 9. Safe Operating Area

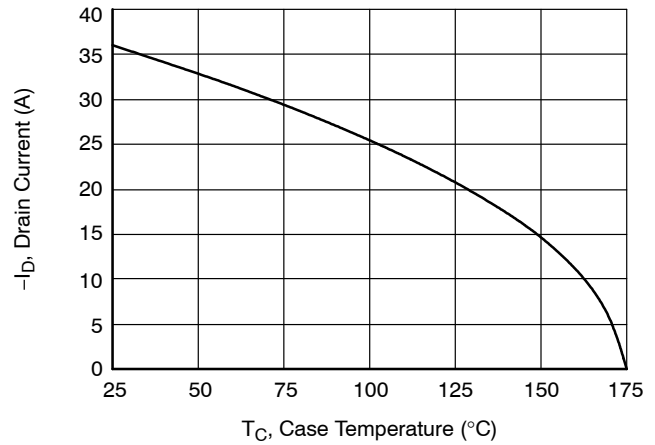


Figure 10. Maximum Drain Current vs. Case Temperature

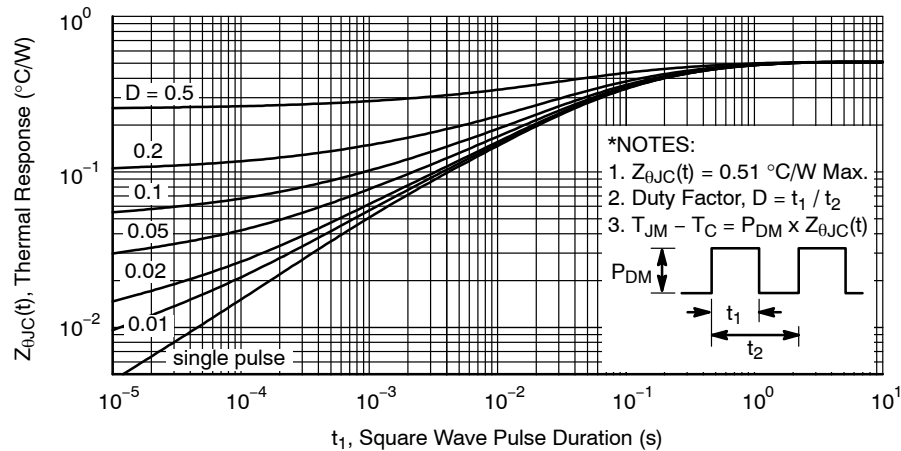
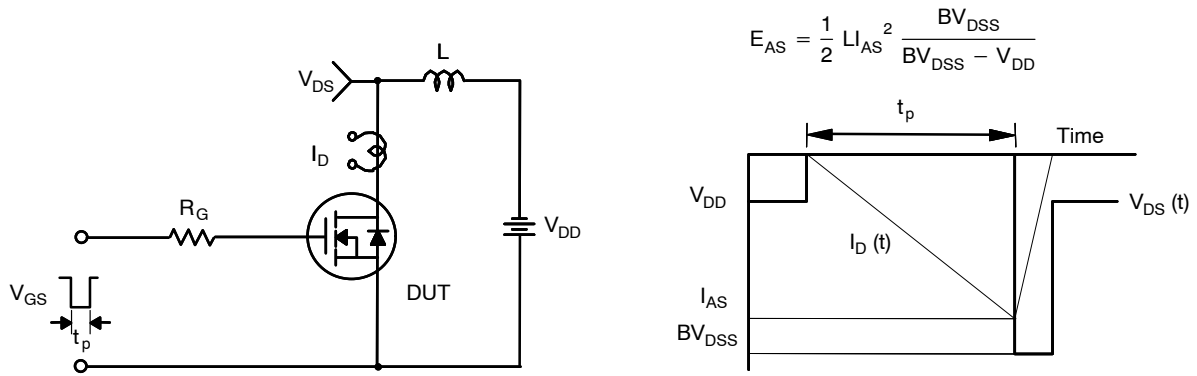
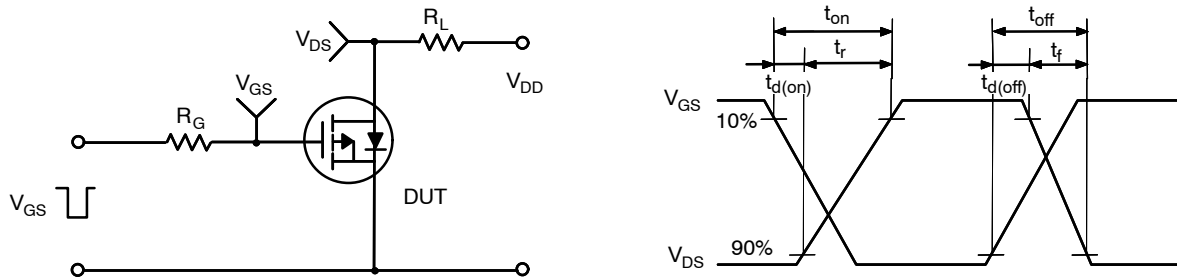
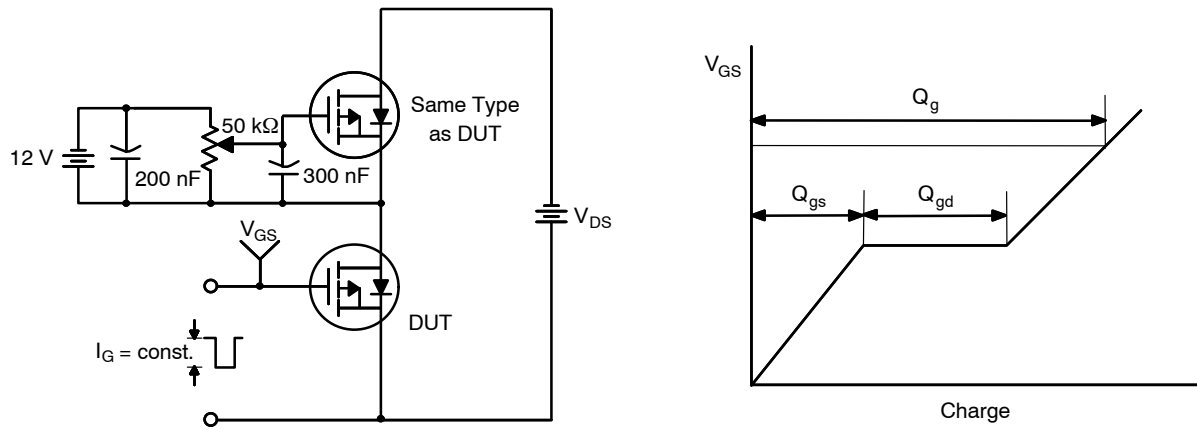


Figure 11. Transient Thermal Response Curve



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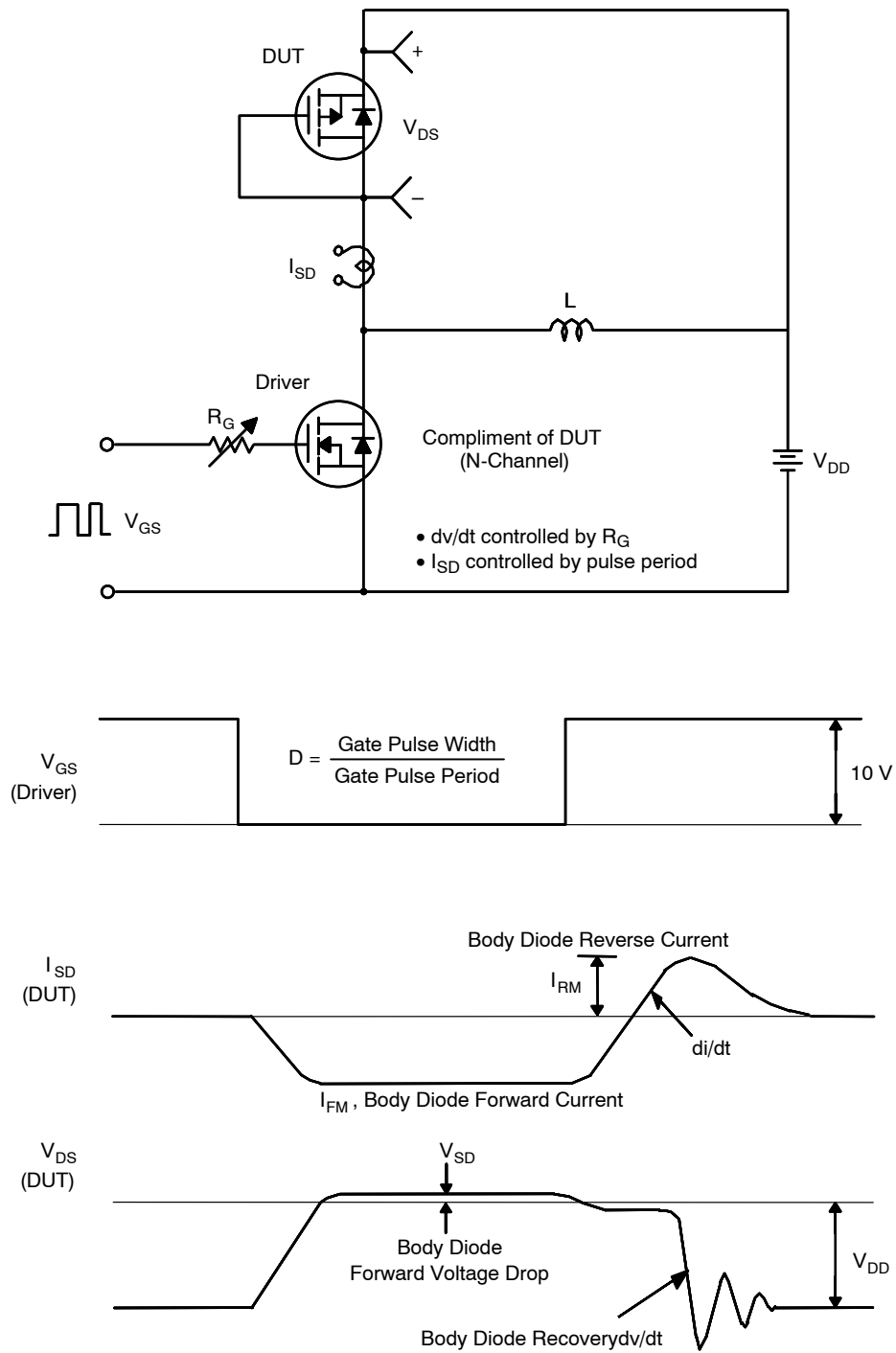


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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REVISION HISTORY

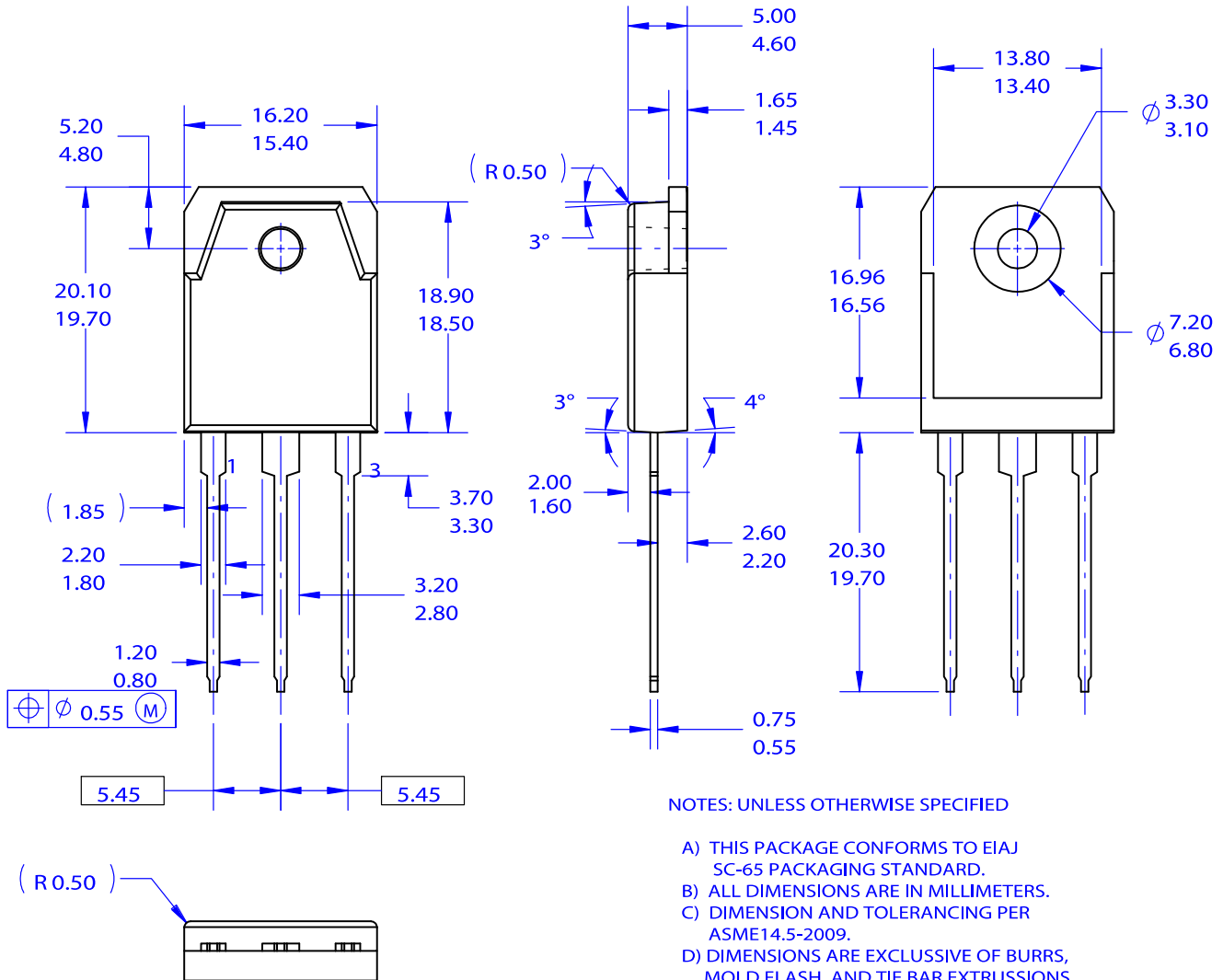
Revision	Description of Changes	Date
4	Converted the Data Sheet to onsemi format.	5/14/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.



TO-3P-3LD / EIAJ SC-65, ISOLATED
CASE 340BZ
ISSUE O

DATE 31 OCT 2016



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO EIAJ SC-65 PACKAGING STANDARD.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSION AND TOLERANCING PER ASME14.5-2009.
- D) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

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