

MOSFET – Single P-Channel, Small Signal, SOT-1123, 1.0 x 0.6 mm -20 V, -200 mA

NTNUS3171PZ

Features

- Single P-Channel MOSFET
- Offers a Low $R_{DS(on)}$ Solution in the Ultra Small 1.0 x 0.6 mm Package
- 1.5 V Gate Voltage Rating
- Ultra Thin Profile (< 0.5 mm) Allows It to Fit Easily into Extremely Thin Environments such as Portable Electronics.
- This is a Pb-Free Device

Applications

- High Side Switch
- High Speed Interfacing
- Optimized for Power Management in Ultra Portable Equipment

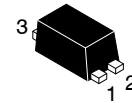
MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	-20	V
Gate-to-Source Voltage			V_{GS}	± 8	V
Continuous Drain Current (Note 1)	Steady State	$T_{\text{A}} = 25^{\circ}\text{C}$	I_{D}	-150	mA
		$T_{\text{A}} = 85^{\circ}\text{C}$		-110	
	$t \leq 5 \text{ s}$	$T_{\text{A}} = 25^{\circ}\text{C}$		-200	
Power Dissipation (Note 1)	Steady State	$T_{\text{A}} = 25^{\circ}\text{C}$	P_{D}	-125	mW
				$t \leq 5 \text{ s}$	
Pulsed Drain Current		$t_{\text{p}} = 10 \mu\text{s}$	I_{DM}	-600	mA
Operating Junction and Storage Temperature			$T_{\text{J}}, T_{\text{STG}}$	-55 to 150	$^{\circ}\text{C}$
Source Current (Body Diode) (Note 2)			I_{S}	-200	mA
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_{L}	260	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

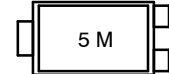
1. Surface-mounted on FR4 board using the minimum recommended pad size, or 2 mm², 1 oz Cu.
2. Pulse Test: pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$

$V_{(BR)DS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ Max}$
-20 V	3.5 Ω @ -4.5 V	-0.20 A
	4.0 Ω @ -2.5 V	
	5.5 Ω @ -1.8 V	
	7.0 Ω @ -1.5 V	



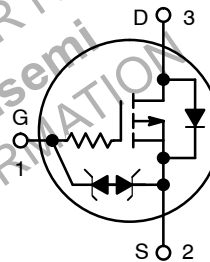
SOT-1123
CASE 524AA

MARKING DIAGRAM



5 = Specific Device Code
(Rotated 90° Clockwise)
M = Date Code

P-Channel MOSFET



ORDERING INFORMATION

Device	Package	Shipping [†]
NTNUS3171PZT5G	SOT-1123 (Pb-Free)	8000/Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	1000	$^{\circ}\text{C/W}$
Junction-to-Ambient – $t = 5\text{ s}$ (Note 3)	$R_{\theta JA}$	600	

3. Surface-mounted on FR4 board using the minimum recommended pad size, or 2 mm², 1 oz Cu.

ELECTRICAL CHARACTERISTICS ($T_J = 25^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-20			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = -5.0\text{ V}, T_J = 25^{\circ}\text{C}$			-50	nA
		$V_{GS} = 0\text{ V}, V_{DS} = -5.0\text{ V}, T_J = 85^{\circ}\text{C}$			-100	
		$V_{GS} = 0\text{ V}, V_{DS} = -16\text{ V}, T_J = 25^{\circ}\text{C}$			-200	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 5.0\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = -250\text{ }\mu\text{A}$	-0.4	-0.7	-1.0	V
Drain-to-Source On Resistance	$R_{DS(ON)}$	$V_{GS} = -4.5\text{ V}, I_D = -100\text{ mA}$		2.0	3.5	Ω
		$V_{GS} = -2.5\text{ V}, I_D = -50\text{ mA}$		2.6	4.0	
		$V_{GS} = -1.8\text{ V}, I_D = -20\text{ mA}$		3.4	5.5	
		$V_{GS} = -1.5\text{ V}, I_D = -10\text{ mA}$		4.0	7.0	
		$V_{GS} = -1.2\text{ V}, I_D = -1.0\text{ mA}$		6.0		
Forward Transconductance	g_{FS}	$V_{DS} = -5.0\text{ V}, I_D = -125\text{ mA}$		0.26		S
Source-Drain Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = -200\text{ mA}$	-0.5		-1.4	V

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C_{ISS}	$f = 1\text{ MHz}, V_{GS} = 0\text{ V}, V_{DS} = -15\text{ V}$		13		pF
Output Capacitance	C_{OSS}			3.4		
Reverse Transfer Capacitance	C_{RSS}			1.6		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}; I_D = 200\text{ mA}$		0.7		nC
Threshold Gate Charge	$Q_{G(TH)}$			0.1		
Gate-to-Source Charge	Q_{GS}			0.2		
Gate-to-Drain Charge	Q_{GD}			0.1		

SWITCHING CHARACTERISTICS, $V_{GS} = 4.5\text{ V}$ (Note 4)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -4.5\text{ V}, V_{DD} = -15\text{ V}, I_D = -200\text{ mA}, R_G = 2.0\text{ }\Omega$		30		ns
Rise Time	t_r			56		
Turn-Off Delay Time	$t_{d(OFF)}$			196		
Fall Time	t_f			145		

4. Switching characteristics are independent of operating junction temperatures

TYPICAL CHARACTERISTICS

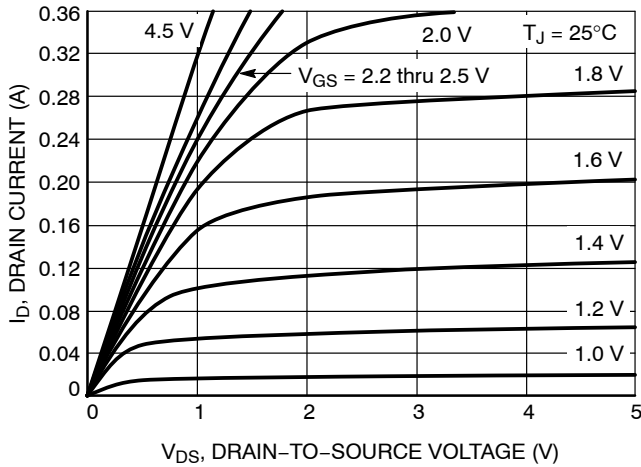


Figure 1. On-Region Characteristics

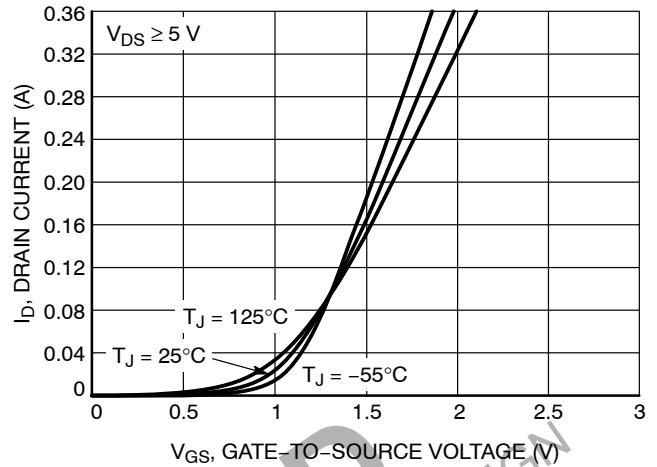


Figure 2. Transfer Characteristics

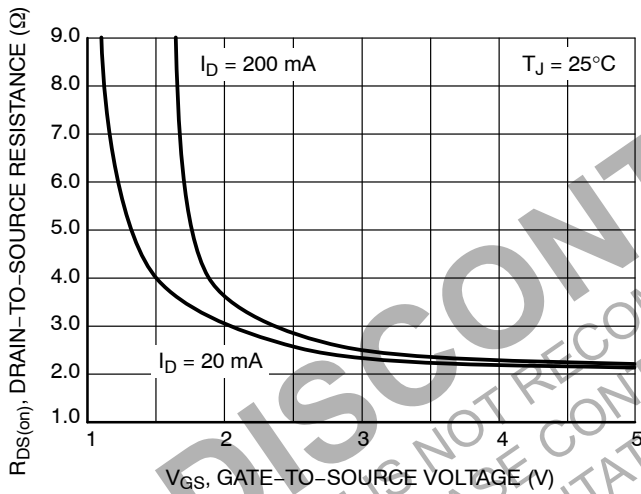


Figure 3. On-Resistance vs. Gate Voltage

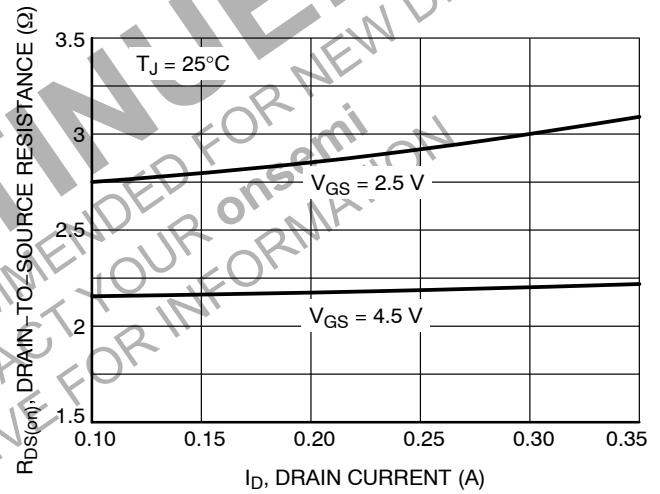


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

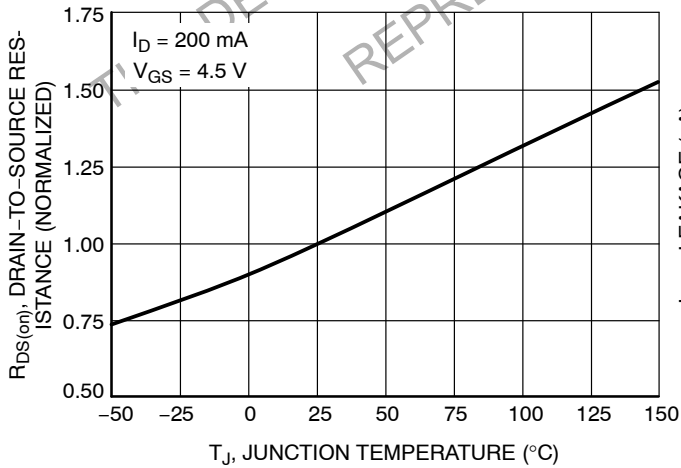


Figure 5. On-Resistance Variation with Temperature

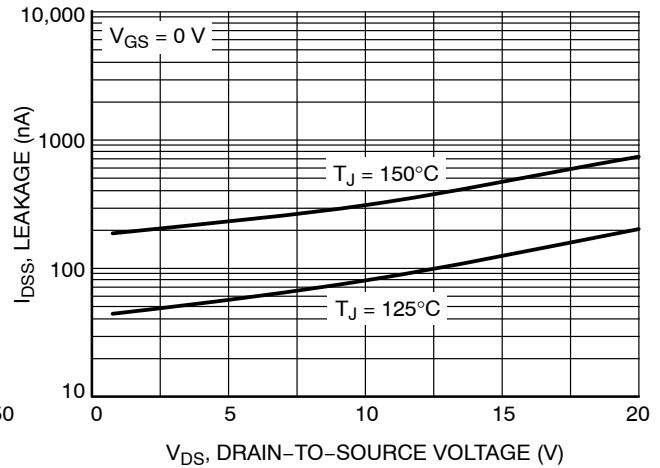


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

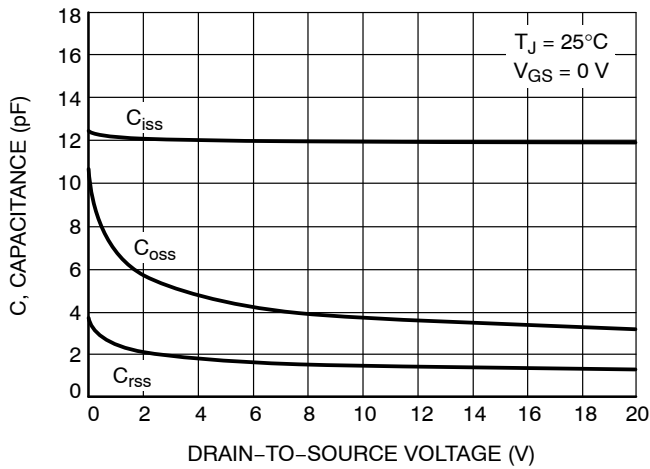


Figure 7. Capacitance Variation

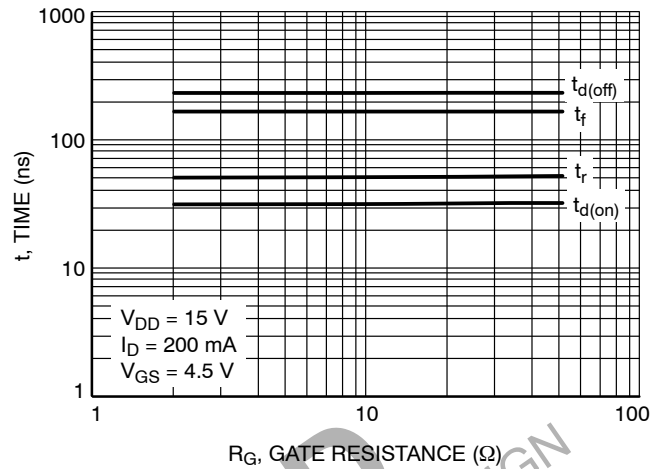


Figure 8. Resistive Switching Time Variation vs. Gate Resistance

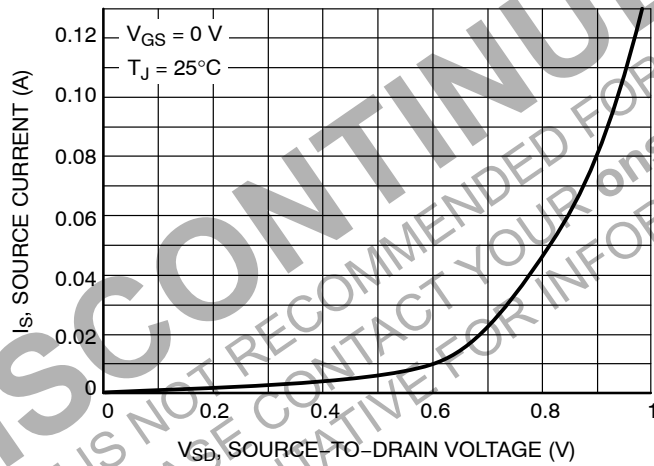
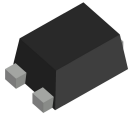
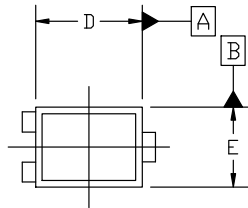


Figure 9. Diode Forward Voltage vs. Current

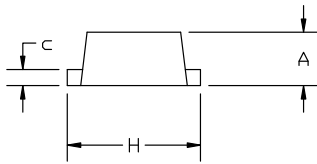


SOT-1123 0.80x0.60x0.37, 0.35P
CASE 524AA
ISSUE D

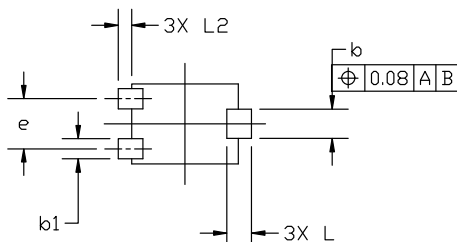
DATE 18 JAN 2024



TOP VIEW

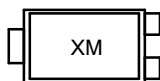


SIDE VIEW



BOTTOM VIEW

**GENERIC
MARKING DIAGRAM***



X = Specific Device Code
M = Date Code

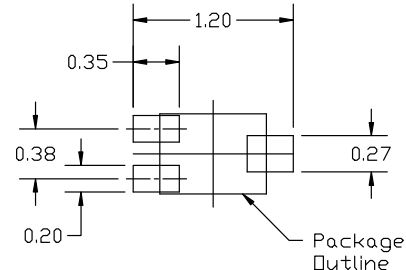
*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

MILLIMETERS

DIM	MIN	NOM	MAX
A	0.34	0.37	0.40
b	0.15	0.22	0.28
b1	0.10	0.15	0.20
c	0.07	0.12	0.17
D	0.75	0.80	0.85
E	0.55	0.60	0.65
e	0.35	0.38	0.40
H	0.950	1.000	1.050
L	0.185 REF		
L2	0.05	0.10	0.15



**RECOMMENDED
MOUNTING FOOTPRINT**

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERM/D.

STYLE 1:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. N/C
3. CATHODE

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. GATE
2. SOURCE
3. DRAIN

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DESCRIPTION:	SOT-1123 0.80x0.60x0.37, 0.35P	PAGE 1 OF 1

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