

P-Channel Enhancement Mode Field-Effect Transistor

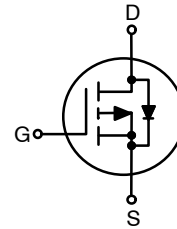
BSS84

General Description

This P-channel enhancement-mode field-effect transistor is produced using onsemi's proprietary, high cell density, DMOS technology. This very high density process minimizes on-state resistance and to provide rugged and reliable performance and fast switching. The BSS84 can be used, with a minimum of effort, in most applications requiring up to 0.13 A DC and can deliver current up to 0.52 A. This product is particularly suited to low-voltage applications requiring a low-current high-side switch.

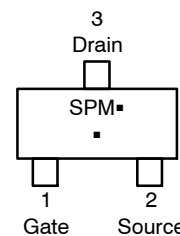
Features

- -0.13 A, -50 V, $R_{DS(on)} = 10\ \Omega$ at $V_{GS} = -5\text{ V}$
- Voltage-Controlled P-Channel Small-Signal Switch
- High-Density Cell Design for Low $R_{DS(on)}$
- High Saturation Current
- This Device is Pb-Free and Halogen Free



SOT-23-3
CASE 318-08

MARKING DIAGRAM



- SP = Specific Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping [†]
BSS84, BSS84-G	SOT-23-3 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain–Source Voltage	–50	V
V_{GSS}	Gate–Source Voltage	± 20	
I_{D}	Drain Current – Continuous (Note 1)	–0.13	A
	Drain Current – Pulsed (Note 1)	–0.52	
P_{D}	Maximum Power Dissipation (Note 1)	0.36	W
	Derate Above 25°C	2.9	mW/ $^\circ\text{C}$
$T_{\text{J}}, T_{\text{STG}}$	Operating and Storage Junction Temperature Range	–55 to +150	$^\circ\text{C}$
T_{L}	Maximum Lead Temperature for Soldering Purposes, 1/16" from Case for 10 s	300	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Ratings	Unit
$R_{\theta\text{JA}}$	Thermal Resistance, Junction–to–Ambient (Note 1)	350	$^\circ\text{C}/\text{W}$

ELECTRICAL CHARACTERISTICS (Note 2) $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain–Source Breakdown Voltage	$V_{\text{GS}} = 0\text{ V}, I_{\text{D}} = -250\text{ }\mu\text{A}$	–50	–	–	V
$\frac{\Delta BV_{\text{DSS}}}{\Delta T_{\text{J}}}$	Breakdown Voltage Temperature Coefficient	$I_{\text{D}} = -250\text{ }\mu\text{A}$, Referenced to 25°C	–	–48	–	mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{\text{DS}} = -50\text{ V}, V_{\text{GS}} = 0\text{ V}$	–	–	–15	μA
		$V_{\text{DS}} = -50\text{ V}, V_{\text{GS}} = 0\text{ V}, T_{\text{J}} = 125^\circ\text{C}$	–	–	–60	
I_{GSS}	Gate–Body Leakage	$V_{\text{GS}} = \pm 20\text{ V}, V_{\text{DS}} = 0\text{ V}$	–	–	± 10	nA

ON CHARACTERISTICS (Note 2)

$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{\text{DS}} = V_{\text{GS}}, I_{\text{D}} = -1\text{ mA}$	–0.8	–1.7	–2	V
$\frac{\Delta V_{\text{GS(th)}}}{\Delta T_{\text{J}}}$	Gate Threshold Voltage Temperature Coefficient	$I_{\text{D}} = -1\text{ mA}$, Referenced to 25°C	–	3	–	mV/ $^\circ\text{C}$
$R_{\text{DS(on)}}$	Static Drain–Source On–Resistance	$V_{\text{GS}} = -5\text{ V}, I_{\text{D}} = -0.10\text{ A}$	–	1.2	10	Ω
		$V_{\text{GS}} = -5\text{ V}, I_{\text{D}} = -0.10\text{ A}, T_{\text{J}} = 125^\circ\text{C}$	–	1.9	17	
$I_{\text{D(on)}}$	On–State Drain Current	$V_{\text{GS}} = -5\text{ V}, V_{\text{DS}} = -10\text{ V}$	–0.6	–	–	A
g_{FS}	Forward Transconductance	$V_{\text{DS}} = -25\text{ V}, I_{\text{D}} = -0.10\text{ A}$	0.05	0.6	–	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{\text{DS}} = -25\text{ V}, V_{\text{GS}} = 0\text{ V}, f = 1.0\text{ MHz}$	–	73	–	pF
C_{oss}	Output Capacitance		–	10	–	
C_{rss}	Reverse Transfer Capacitance		–	5	–	
R_{G}	Gate Resistance	$V_{\text{GS}} = 15\text{ mV}, f = 1.0\text{ MHz}$	–	9	–	Ω



ELECTRICAL CHARACTERISTICS (Note 2) $T_A = 25^\circ\text{C}$ unless otherwise noted. (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS (Note 2)						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -30\text{ V}$, $I_D = -0.27\text{ A}$, $V_{GS} = -10\text{ V}$, $R_{GEN} = 6\ \Omega$	–	2.5	5.0	ns
t_r	Turn-On Rise Time		–	6.3	13	
$t_{d(off)}$	Turn-Off Delay Time		–	10	20	
t_f	Turn-Off Fall Time		–	4.8	9.6	
Q_g	Total Gate Charge	$V_{DS} = -25\text{ V}$, $I_D = -0.10\text{ A}$, $V_{GS} = -5\text{ V}$	–	0.9	1.3	nC
Q_{gs}	Gate-Source Charge		–	0.2	–	
Q_{gd}	Gate-Drain Charge		–	0.3	–	

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I _S	Maximum Continuous Drain–Source Diode Forward Current		–	–	–0.13	A
V _{SD}	Drain–Source Diode Forward Voltage	V _{GS} = 0 V, I _S = –0.26 A (Note 2)	–	–0.8	–1.2	V
t _{rr}	Diode Reverse Recovery Time	I _F = –0.1 A, d _I /d _t = 100 A/μs (Note 2)	–	10	–	ns
Q _{rr}	Diode Reverse Recovery Charge		–	3	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



- $350^\circ\text{C}/\text{W}$ when mounted on a minimum pad.

- Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$

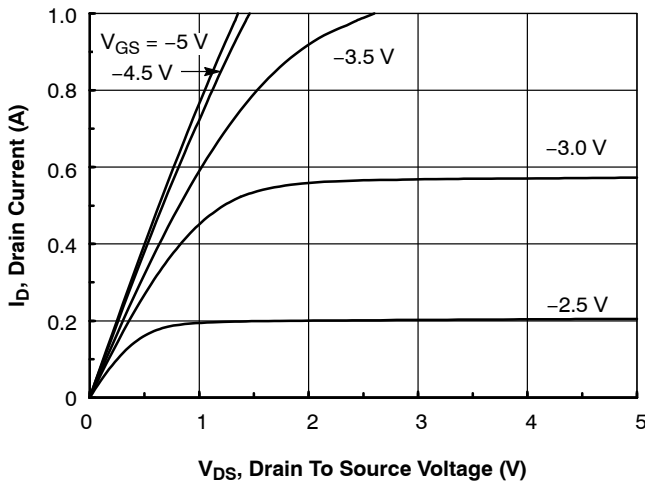
TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

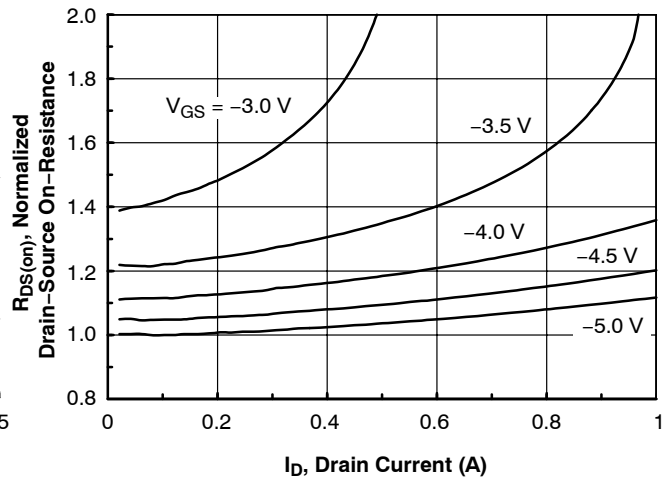


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage



TYPICAL CHARACTERISTICS (continued)

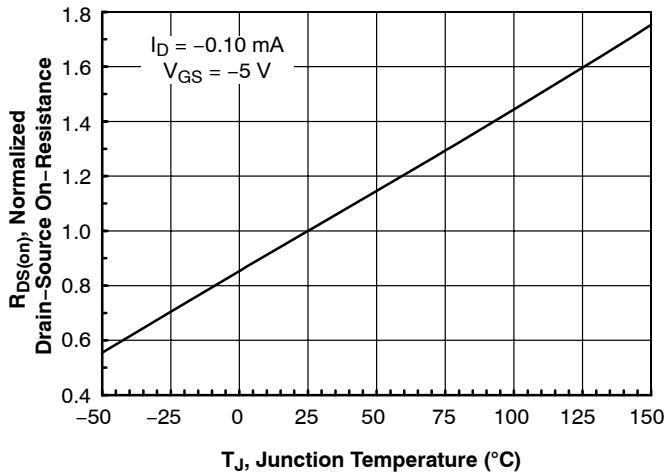


Figure 3. On-Resistance Variation with Temperature

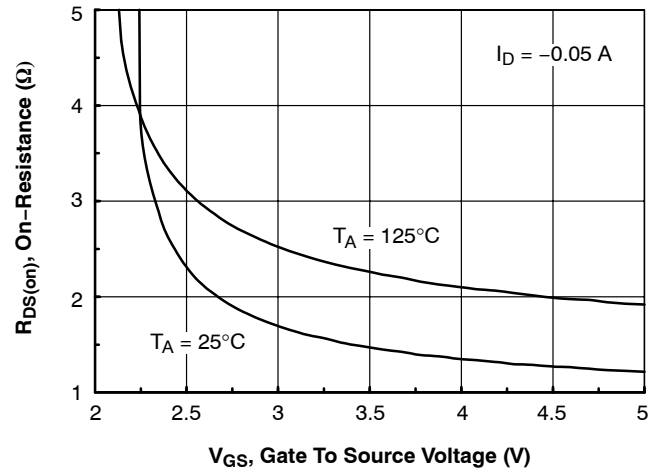


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

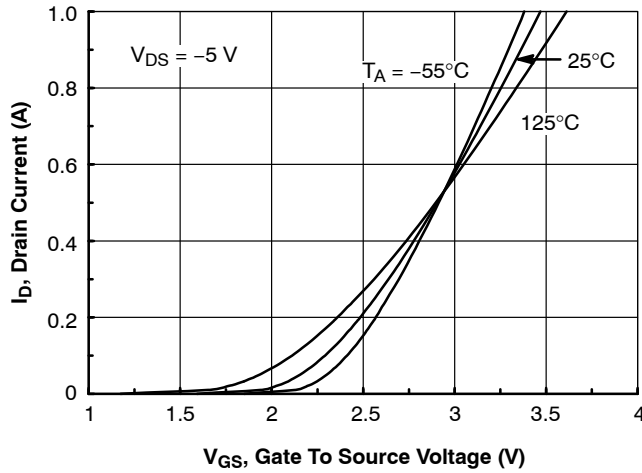


Figure 5. Transfer Characteristics

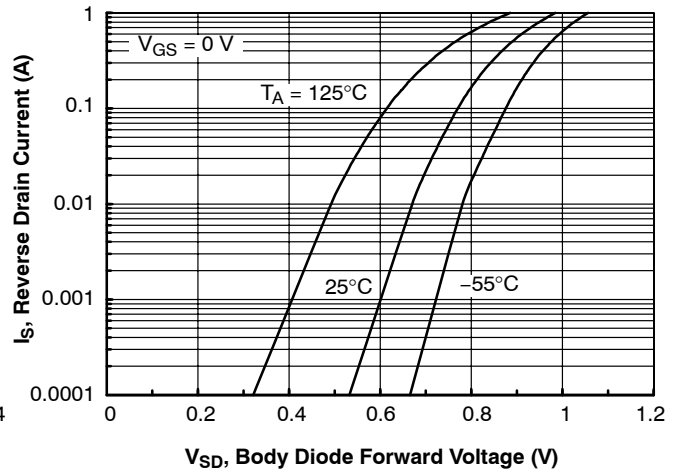


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

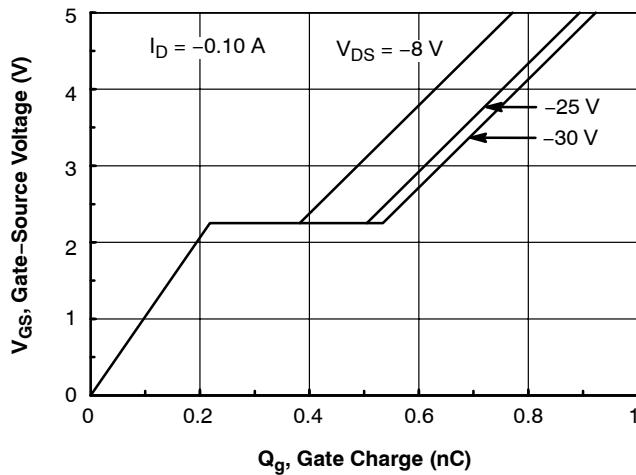


Figure 7. Gate Charge Characteristics

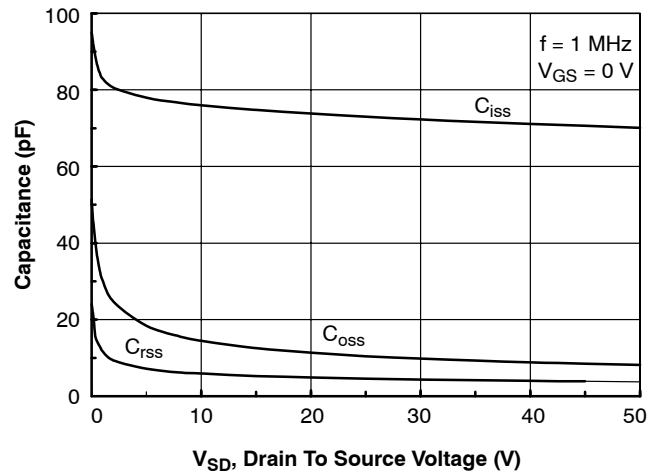


Figure 8. Capacitance Characteristics



TYPICAL CHARACTERISTICS (continued)

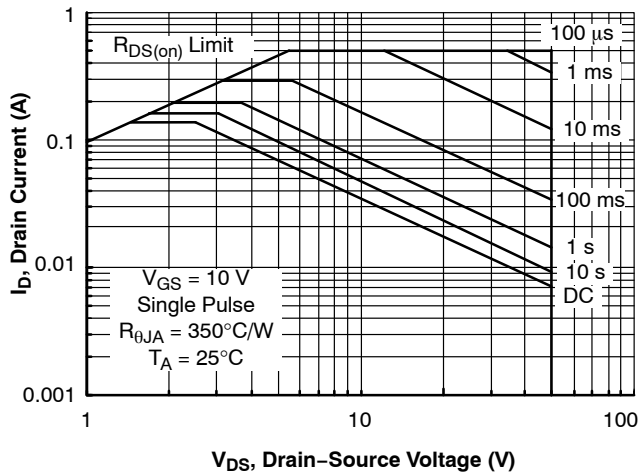


Figure 9. Maximum Safe Operating Area

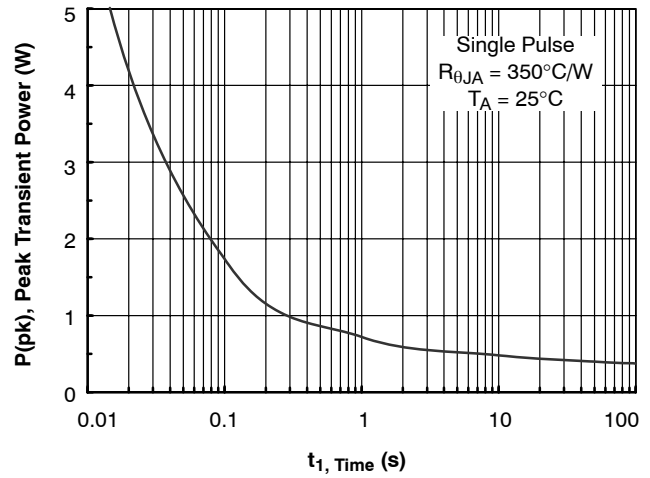


Figure 10. Single Pulse Maximum Power Dissipation

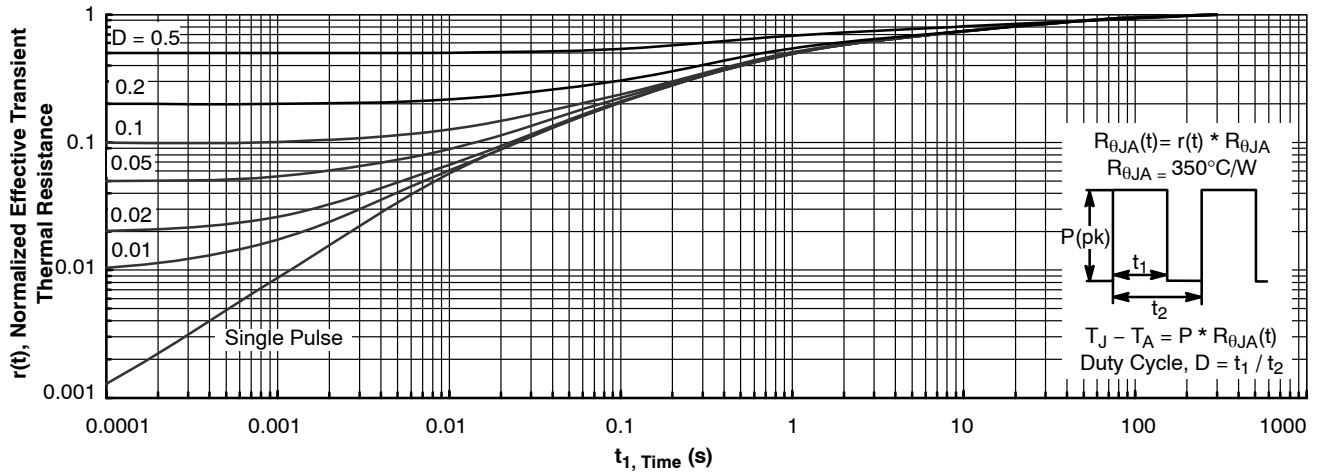
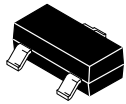


Figure 11. Transient Thermal Response Curve

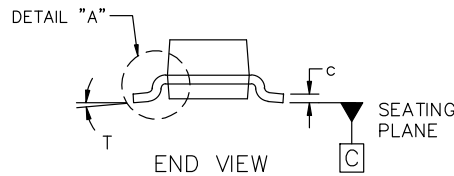
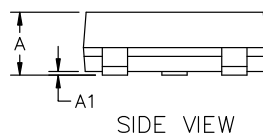
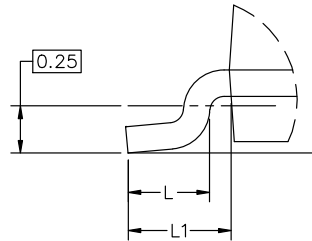
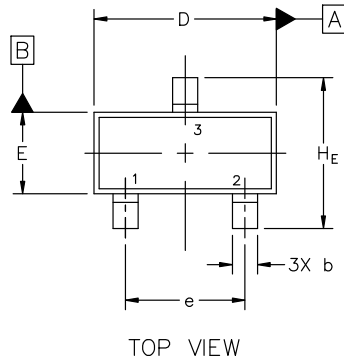
Thermal characterization performed using the conditions described in Note 1a.
Transient thermal response will change depending on the circuit board design.



SCALE 4:1

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CASE 318
ISSUE AU

DATE 14 AUG 2024

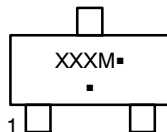


MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.89	1.00	1.11
A1	0.01	0.06	0.10
b	0.37	0.44	0.50
c	0.08	0.14	0.20
D	2.80	2.90	3.04
E	1.20	1.30	1.40
e	1.78	1.90	2.04
L	0.30	0.43	0.55
L1	0.35	0.54	0.69
HE	2.10	2.40	2.64
T	0°	---	10°

NOTES:

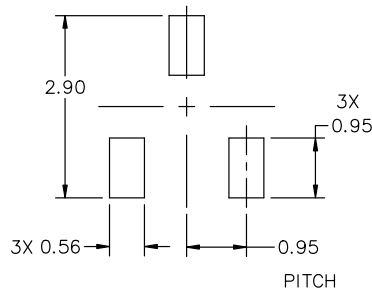
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

GENERIC
MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

STYLES ON PAGE 2

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STYLE 1 THRU 5: CANCELLED	STYLE 6: PIN 1. BASE 2. EMITTER 3. COLLECTOR	STYLE 7: PIN 1. EMITTER 2. BASE 3. COLLECTOR	STYLE 8: PIN 1. ANODE 2. NO CONNECTION 3. CATHODE		
STYLE 9: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 10: PIN 1. DRAIN 2. SOURCE 3. GATE	STYLE 11: PIN 1. ANODE 2. CATHODE 3. CATHODE-ANODE	STYLE 12: PIN 1. CATHODE 2. CATHODE 3. ANODE	STYLE 13: PIN 1. SOURCE 2. DRAIN 3. GATE	STYLE 14: PIN 1. CATHODE 2. GATE 3. ANODE
STYLE 15: PIN 1. GATE 2. CATHODE 3. ANODE	STYLE 16: PIN 1. ANODE 2. CATHODE 3. CATHODE	STYLE 17: PIN 1. NO CONNECTION 2. ANODE 3. CATHODE	STYLE 18: PIN 1. NO CONNECTION 2. CATHODE 3. ANODE	STYLE 19: PIN 1. CATHODE 2. ANODE 3. CATHODE-ANODE	STYLE 20: PIN 1. CATHODE 2. ANODE 3. GATE
STYLE 21: PIN 1. GATE 2. SOURCE 3. DRAIN	STYLE 22: PIN 1. RETURN 2. OUTPUT 3. INPUT	STYLE 23: PIN 1. ANODE 2. ANODE 3. CATHODE	STYLE 24: PIN 1. GATE 2. DRAIN 3. SOURCE	STYLE 25: PIN 1. ANODE 2. CATHODE 3. GATE	STYLE 26: PIN 1. CATHODE 2. ANODE 3. NO CONNECTION
STYLE 27: PIN 1. CATHODE 2. CATHODE 3. CATHODE	STYLE 28: PIN 1. ANODE 2. ANODE 3. ANODE				

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