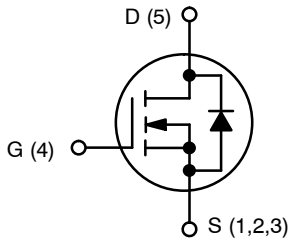
MOSFET – Power, Single N-Channel

60 V, 2.0 mΩ, 185 A

NVMYS2D2N06CL

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
60 V	2.0 mΩ @ 10 V	185 A
	2.7 mΩ @ 4.5 V	

LFPAK4
CASE 760AB



N-CHANNEL MOSFET

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- LFPAK4 Package, Industry Standard
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25 °C unless otherwise noted)

Symbol	Parameter			Value	Unit
V_{DSS}	Drain-to-Source Voltage			60	V
V_{GS}	Gate-to-Source Voltage			±20	V
I_D	Continuous Drain Current $R_{\theta JC}$ (Notes 1, 2, 3)	Steady State	T_C = 25 °C	185	A
			T_C = 100 °C	131	
P_D	Power Dissipation $R_{\theta JC}$ (Notes 1, 2)		T_C = 25 °C	134	W
			T_C = 100 °C	67	
I_D	Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	T_A = 25 °C	31	A
			T_A = 100 °C	22	
P_D	Power Dissipation $R_{\theta JA}$ (Notes 1, 2)		T_A = 25 °C	3.9	W
			T_A = 100 °C	1.9	
I_{DM}	Pulsed Drain Current	T_A = 25 °C, t_p = 10 μs		900	A
T_J, T_{stg}	Operating Junction and Storage Temperature			−55 to + 175	°C
I_S	Source Current (Body Diode)			112	A
E_{AS}	Single Pulse Drain-to-Source Avalanche Energy (T_J = 25 °C, $I_{L(pk)}$ = 11.9 A)			941	mJ
T_L	Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			260	°C

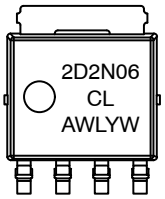
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Junction-to-Case - Steady State	1.12	°C/W
$R_{\theta JA}$	Junction-to-Ambient - Steady State (Note 2)	39	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

MARKING DIAGRAM



2D6N06CL	= Specific Device Code
A	= Assembly Location
WL	=Wafer Lot
Y	= Year
W	= Work Week

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

© Semiconductor Components Industries, LLC, 2018

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise specified)

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA		60	–	–	V
$V_{(BR)DSS}/T_J$	Drain-to-Source Breakdown Voltage Temperature Coefficient			–	26	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS} = 0 V, V_{DS} = 60 V	T_J = 25 °C	–	–	10	μA
			T_J = 125 °C	–	–	100	
I_{GSS}	Gate-to-Source Leakage Current	V_{DS} = 0 V, V_{GS} = 20 V		–	–	100	nA
ON CHARACTERISTICS (Note 4)							
$V_{GS(TH)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 180 μA		1.2	–	2.0	V
$V_{GS(TH)}/T_J$	Negative Threshold Temperature Coefficient			–	–5.3	–	mV/°C
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = 10 V	I_D = 50 A	–	1.6	1.9	mΩ
		V_{GS} = 4.5 V	I_D = 50 A	–	2.1	2.6	
g_{FS}	Forward Transconductance	V_{DS} = 15 V, I_D = 50 A		–	135	–	S
CHARGES, CAPACITANCES & GATE RESISTANCE							
C_{ISS}	Input Capacitance	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 25 V		–	4850	–	pF
C_{OSS}	Output Capacitance			–	2450	–	
C_{RSS}	Reverse Transfer Capacitance			–	25	–	
$Q_{G(TOT)}$	Total Gate Charge	V_{GS} = 4.5 V, V_{DS} = 48 V; I_D = 50 A		–	31	–	nC
$Q_{G(TOT)}$	Total Gate Charge	V_{GS} = 10 V, V_{DS} = 48 V; I_D = 50 A		–	69	–	
$Q_{G(TH)}$	Threshold Gate Charge	V_{GS} = 10 V, V_{DS} = 48 V; I_D = 50 A		–	6.3	–	
Q_{GS}	Gate-to-Source Charge			–	11.5	–	
Q_{GD}	Gate-to-Drain Charge			–	7.6	–	
V_{GP}	Plateau Voltage			–	2.7	–	V
SWITCHING CHARACTERISTICS (Note 5)							
$t_{d(ON)}$	Turn-On Delay Time	V_{GS} = 10 V, V_{DS} = 48 V, I_D = 50 A, R_G = 2.5 Ω		–	13	–	ns
t_r	Rise Time			–	20	–	
$t_{d(OFF)}$	Turn-Off Delay Time			–	53	–	
t_f	Fall Time			–	9.4	–	
DRAIN-SOURCE DIODE CHARACTERISTICS							
V_{SD}	Forward Diode Voltage	V_{GS} = 0 V, I_S = 50 A	T_J = 25 °C	–	0.8	1.2	V
			T_J = 125 °C	–	0.7	–	
t_{RR}	Reverse Recovery Time	V_{GS} = 0 V, dIS/dt = 20 A/μs, I_S = 50 A		–	64	–	ns
t_a	Charge Time			–	40	–	
t_b	Discharge Time			–	24	–	
Q_{RR}	Reverse Recovery Charge			–	84	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

Share Feedback
Your Opinion Matters

TYPICAL CHARACTERISTICS

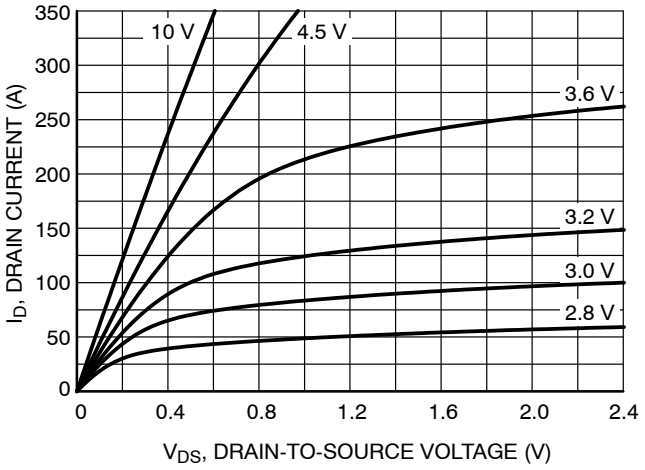


Figure 1. On-Region Characteristics

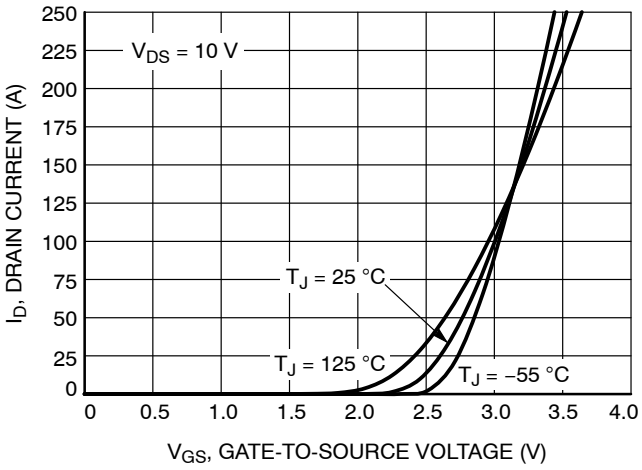


Figure 2. Transfer Characteristics

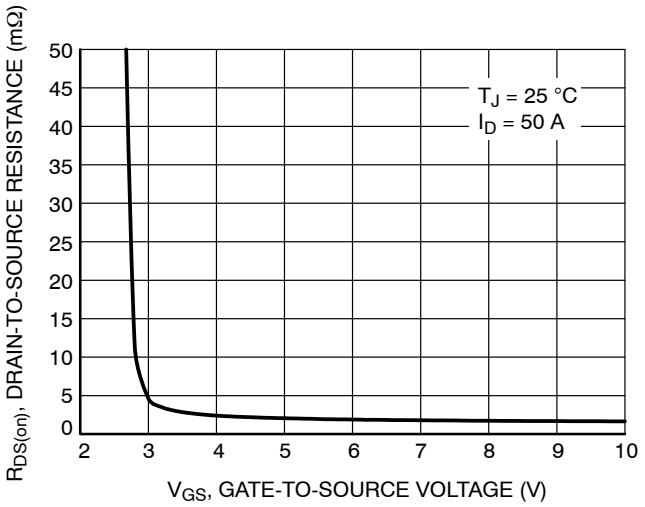


Figure 3. On-Resistance vs. Gate-to-Source Voltage

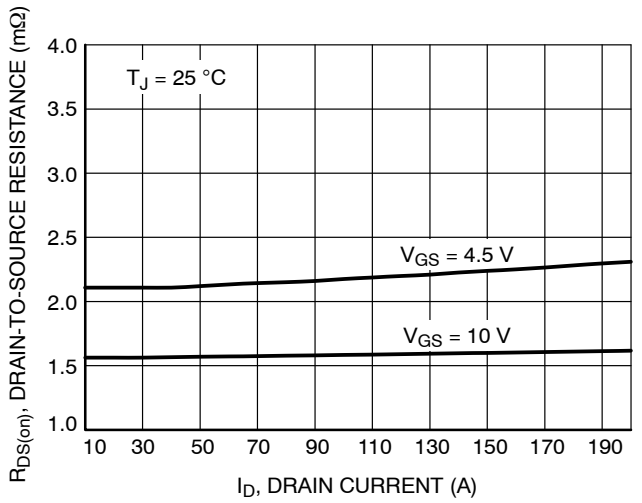


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

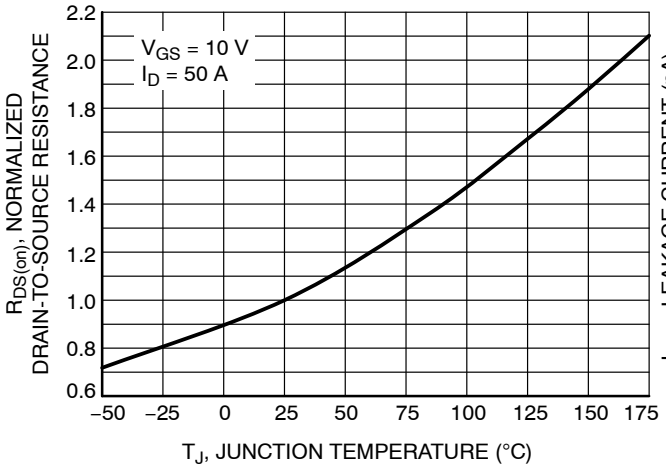


Figure 5. On-Resistance Variation with Temperature

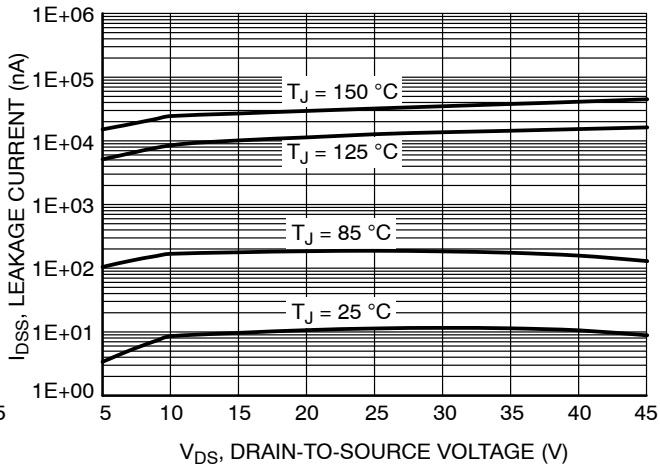


Figure 6. Drain-to-Source Leakage Current vs. Voltage

Share Feedback
Your Opinion Matters

TYPICAL CHARACTERISTICS (continued)

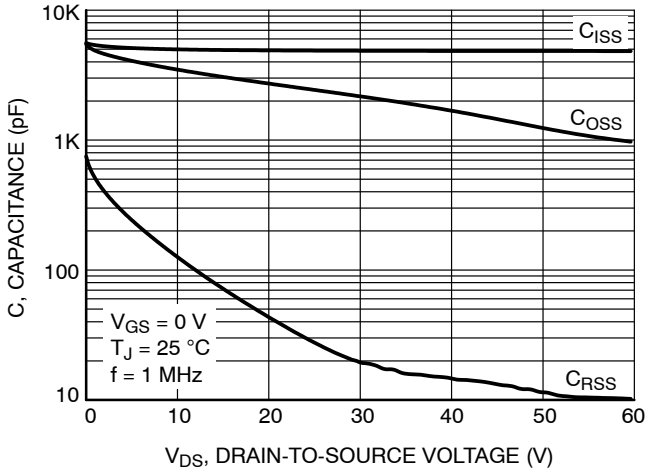


Figure 7. Capacitance Variation

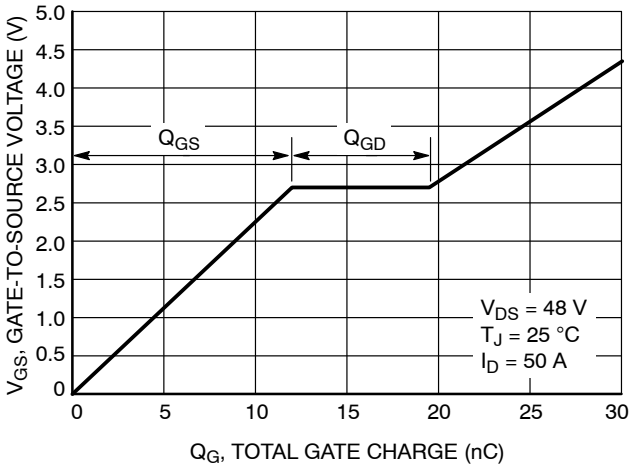


Figure 8. Gate-to-Source Voltage vs. Total Charge

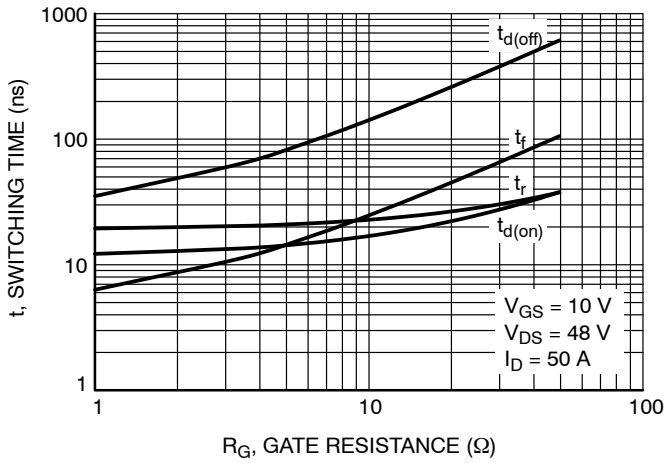


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

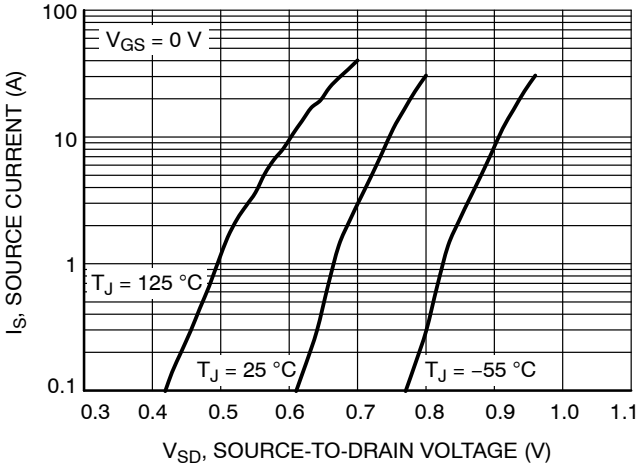


Figure 10. Diode Forward Voltage vs. Current

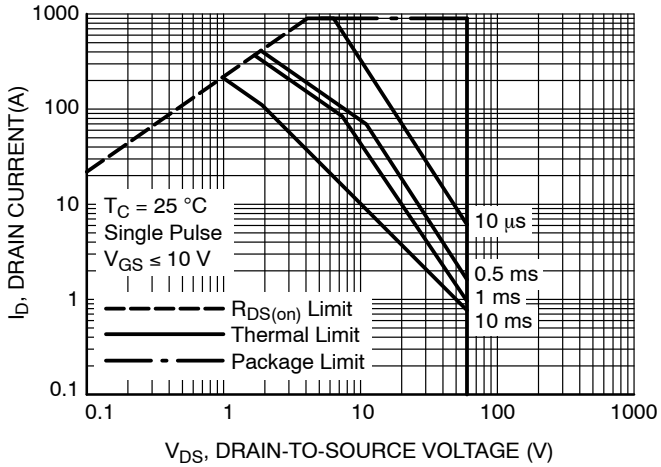


Figure 11. Maximum Rated Forward Biased Safe Operating Area

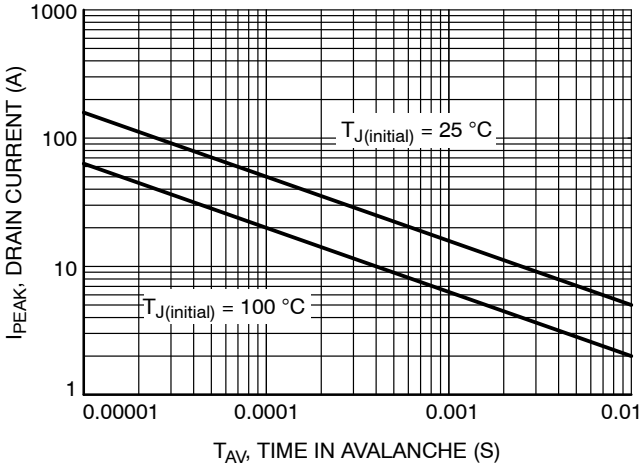


Figure 12. Maximum Drain Current vs. Time in Avalanche

Share Feedback
Your Opinion Matters

TYPICAL CHARACTERISTICS (continued)

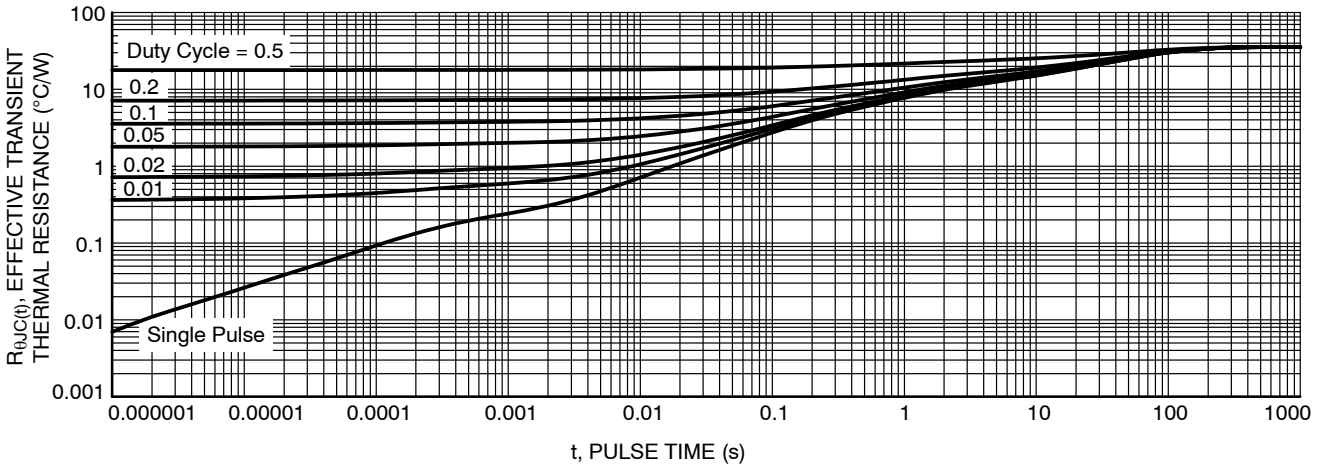


Figure 13. Thermal Response

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NVMYS2D2N06CLTWG	2D2N06CL	LFPAK4 (Pb-Free)	3,000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Share Feedback
Your Opinion Matters

REVISION HISTORY

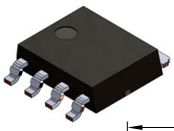
Revision	Description of Changes	Date
1	Rebranded the Data Sheet to **onsemi**.	11/19/2025

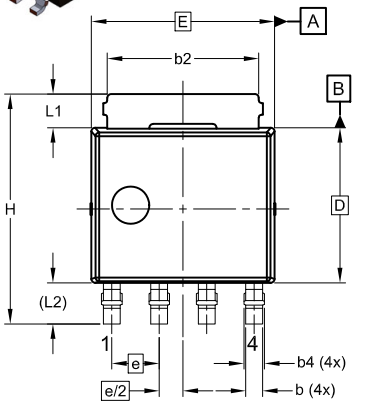
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

Share Feedback
Your Opinion Matters

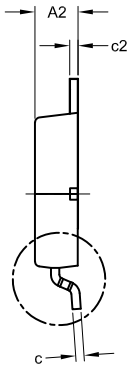
LFPAK4 4.90x4.15x1.15MM, 1.27P
CASE 760AB
ISSUE D

DATE 22 MAY 2024



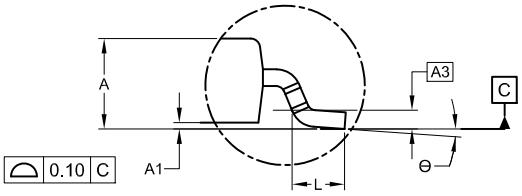


TOP VIEW

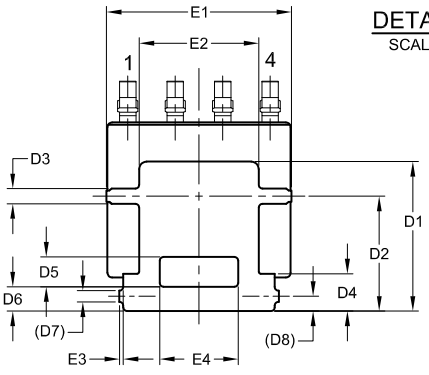


SIDE VIEW

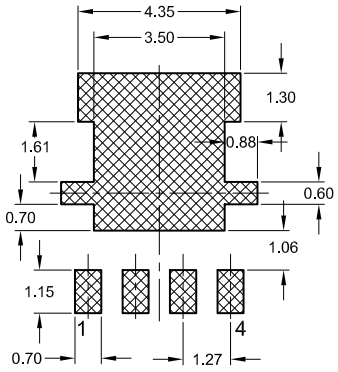
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
4. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.



DETAIL 'A'
SCALE: 2:1



BOTTOM VIEW

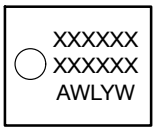


RECOMMENDED LAND PATTERN

*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

MILLIMETER			
DIM	MIN	NOM	MAX
A	1.10	1.20	1.30
A1	0.00	0.08	0.15
A2	1.10	1.15	1.20
A3	0.25 BSC		
b	0.40	0.45	0.50
b2	3.80	4.10	4.40
b4	0.45	0.55	0.65
c	0.19	0.22	0.25
c2	0.19	0.22	0.25
D	4.15 BSC		
D1	3.80	4.00	4.20
D2	3.00	3.10	3.20
D3	0.30	0.40	0.50
D4	0.90	1.00	1.10
D5	0.70	0.80	0.90
D6	0.55	0.65	0.75
D7	0.31 REF		
D8	0.40 REF		
E	4.90 BSC		
E1	4.85	4.95	5.05
E2	3.10	3.20	3.30
E3	0.00	0.10	0.20
E4	2.00	2.10	2.20
e	1.27 BSC		
e/2	0.635 BSC		
e1	0.40 REF		
H	6.00	6.15	6.30
L	0.50	0.70	0.90
L1	0.80	0.90	1.00
L2	1.10 REF		
Θ	0°	4°	8°

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON82777G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**LFPAK4 4.90x4.15x1.15MM, 1.27P**		**PAGE 1 OF 1**

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

onsemi, ONSEMI , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales