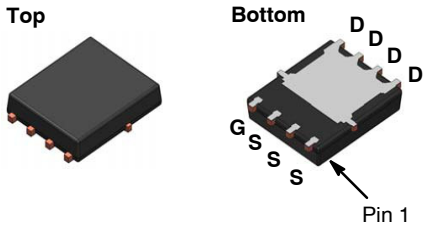
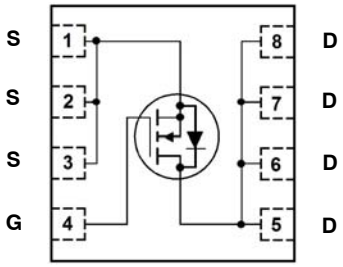
MOSFET – N-Channel, Shielded Gate, POWERTRENCH®

100 V, 78 A, 7.2 mΩ

FDMS86182, FDMS86182-NC



Power 56
(PQFN8)
CASE 483AE



General Description

This N-Channel MV MOSFET is produced using **onsemi**'s advanced POWETRENCH process that incorporates Shielded Gate technology. This process has been optimized to minimize on-state resistance and yet maintain superior switching performance with best class soft body diode.

Features

- Shielded Gate MOSFET Technology
- Max $R_{DS(on)}$ = 7.2 mΩ at V_{GS} = 10 V, I_D = 28 A
- Max $R_{DS(on)}$ = 19.5 mΩ at V_{GS} = 6 V, I_D = 14 A
- 50% Lower Q_{rr} than Other MOSFET Suppliers
- Lowers Switching Noise/EMI
- MSL1 Robust Package Design
- 100% UIL Tested
- RoHS Compliant

Applications

- Primary DC-DC MOSFET
- Synchronus Rectifier in DC-DC and AC-DC
- Motor Drive
- Solar

MARKING DIAGRAM

$Y	= **onsemi** Logo
&Z	= Assembly Plant Code
&3	= Date Code (Year &Week)
&K	= Lot Traceability Code
FDMS86182	= Specific Device Code

MOSFET MAXIMUM RATINGS (T_A = 25 °C unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DS}	Drain to Source Voltage	100	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current: - Continuous T_C = 25 °C (Note 5) - Continuous T_C = 100 °C (Note 5) - Continuous T_A = 25 °C (Note 1a) - Pulsed (Note 4)	 78 49 13 364	A
E_{AS}	Single Pulse Avalanche Energy (Note 3)	216	mJ
P_D	Power Dissipation: T_C = 25 °C T_A = 25 °C (Note 1a)	 83 2.5	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	50	

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain-to-Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		56		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate-to-Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 150 μA	2.0	3.2	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate-to-Source Threshold Voltage Temperature Coefficient	I_D = 150 μA, referenced to 25 °C		–9		mV/°C
$R_{DS(on)}$	Static Drain-to-Source On Resistance	V_{GS} = 10 V, I_D = 28 A		5.9	7.2	mΩ
		V_{GS} = 6 V, I_D = 14 A		9.3	19.5	
		V_{GS} = 10 V, I_D = 28 A, T_J = 125 °C		9.9	12.1	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 28 A		63		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz		1880	2635	pF
C_{oss}	Output Capacitance			1105	1550	pF
C_{rss}	Reverse Transfer Capacitance			13	25	pF
R_g	Gate Resistance		0.1	0.5	1.2	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 50 V, I_D = 28 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		13	24	ns
t_r	Rise Time			4	10	
$t_{d(off)}$	Turn-Off Delay Time			18	33	
t_f	Fall Time			4	10	
$Q_{g(tot)}$	Total Gate Charge	V_{GS} = 0 V to 10 V, V_{DD} = 50 V, I_D = 28 A		26	37	nC
$Q_{g(tot)}$	Total Gate Charge	V_{GS} = 0 V to 6 V, V_{DD} = 50 V, I_D = 28 A		17	24	
Q_{gs}	Gate-to-Source Charge	V_{DD} = 50 V, I_D = 28 A		8.2		
Q_{gd}	Gate-to-Drain “Miller” Charge	V_{DD} = 50 V, I_D = 28 A		5.1		
Q_{oss}	Output Charge	V_{DD} = 50 V, V_{GS} = 0 V		73		

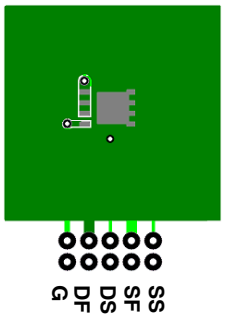
ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source-to-Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.1 A (Note 2)		0.7	1.2	V
		V_{GS} = 0 V, I_S = 28 A (Note 2)		0.8	1.3	V
t_{rr}	Reverse Recovery Time	I_F = 14 A, di/dt = 300 A/μs		28	45	ns
Q_{rr}	Reverse Recovery Charge			52	84	nC
t_{rr}	Reverse Recovery Time	I_F = 14 A, di/dt = 1000 A/μs		22	36	ns
Q_{rr}	Reverse Recovery Charge			116	186	nC

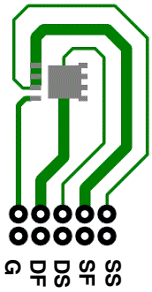
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material. $R_{\theta CA}$ is determined by the user's board design.



a) 50 °C/W when mounted on a 1 in^2 pad of 2 oz copper



b) 125 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. E_{AS} of 216 mJ is based on starting T_J = 25 °C, N-ch: L = 3 mH, I_{AS} = 12 A, V_{DD} = 100 V, V_{GS} = 10 V. 100% test at L = 0.1 mH, I_{AS} = 38 A.
4. Pulsed Id please refer to Fig 11 SOA graph for more details.
5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

TYPICAL CHARACTERISTICS

(T_J = 25 °C unless otherwise noted)

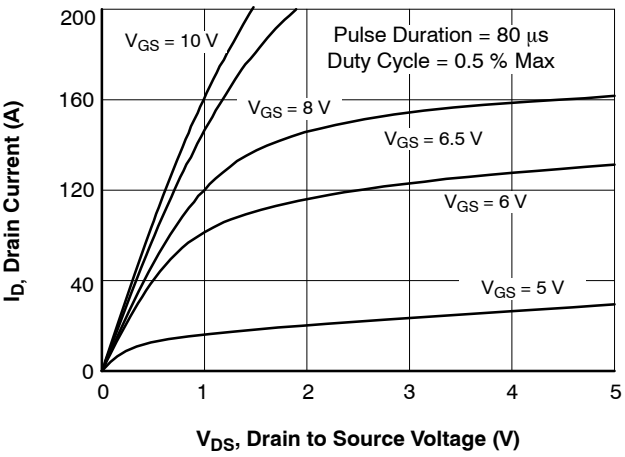


Figure 1. On-Region Characteristics

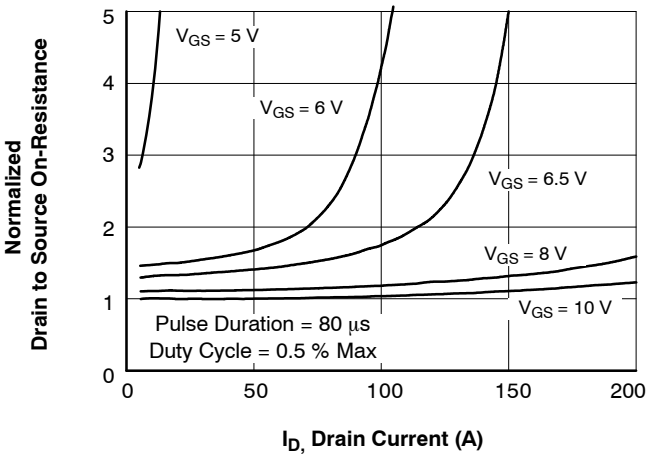


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

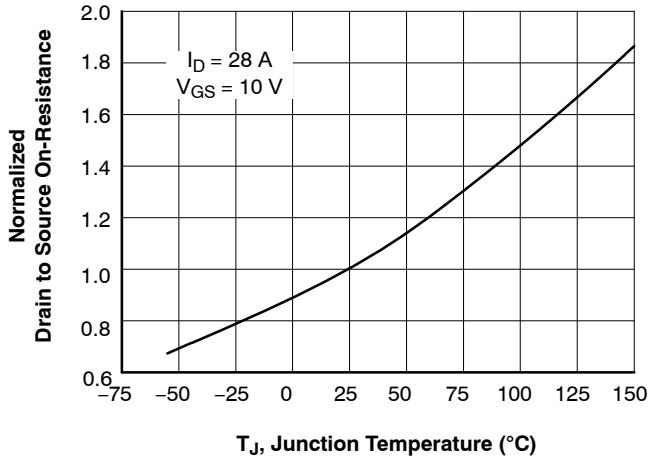


Figure 3. Normalized On-Resistance vs. Junction Temperature

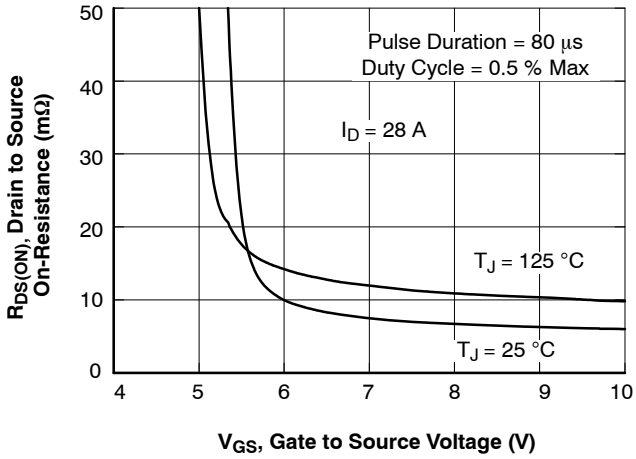


Figure 4. On-Resistance vs. Gate to Source Voltage

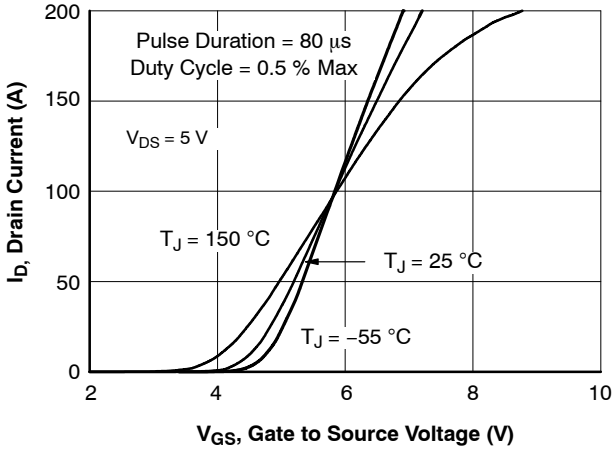


Figure 5. Transfer Characteristics

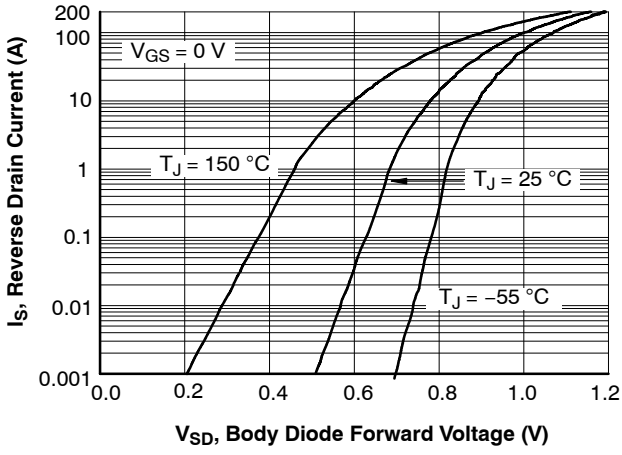


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (continued)

(T_J = 25 °C unless otherwise noted)

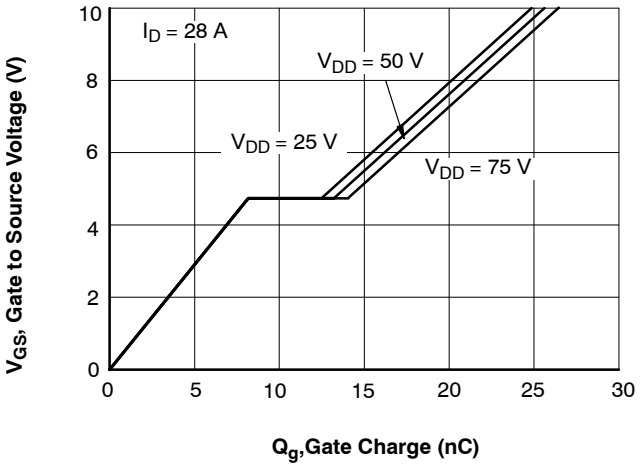


Figure 7. Gate Charge Characteristics

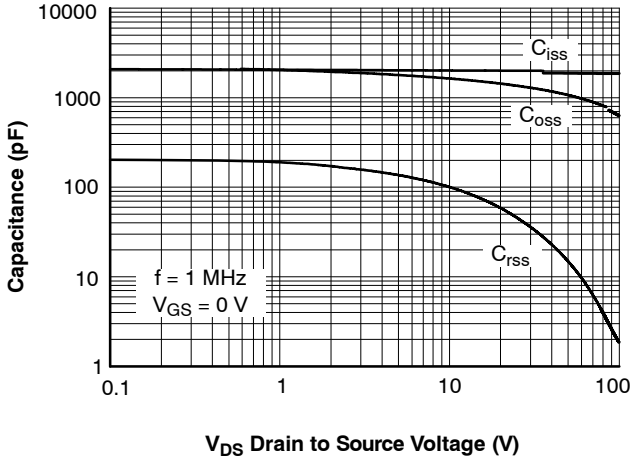


Figure 8. Capacitance vs Drain to Source Voltage

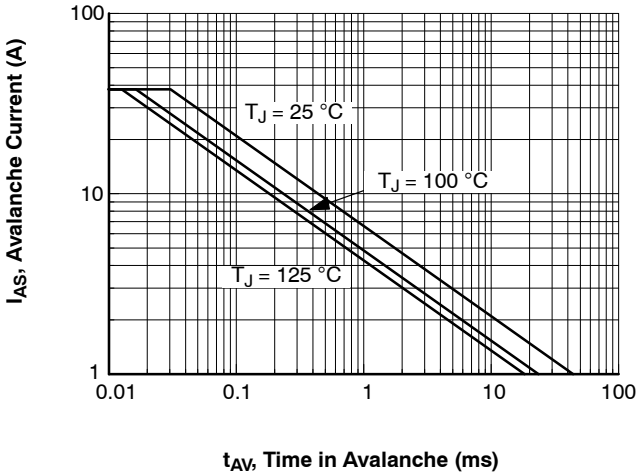


Figure 9. Unclamped Inductive Switching Capability

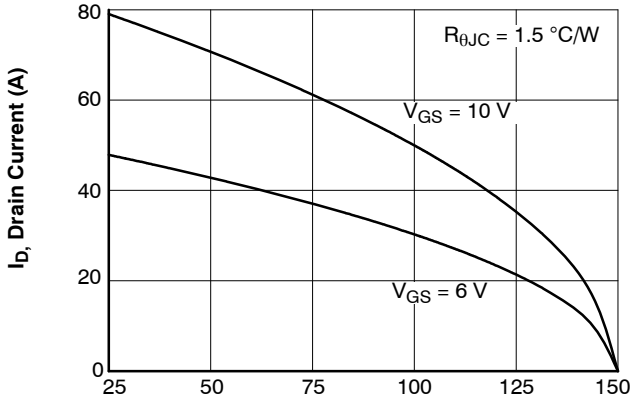


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

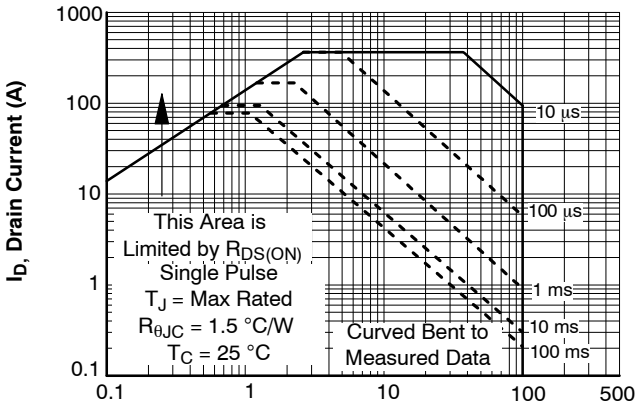


Figure 11. Forward Bias Safe Operating Area

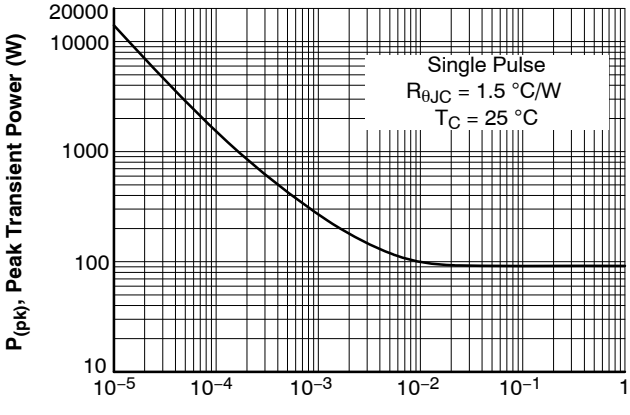


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (continued)

(T_J = 25 °C unless otherwise noted)

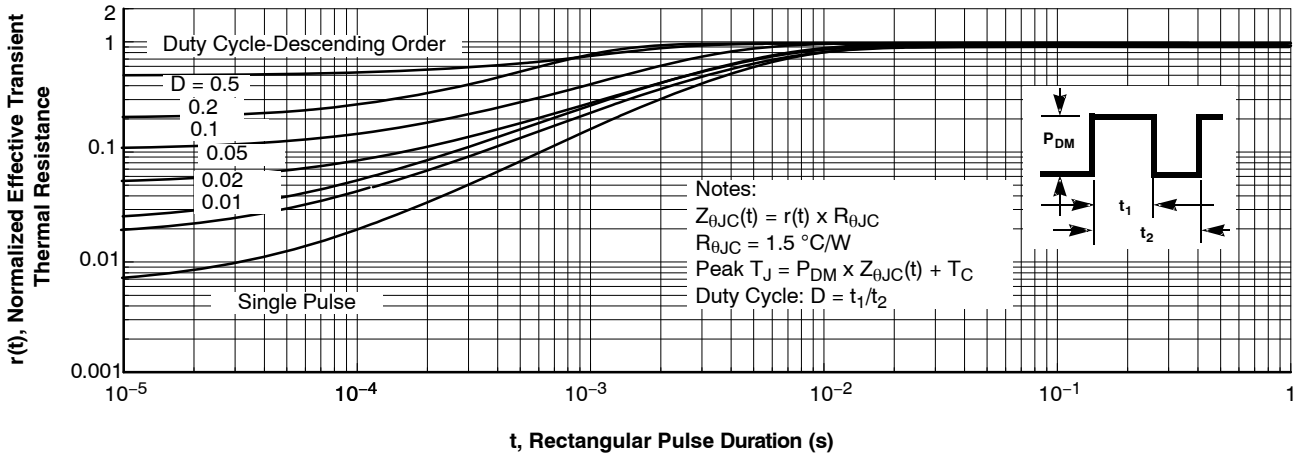


Figure 13. Junction-to-Case Transient Thermal Response Curve

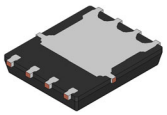
ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Shipping†
FDMS86182	FDMS86182	Power 56	13”	12mm	3,000 / Tape & Reel
FDMS86182-NC	FDMS86182	Power 56	13”	12mm	3,000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

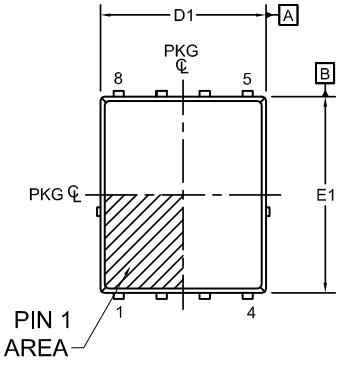
REVISION HISTORY

Revision	Description of Changes	Date
2	Addition of FDMS86182-NC OPN + Converted the Data Sheet to **onsemi** format.	2/6/2026

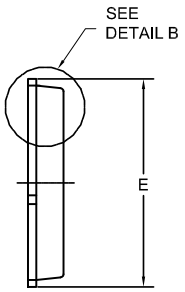


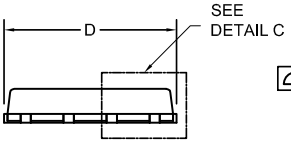
PQFN8 5X6, 1.27P
CASE 483AE
ISSUE C

DATE 21 JAN 2022

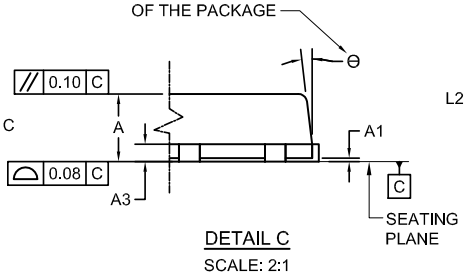


TOP VIEW

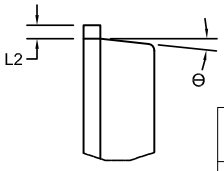




SIDE VIEW



DETAIL C
SCALE: 2:1

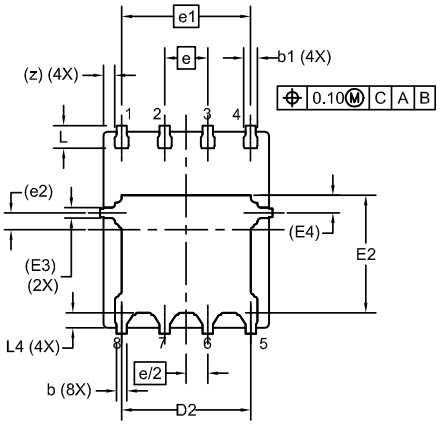


DETAIL B
SCALE: 2:1

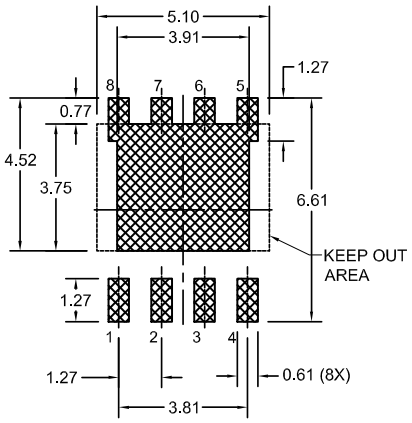
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
b	0.21	0.31	0.41
b1	0.31	0.41	0.51
A3	0.15	0.25	0.35
D	4.90	5.00	5.20
D1	4.80	4.90	5.00
D2	3.61	3.82	3.96
E	5.90	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.78
E3	0.30 REF		
E4	0.52 REF		
e	1.27 BSC		
e/2	0.635 BSC		
e1	3.81 BSC		
e2	0.50 REF		
L	0.51	0.66	0.76
L2	0.05	0.18	0.30
L4	0.34	0.44	0.54
z	0.34 REF		
Θ	0°	-	12°



BOTTOM VIEW



LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON13655G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**PQFN8 5X6, 1.27P**		**PAGE 1 OF 1**

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