

# MOSFET – N-Channel, Shielded Gate, POWERTRENCH®

100 V, 22 A, 25 mΩ

## FDMS86102LZ, FDMS86102LZ-NC

### General Description

This N-Channel logic Level MOSFETs are produced using onsemi's advanced POWERTRENCH process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance. G-S zener has been added to enhance ESD voltage level.

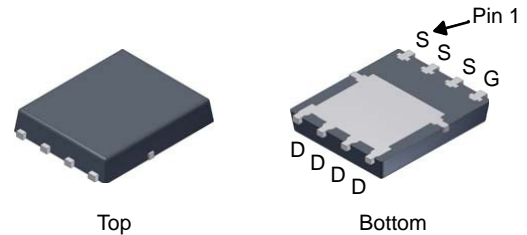
### Features

- Shielded Gate MOSFET Technology
- Max  $R_{DS(on)}$  = 25 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 7\text{ A}$
- Max  $R_{DS(on)}$  = 37 mΩ at  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 5.8\text{ A}$
- HBM ESD Protection Level > 6 kV Typical (Note 4)
- 100% UIL Tested
- This Device is Halide Free and RoHS Compliant with Exemption 7a, Pb-Free 2LI (on second level interconnection)

### Applications

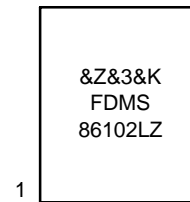
- DC-DC Conversion
- Inverter
- Synchronous Rectifier

$V_{DS}$	$R_{DS(on)}$ MAX	$I_D$ Max
100 V	25 mΩ @ $V_{GS} = 10\text{ V}$	22 A
	37 mΩ @ $V_{GS} = 4.5\text{ V}$	



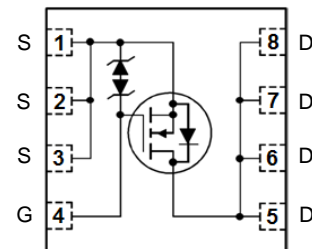
PQFN8 5X6, 1.27P  
Power 56  
CASE 483AE

### MARKING DIAGRAM



&Z = Assembly Plant Code  
&3 = 3-Digit Date Code  
&K = 2-Digits Lot Run Code  
FDMS86102LZ = Specific Device Code

### PIN CONNECTIONS



### ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

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## MOSFET MAXIMUM RATINGS ( $T_A = 25\text{ }^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating	Unit
$V_{DS}$	Drain to Source Voltage	100	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current	Continuous, $T_C = 25\text{ }^\circ\text{C}$	22
		Continuous, $T_A = 25\text{ }^\circ\text{C}$ (Note 1a)	7
		Pulsed	40
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	84	mJ
$P_D$	Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	69
		$T_A = 25\text{ }^\circ\text{C}$ (Note 1a)	2.5
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## THERMAL CHARACTERISTICS

Symbol	Parameter	Rating	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.8	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

## ELECTRICAL CHARACTERISTICS ( $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}, V_{GS} = 0\text{ V}$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		70		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			$\pm 10$	$\mu\text{A}$

### ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	1.0	1.5	2.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-6		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 7\text{ A}$		18.6	25	m $\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 5.8\text{ A}$		23.5	37	
		$V_{GS} = 10\text{ V}, I_D = 7\text{ A}, T_J = 125\text{ }^\circ\text{C}$		31.2	42	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 7\text{ A}$		26		S

### DYNAMIC CHARACTERISTICS

$C_{iss}$	Input Capacitance	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		979	1305	pF
$C_{oss}$	Output Capacitance			175	235	pF
$C_{rss}$	Reverse Transfer Capacitance			8.9	15	pF
$R_g$	Gate Resistance			0.9		$\Omega$

### SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{ V}, I_D = 7\text{ A}, V_{GS} = 10\text{ V}, R_{GEN} = 6\text{ }\Omega$		6.7	14	ns
$t_r$	Rise Time			2.6	10	ns
$t_{d(off)}$	Turn-Off Delay Time			19	35	ns
$t_f$	Fall Time			2.5	10	ns

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## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25 °C unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
<b>SWITCHING CHARACTERISTICS</b>						
Q <sub>g(TOT)</sub>	Total Gate Charge	V <sub>GS</sub> = 0 V to 10 V, V <sub>DD</sub> = 50 V, I <sub>D</sub> = 7 A		16	22	nC
		V <sub>GS</sub> = 0 V to 4.5 V, V <sub>DD</sub> = 50 V, I <sub>D</sub> = 7 A		7.8	11	
Q <sub>gs</sub>	Total Gate Charge	V <sub>DD</sub> = 50 V, I <sub>D</sub> = 7 A		2.4		nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge			2.6		nC

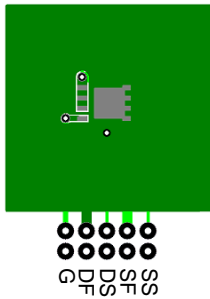
## DRAIN-SOURCE DIODE CHARACTERISTICS

V <sub>SD</sub>	Source to Drain Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 7 A (Note 2)		0.81	1.3	V
		V <sub>GS</sub> = 0 V, I <sub>S</sub> = 2 A (Note 2)		0.72	1.2	
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = 7 A, di/dt = 100 A/μs		35	57	ns
Q <sub>rr</sub>	Reverse Recovery Charge			25	40	nC

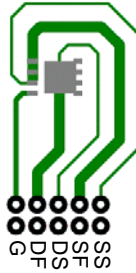
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

### NOTES:

- R<sub>θJA</sub> is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R<sub>θJC</sub> is guaranteed by design while R<sub>θCA</sub> is determined by the user's board design.



a. 50 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b. 125 °C/W when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
- Starting T<sub>J</sub> = 25 °C; N-ch: L = 1 mH, I<sub>AS</sub> = 13 A, V<sub>DD</sub> = 90 V, V<sub>GS</sub> = 10 V.
- The diode connected between gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

TYPICAL CHARACTERISTICS ( $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted)

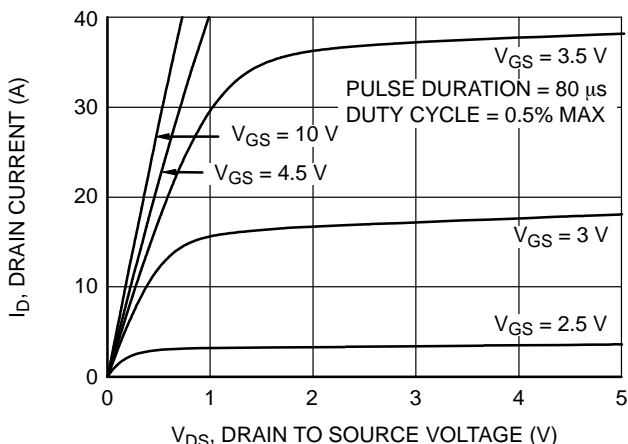


Figure 1. On-Region Characteristics

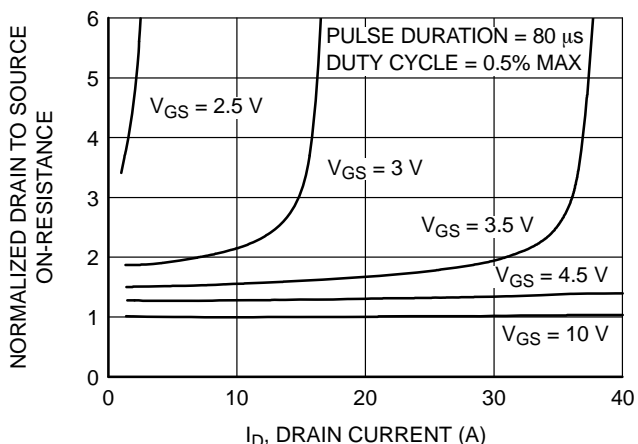


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

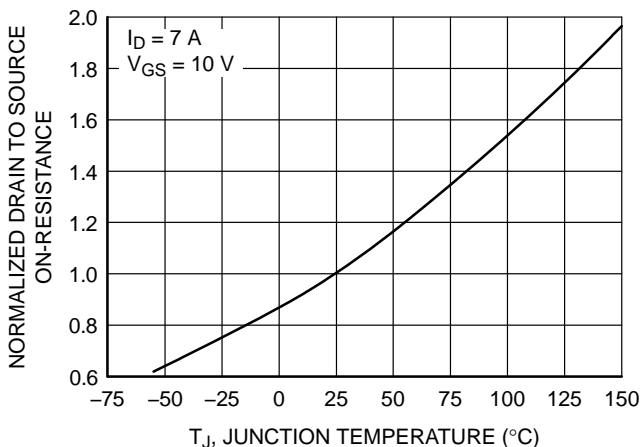


Figure 3. Normalized On-Resistance vs. Junction Temperature

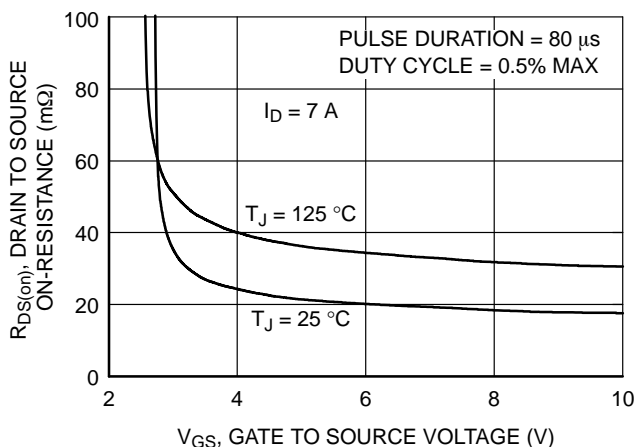


Figure 4. On-Resistance vs. Gate to Source Voltage

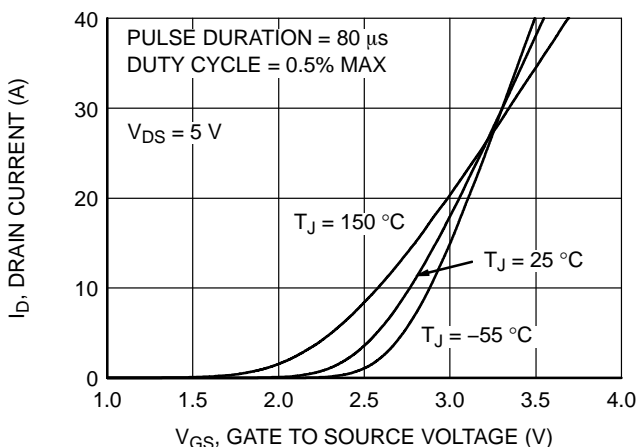


Figure 5. Transfer Characteristics

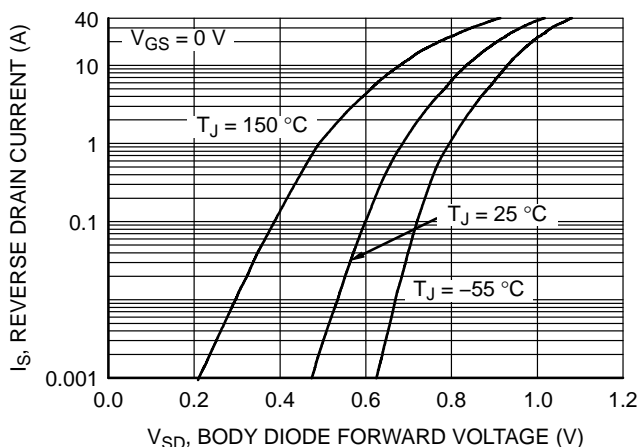


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

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## TYPICAL CHARACTERISTICS ( $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted) (continued)

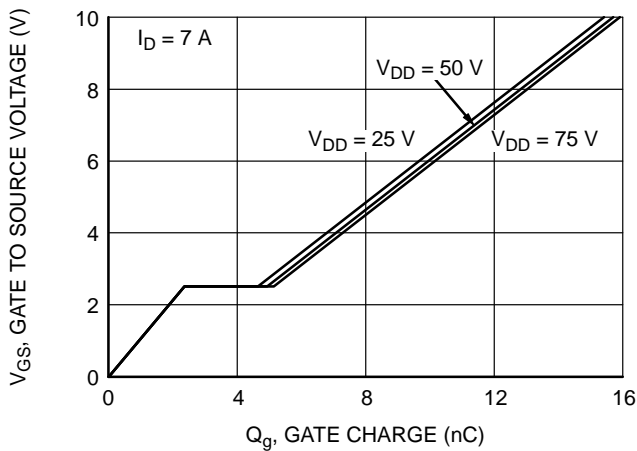


Figure 7. Gate Charge Characteristics

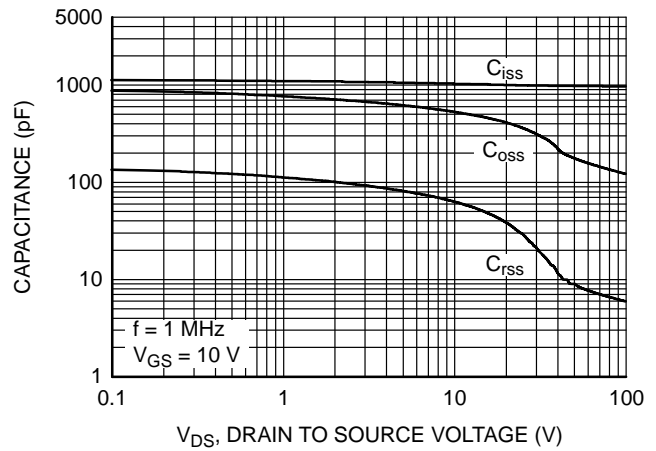


Figure 8. Capacitance vs. Drain to Source Voltage

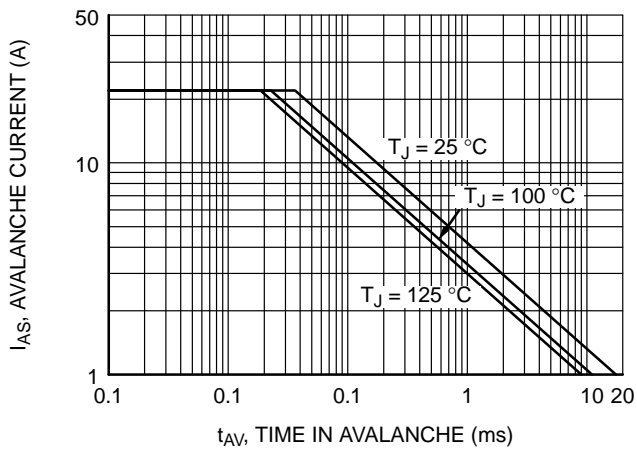


Figure 9. Unclamped Inductive Switching Capability

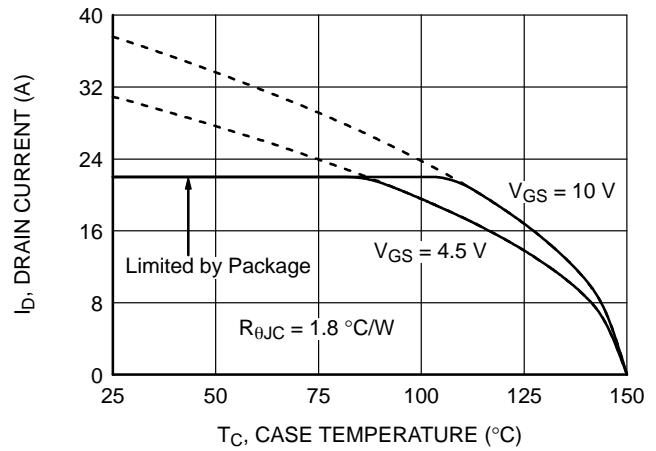


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

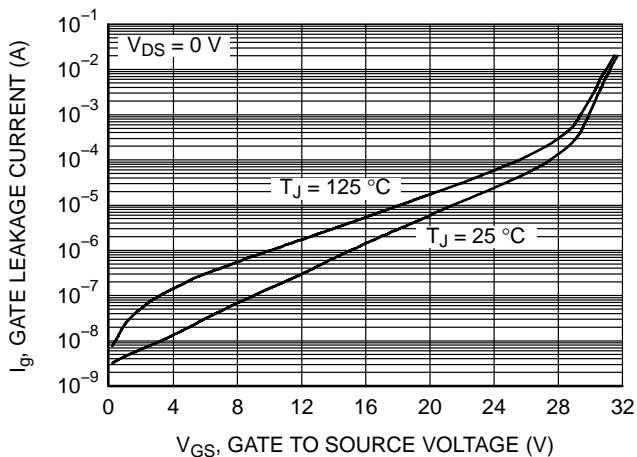


Figure 11. Gate Leakage Current vs. Gate to Source Voltage

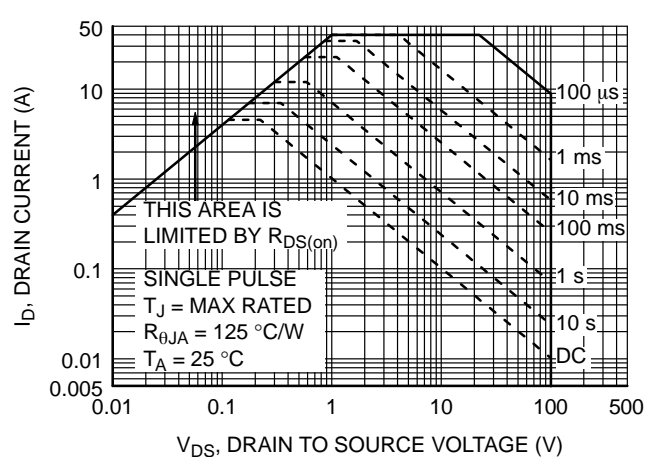


Figure 12. Forward Bias Safe Operating Area

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## TYPICAL CHARACTERISTICS ( $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted) (continued)

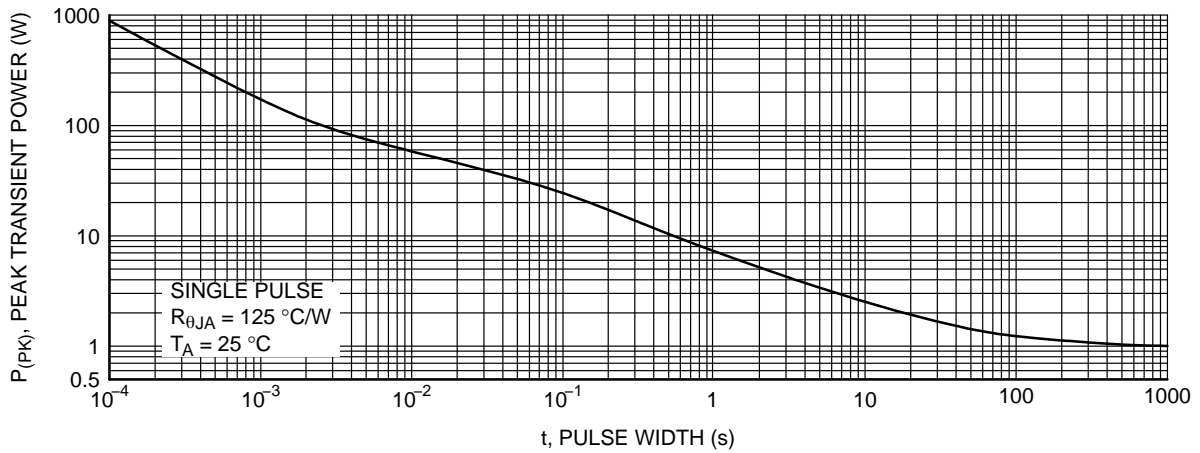


Figure 13. Single Pulse Maximum Power Dissipation

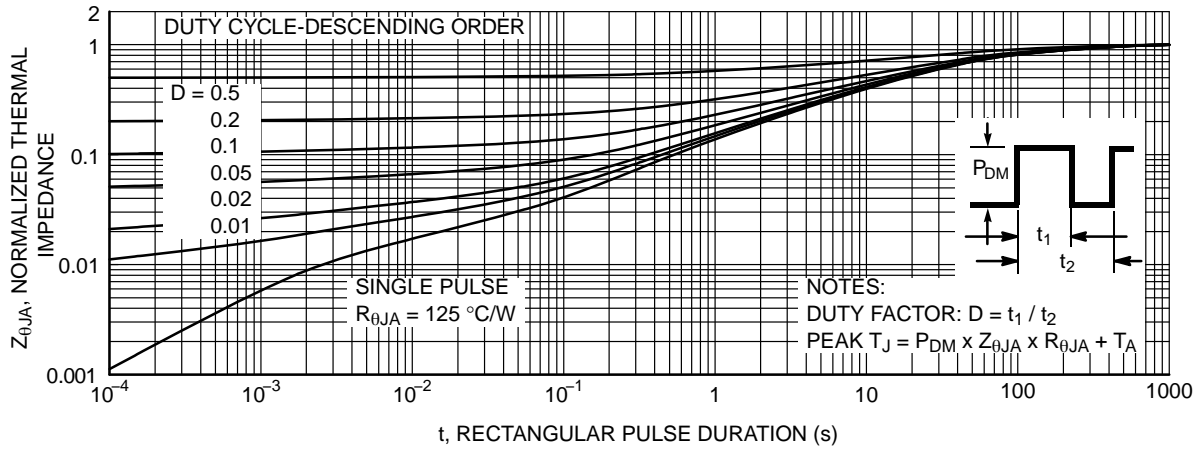


Figure 14. Junction-to-Ambient Transient Thermal Response Curve

### PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package Type	Reel Size	Tape Width	Shipping†
FDMS86102LZ	FDMS86102LZ	PQFN8 5X6, 1.27P Power 56	13"	12 mm	3000 / Tape & Reel
FDMS86102LZ-NC					

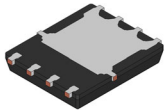
† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

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## REVISION HISTORY

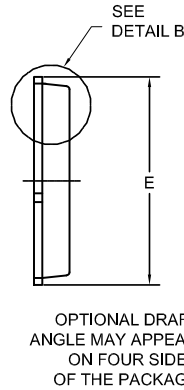
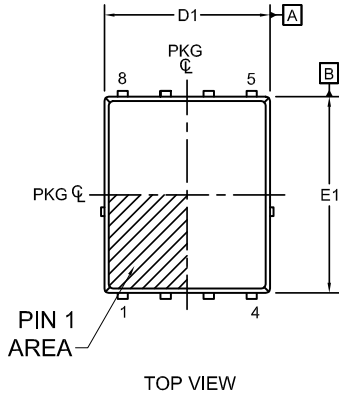
Revision	Description of Changes	Date
3	Converted the document to <b>onsemi</b> format. Added new OPN.	6/1/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.



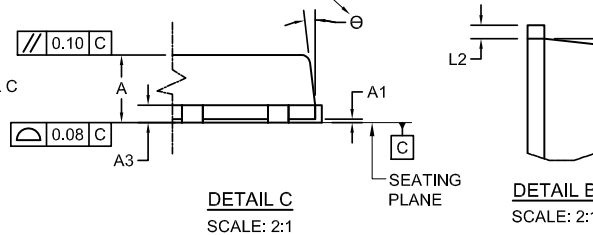
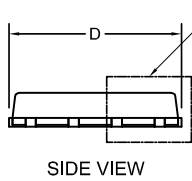
**PQFN8 5X6, 1.27P**  
**CASE 483AE**  
**ISSUE C**

DATE 21 JAN 2022

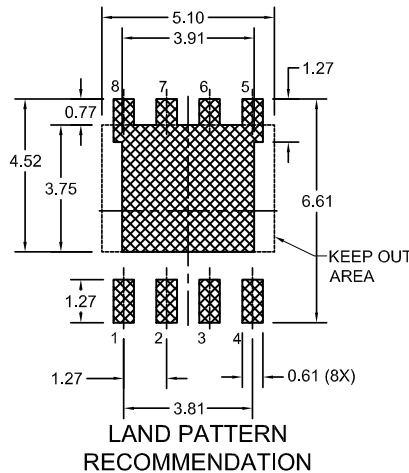
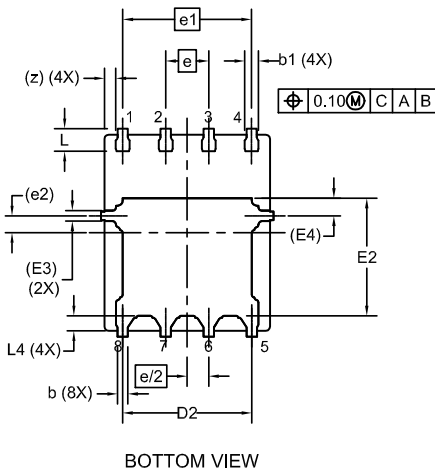


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
b	0.21	0.31	0.41
b1	0.31	0.41	0.51
A3	0.15	0.25	0.35
D	4.90	5.00	5.20
D1	4.80	4.90	5.00
D2	3.61	3.82	3.96
E	5.90	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.78
E3	0.30 REF		
E4	0.52 REF		
e	1.27 BSC		
e/2	0.635 BSC		
e1	3.81 BSC		
e2	0.50 REF		
L	0.51	0.66	0.76
L2	0.05	0.18	0.30
L4	0.34	0.44	0.54
z	0.34 REF		
θ	0°	-	12°



\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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<b>DESCRIPTION:</b>	<b>PQFN8 5X6, 1.27P</b>	<b>PAGE 1 OF 1</b>

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