

E Series Power MOSFET

PRODUCT SUMMARY

V_{DS} (V) at T_J max.	650	
$R_{DS(on)}$ max. at 25 °C (Ω)	$V_{GS} = 10$ V	0.6
Q_g max. (nC)	40	
Q_{gs} (nC)	5	
Q_{gd} (nC)	9	
Configuration	Single	

FEATURES

- Low figure-of-merit (FOM) $R_{on} \times Q_g$
- Low input capacitance (C_{iss})
- Reduced switching and conduction losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

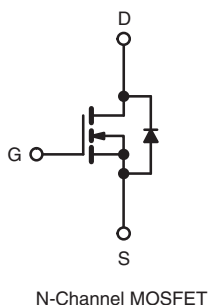
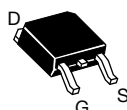


RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial
 - Welding
 - Induction heating
 - Motor drives
 - Battery chargers
 - Renewable energy
 - Solar (PV inverters)

DPAK
(TO-252)



ORDERING INFORMATION

Package	DPAK (TO-252)
Lead (Pb)-free and Halogen-free	SiHD7N60E-GE3
	SiHD7N60ET1-GE3
	SiHD7N60ET5-GE3
	SiHD7N60ET4-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	600	V
		575	
Gate-Source Voltage	V_{GS}	± 30	
Continuous Drain Current ($T_J = 150$ °C)	I_D	7	A
		5	
Pulsed Drain Current ^a	I_{DM}	18	
Linear Derating Factor		0.63	W/°C
Single Pulse Avalanche Energy ^b	E_{AS}	43	mJ
Maximum Power Dissipation	P_D	78	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	°C
Drain-Source Voltage Slope	dV/dt	3	V/ns
Reverse Diode dV/dt ^d			
Soldering Recommendations (Peak Temperature) ^c		300	°C

Notes

- Repetitive rating; pulse width limited by maximum junction temperature.
- $V_{DS} = 50$ V, starting $T_J = 25$ °C, $L = 13.8$ mH, $R_g = 25$ Ω , $I_{AS} = 2.5$ A.
- 1.6 mm from case.
- $I_{SD} \leq I_D$, $dI/dt = 100$ A/ μ s, starting $T_J = 25$ °C.

THERMAL RESISTANCE RATINGS

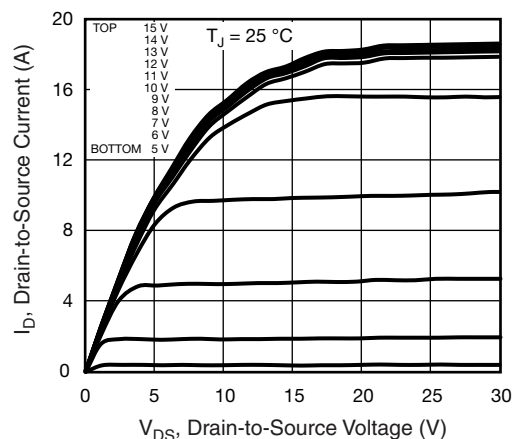
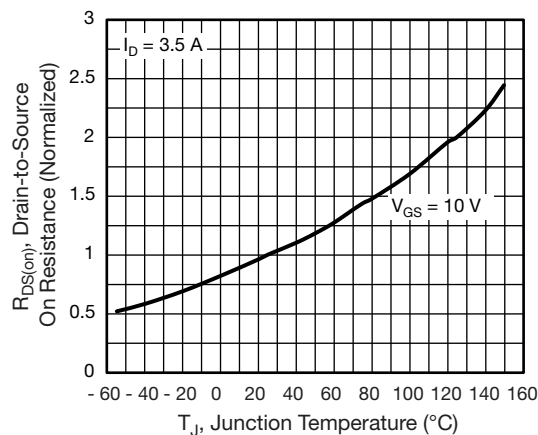
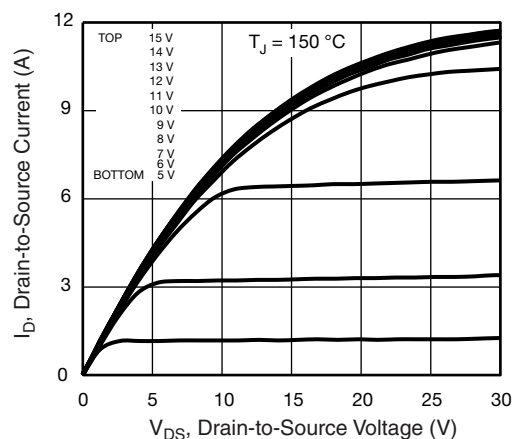
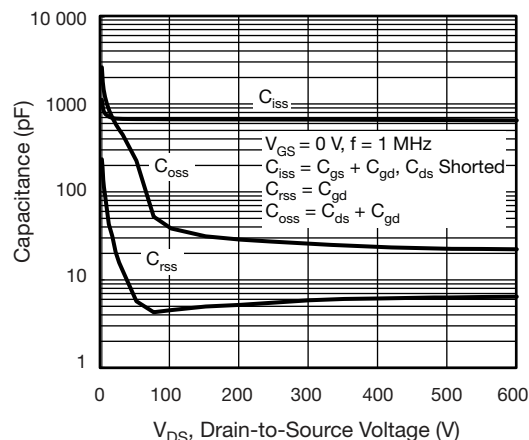
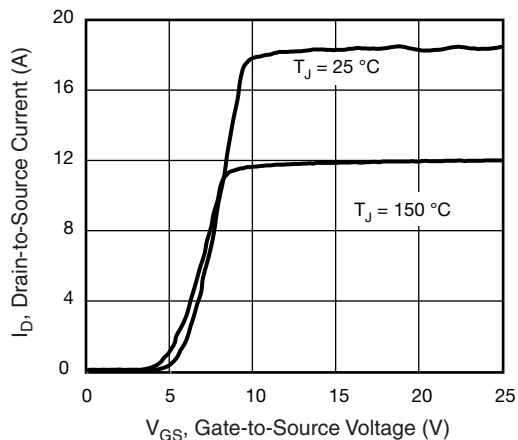
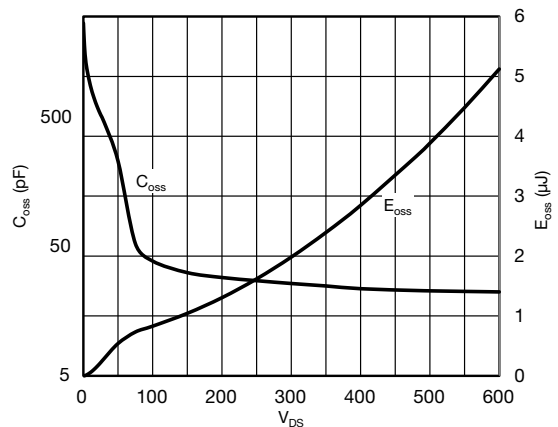
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.6	

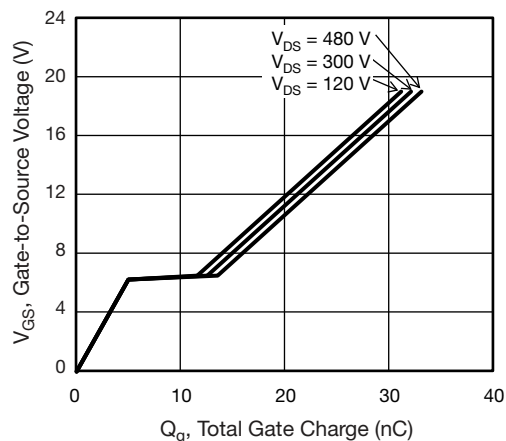
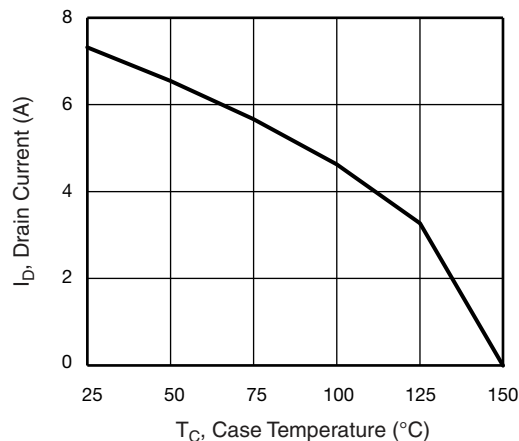
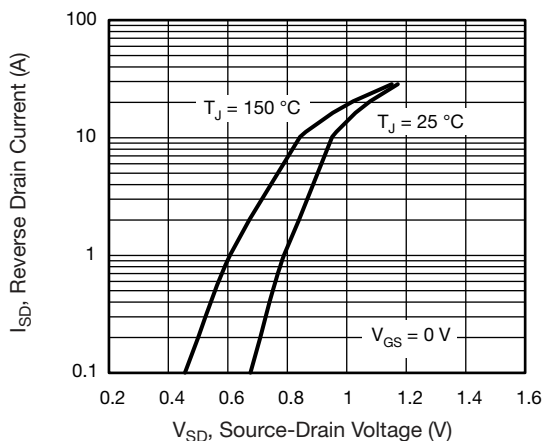
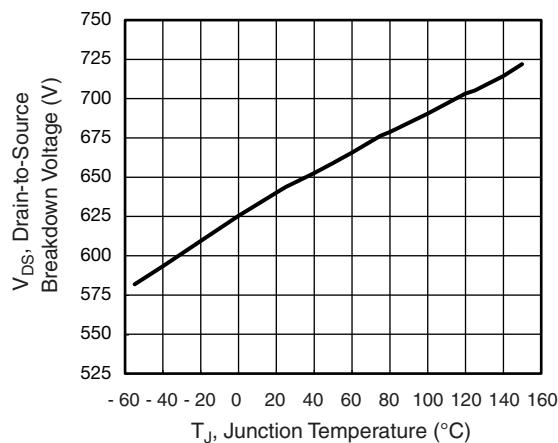
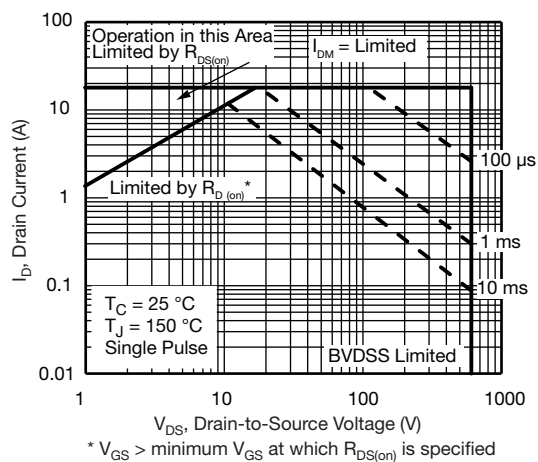
SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

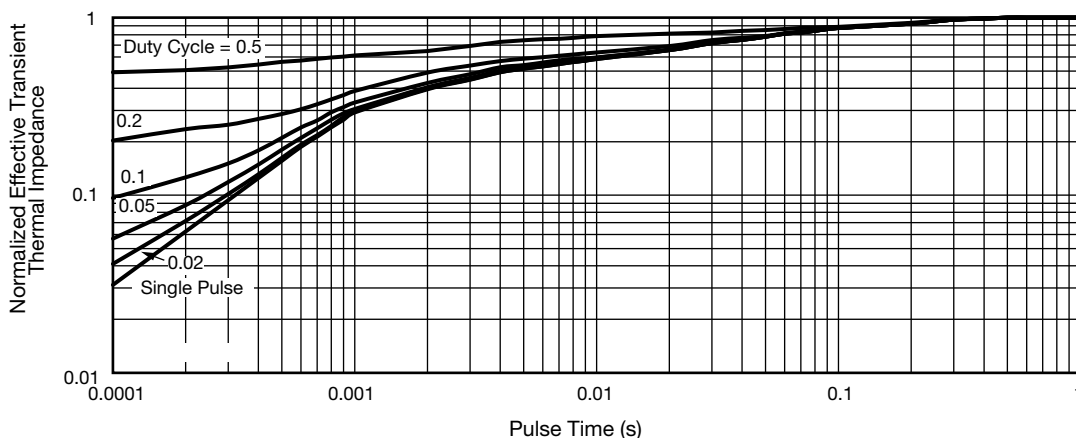
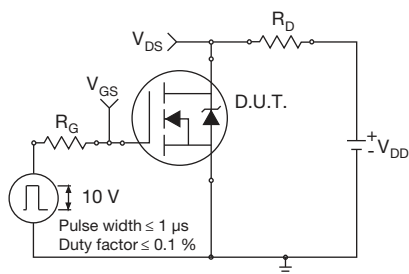
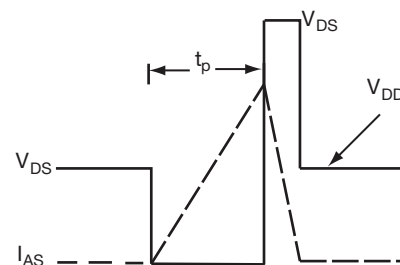
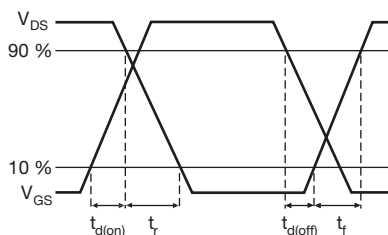
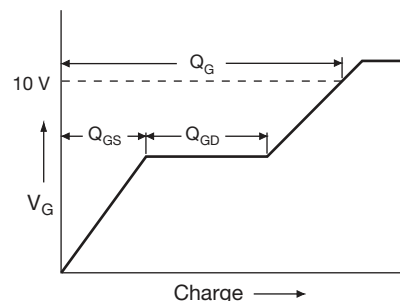
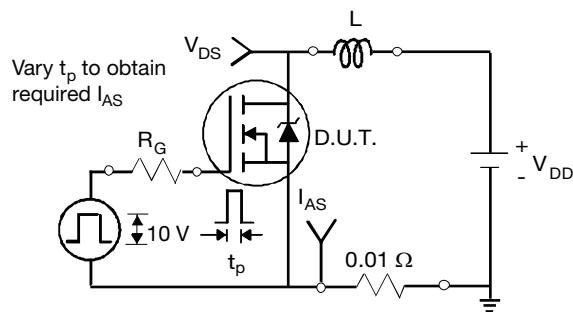
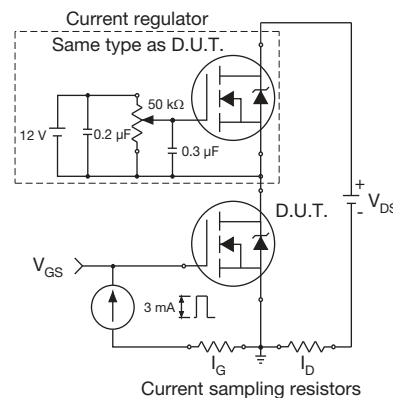
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	609	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^{\circ}\text{C}$, $I_D = 1\text{ mA}$	-	0.68	-	V/ $^{\circ}\text{C}$
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	-	4	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$	-	-	± 100	nA
		$V_{GS} = \pm 30\text{ V}$	-	-	± 1	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 600\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	1	μA
		$V_{DS} = 480\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^{\circ}\text{C}$	-	-	10	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 3.5\text{ A}$	-	0.5	0.6	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 50\text{ V}$, $I_D = 3.5\text{ A}$	-	1.9	-	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$	-	680	-	pF
Output Capacitance	C_{oss}		-	39	-	
Reverse Transfer Capacitance	C_{rss}		-	5	-	
Effective Output Capacitance, Energy Related ^a	$C_{o(er)}$	$V_{DS} = 0\text{ V to } 480\text{ V}$, $V_{GS} = 0\text{ V}$	-	34	-	
Effective Output Capacitance, Time Related ^b	$C_{o(tr)}$		-	100	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$, $I_D = 3.5\text{ A}$, $V_{DS} = 480\text{ V}$	-	20	40	nC
Gate-Source Charge	Q_{gs}		-	5	-	
Gate-Drain Charge	Q_{gd}		-	9	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 480\text{ V}$, $I_D = 3.5\text{ A}$, $V_{GS} = 10\text{ V}$, $R_g = 9.1\text{ }\Omega$	-	13	26	ns
Rise Time	t_r		-	13	26	
Turn-Off Delay Time	$t_{d(off)}$		-	24	48	
Fall Time	t_f		-	14	28	
Gate Input Resistance	R_g	$f = 1\text{ MHz}$, open drain	-	1.1	-	Ω
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	7	A
Pulsed Diode Forward Current	I_{SM}		-	-	18	
Diode Forward Voltage	V_{SD}	$T_J = 25\text{ }^{\circ}\text{C}$, $I_S = 3.5\text{ A}$, $V_{GS} = 0\text{ V}$	-	-	1.2	V
Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^{\circ}\text{C}$, $I_F = I_S = 3.5\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}$, $V_R = 20\text{ V}$	-	230	-	ns
Reverse Recovery Charge	Q_{rr}		-	1.9	-	μC
Reverse Recovery Current	I_{RRM}		-	14	-	A

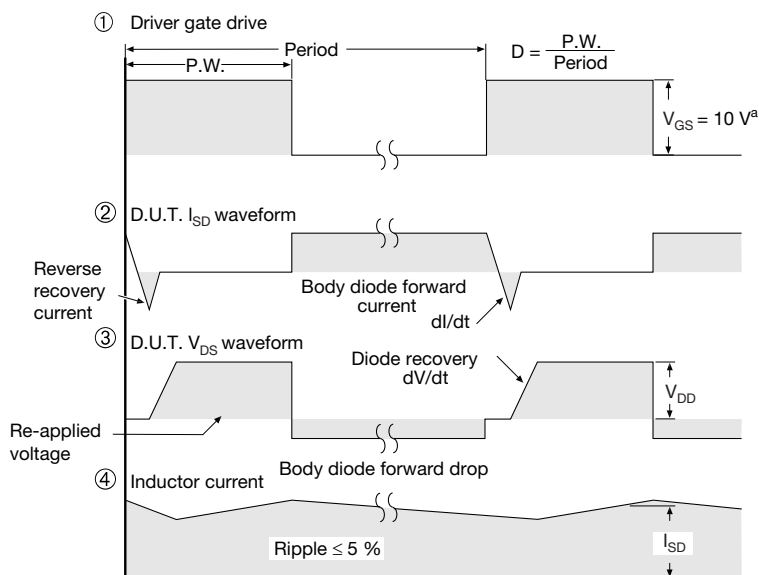
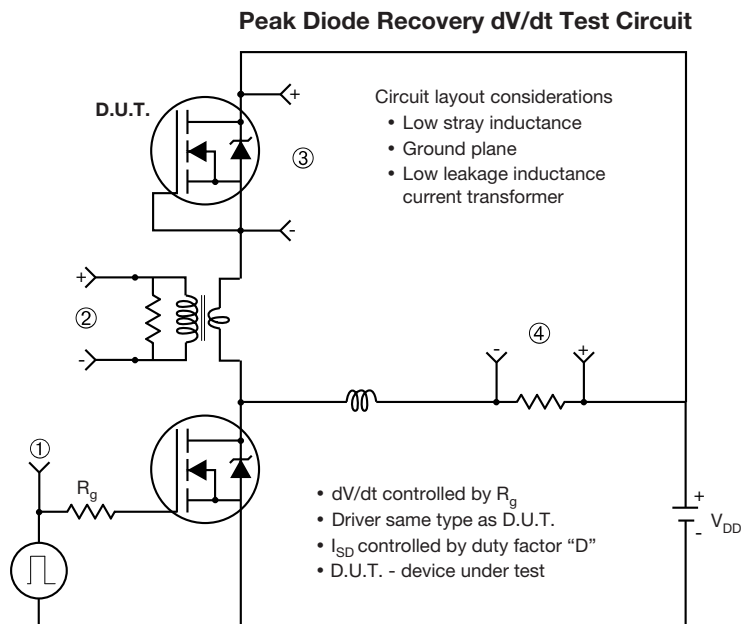
Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .
b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics

Fig. 4 - Normalized On-Resistance vs. Temperature

Fig. 2 - Typical Output Characteristics

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 3 - Typical Transfer Characteristics

Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

Fig. 10 - Maximum Drain Current vs. Case Temperature

Fig. 8 - Typical Source-Drain Diode Forward Voltage

Fig. 11 - Temperature vs. Drain-to-Source Voltage

Fig. 9 - Maximum Safe Operating Area


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

Fig. 13 - Switching Time Test Circuit

Fig. 16 - Unclamped Inductive Waveforms

Fig. 14 - Switching Time Waveforms

Fig. 17 - Basic Gate Charge Waveform

Fig. 15 - Unclamped Inductive Test Circuit

Fig. 18 - Gate Charge Test Circuit


Note

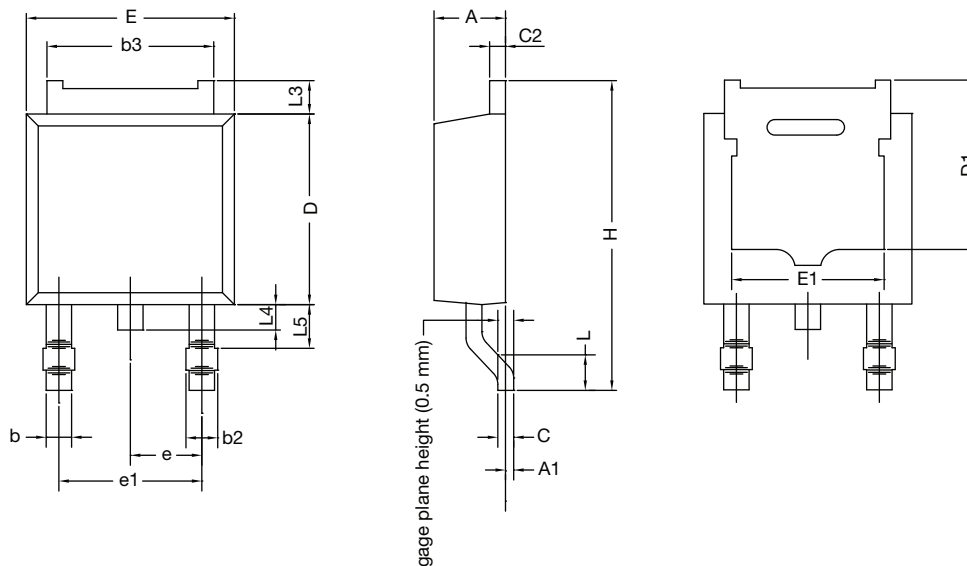
a. $V_{GS} = 5 V$ for logic level devices

Fig. 19 - For N-Channel

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TO-252AA Case Outline

VERSION 1: FACILITY CODE = Y



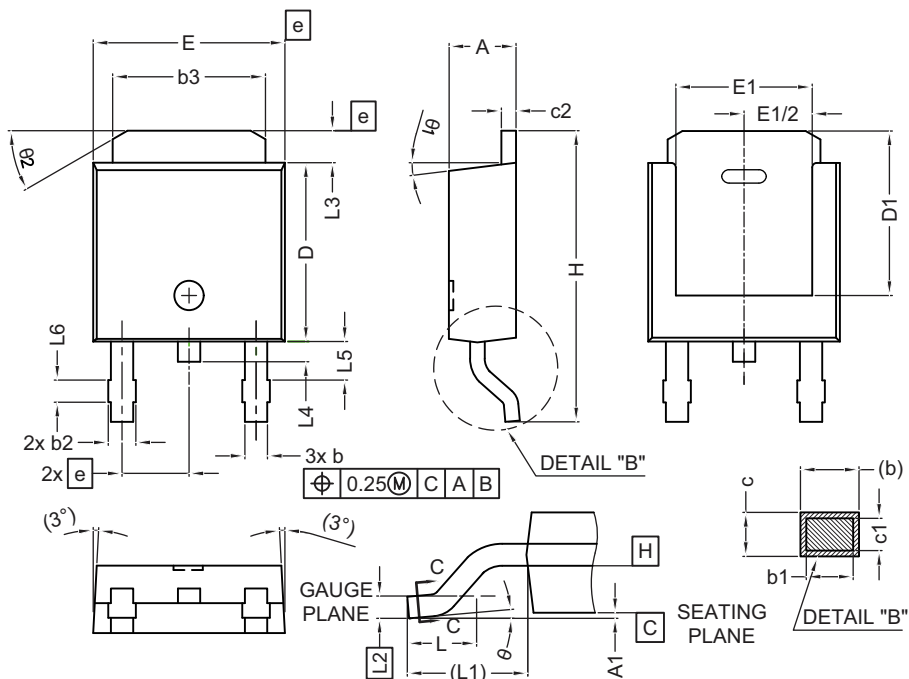
MILLIMETERS		
DIM.	MIN.	MAX.
A	2.18	2.38
A1	-	0.127
b	0.64	0.88
b2	0.76	1.14
b3	4.95	5.46
C	0.46	0.61
C2	0.46	0.89
D	5.97	6.22
D1	4.10	-
E	6.35	6.73
E1	4.32	-
H	9.40	10.41
e	2.28 BSC	
e1	4.56 BSC	
L	1.40	1.78
L3	0.89	1.27
L4	-	1.02
L5	1.01	1.52

Note

- Dimension L3 is for reference only



VERSION 2: FACILITY CODE = N



DIM.	MILLIMETERS	
	MIN.	MAX.
A	2.18	2.39
A1	-	0.13
b	0.65	0.89
b1	0.64	0.79
b2	0.76	1.13
b3	4.95	5.46
c	0.46	0.61
c1	0.41	0.56
c2	0.46	0.60
D	5.97	6.22
D1	5.21	-
E	6.35	6.73
E1	4.32	-
e	2.29 BSC	
H	9.94	10.34

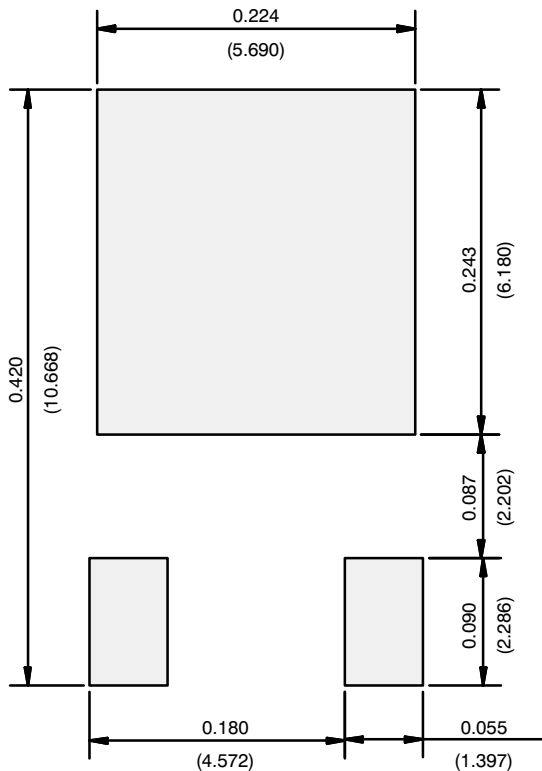
DIM.	MILLIMETERS	
	MIN.	MAX.
L	1.50	1.78
L1	2.74 ref.	
L2	0.51 BSC	
L3	0.89	1.27
L4	-	1.02
L5	1.14	1.49
L6	0.65	0.85
theta	0°	10°
theta1	0°	15°
theta2	25°	35°

Notes

- Dimensioning and tolerance confirm to ASME Y14.5M-1994
- All dimensions are in millimeters. Angles are in degrees
- Heat sink side flash is max. 0.8 mm
- Radius on terminal is optional

ECN: E22-0399-Rev. R, 03-Oct-2022
DWG: 5347

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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